Agenda	5
Source:	GBT
Subject:	CR023 r4.0 25.211 CPCH-related editorial changes, technical changes and additions and some clarification on PCPCH/AICH timing relation
Document for	Approval

Current document is a revision of Tdoc#336 which was presented to Ad-Hoc 14. Some more comments were received which have been incorporated here.

Please note that Tdocs R1(00)0200 CR023 r2 of 25.211 and R1(00)0203 CR032 of 25.211 have been combined and are replaced by this Tdoc R1(00)0336_CR023 r3

The first revision of this CR partially included most of the changes that GBT proposed in the WG1#9 meeting. These changes were approved pending changing the format of the document. However, GBT has added new items to this CR that have been discussed on the reflector. Specifically several tables have been added to provide the DPDCH and DPCCH fields for the CPCH message part. Also the editorial change of CD-AICH to CD-ICH necessitates introduction of new physicial channel which is also proposed in this CR.

The second revision of this CR (r1.0) included a correction to the previous CR regarding section 5.3.3.7.

This revision of the CR (r2.0) is based on the latest 25.211 version 3.1.1.

TSG Working Group 1 # 11 San Diego, CA, USA, Feb 29 - Mar 3, 2000



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<u>Reason for</u> <u>change:</u>	2. Introduction	of tables for CPCF on of CD-ICH as a r c editorial changes a	new phys	ical chanr	nel			
Clauses affected	<u>d:</u> <u>3.3, 5.2</u>	2 <mark>.2.2.1, 5.2.2.2.4,</mark>	5.2.2.2.	5 <mark>, 5.3.2.3</mark>	, <mark>5.3.3.</mark>	6, <u>5.3.3.7, 6, 7</u> .	4	
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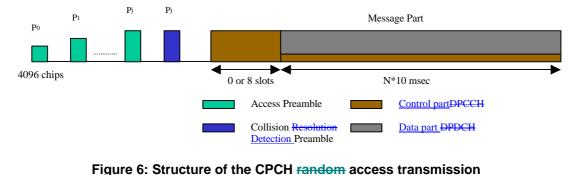
3 Abbreviations

For the purposes of	the present document, the following abbreviations apply:									
AI	Acquisition Indicator									
AICH	Acquisition Indicator Channel									
AP	Access Preamble									
BCH	Broadcast Channel									
CCPCH	Common Control Physical Channel									
CCTrCH	Coded Composite Transport Channel									
CD	Collision Detection									
CPCH	Common Packet Channel									
CPICH	Common Pilot Channel									
DCH	Dedicated Channel									
DPCCH	Dedicated Physical Control Channel									
DPCH	Dedicated Physical Channel									
DPDCH	Dedicated Physical Data Channel									
DSCH	Downlink Shared Channel									
DSMA-CD	Digital Sense Multiple Access – Collison Detection									
DTX	Discontinuous Transmission									
FACH	Forward Access Channel									
FBI	Feedback Information									
MUI	Mobile User Identifier									
PCH	Paging Channel									
P-CCPCH	Primary Common Control Physical Channel									
PCPCH	Physical Common Packet Channel									
PDSCH	Physical Downlink Shared Channel									
PI	Page Indicator									
PICH	Page Indicator Channel									
PRACH	Physical Random Access Channel									
PSC	Primary Synchronisation Code									
RACH	Random Access Channel									
RNC	Radio Network Controller									
S-CCPCH	Secondary Common Control Physical Channel									
SCH	Synchronisation Channel									
SF	Spreading Factor									
SFN	System Frame Number									
SSC	Secondary Synchronisation Code									
STTD	Space Time Transmit Diversity									
TFCI	Transport Format Combination Indicator									
TSTD	Time Switched Transmit Diversity									
TPC	Transmit Power Control									
UE	User Equipment									
UTRAN	UMTS Terrestrial Radio Access Network									

5.2.2.2.1 CPCH transmission

The CPCH transmission is based on DSMA-CD approach with fast acquisition indication. The UE can start transmission at <u>the beginning of</u> a number of well-defined time-<u>intervals</u>, relative to the frame boundary of the received BCH of the current cell. The access slot timing and structure is identical to RACH in section 5.2.2.1.1. The structure of the CPCH random access transmission is shown in figure 6. The <u>PCPCH</u> random access transmission consists of one or several Access Preambles [A-P] of length 4096 chips, one

Collision Detection Preamble (CD-P) of length 4096 chips, a DPCCH Power Control Preamble (PC-P) which is either 0 slots or 8 slots in length, and a message of variable length Nx10 ms.



5.2.2.2.4 CPCH power control preamble part

The power control preamble segment is a <u>DPCCH-PCPCH</u> Power Control Preamble (PC-P). <u>The following</u> table 9 is identical to Rows 2 and 4 of table 2 in section 5.2.1. Table 9 defines the DPCCH fields which only include Pilot, FBI and TPC bits. The Power Control Preamble length is a parameter which shall take the values 0 or 8 slots, as set by the higher layers.

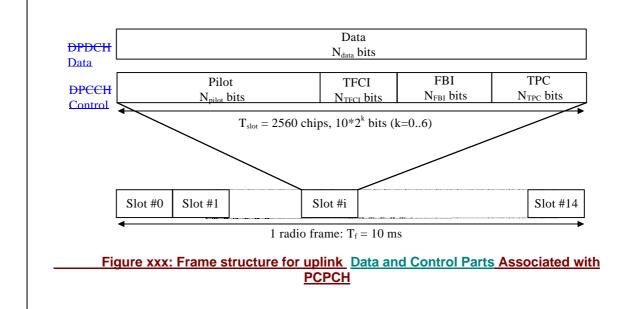
Table 9: DPCCH fields for CPCH	power control preamble segment
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Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N _{pilot}	N _{tfci}	N _{FBI}	N _{TPC}
0	15	15	256	150	10	8	0	0	2
1	15	15	256	150	10	7	0	1	2

5.2.2.2.5 CPCH message part

Figure 1in section 5.2.1 shows the structure of the CPCH message part. Each message consists of up to N_Max_frames 10 ms frames. N_Max_frames is a higher layer parameter. Each 10 ms frame is split into 15 slots, each of length $T_{slot} = 2560$ chips. Each slot consists of two parts, a data part that carries higher layer information and a control part that carries Layer 1 control information. The data and control parts are transmitted in parallel.

Figure xxx shows the frame structure of the uplink common packet physical channel. Each frame of length 10 ms is split into 15 slots, each of length $T_{slot} = 2560$ chips, corresponding to one power-control period.



The data part consists of $10*2^k$ bits, where k = 0, 1, 2, 3, 4, 5, 6, corresponding to spreading factors of 256, 128, 64, 32, 16, 8, 4 respectively. Note that various rates might be mapped to different signature sequences.

The spreading factor for the <u>UL DPCCH PCPCH</u> (message control part) is 256. The entries in <u>the</u> <u>following</u> table $\pm xxx$ corresponding to spreading factors of 256 and below and table 2 [both in section 5.2.1] apply to the <u>DPDCH data part of and DPCCH fields respectively for the P</u>-CPCH message part.

Table xxx: Data part - of the PCPCH message part

<u>Slot Format #i</u>	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	<u>SF</u>	<u>Bits/</u> Frame	<u>Bits/</u> Slot	<u>N_{data}</u>
<u>0</u>	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	<u>10</u>
1	<u>30</u>	<u>30</u>	<u>128</u>	<u>300</u>	<u>20</u>	<u>20</u>
2	<u>60</u>	<u>60</u>	<u>64</u>	<u>600</u>	<u>40</u>	<u>40</u>
3	<u>120</u>	<u>120</u>	<u>32</u>	<u>1200</u>	<u>80</u>	<u>80</u>
4	<u>240</u>	<u>240</u>	<u>16</u>	<u>2400</u>	<u>160</u>	<u>160</u>
<u>5</u>	<u>480</u>	<u>480</u>	<u>8</u>	<u>4800</u>	<u>320</u>	<u>320</u>
<u>6</u>	<u>960</u>	<u>960</u>	<u>4</u>	<u>9600</u>	<u>640</u>	<u>640</u>

The following table xxx corresponds to the control part of the PCPCH message. Table xxx: Control Part of the PCPCH message

<u>Slot</u> Format <u>#i</u>	<u>Channel Bit</u> <u>Rate (kbps)</u>	<u>Channel</u> <u>Symbol Rate</u> <u>(ksps)</u>	<u>SF</u>	<u>Bits/</u> Frame	<u>Bits/</u> <u>Slot</u>	<u>Npilot</u>	<u>N_{tpc}</u>	<u>N_{TFCI}</u>	<u>N_{FBI}</u>
<u>0</u>	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	<u>6</u>	<u>2</u>	<u>2</u>	<u>0</u>
<u>1</u>	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	<u>8</u>	2	<u>0</u>	<u>0</u>
2	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	<u>5</u>	2	2	<u>1</u>
<u>3</u>	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	<u>7</u>	2	<u>0</u>	<u>1</u>
4	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	6	2	0	2
<u>5</u>	<u>15</u>	<u>15</u>	<u>256</u>	<u>150</u>	<u>10</u>	5	1	2	2
_				·	·				

5.3.2.3 DL-DPCCH for CPCH

The spreading factor for the UL-DPCCH (message control part) is 256. The spreading factor for the DL-DPCCH (message control part) is 512. The following table 15 shows the DL-DPCCH fields (message control part) which are identical to the first row of table 11 in section 5.3.2.

Table 15: DPDCH and DPCCH fields for CPCH message transmission

Slot Format	Channel Bit	Channel Symbol	SF	E	Bits/Frame		Bits/ Slot	DPI Bits	DCH /Slot	DPCCH Bits/Slot				
#i	Rate (kbps)	Rate (ksps)		DPDCH	DPCCH	тот		NData1	NData2	NTFCI	NTPC	NPilot		
0	15	7.5	512	60	90	150	10	2 0	2 4	0	2	4		

5.3.3.6 Acquisition Indicator Channel (AICH)

The Acquisition Indicator channel (AICH) is a physical channel used to carry Acquisition Indicators (AI). Acquisition Indicator AI_s corresponds to signature s on the PRACH or PCPCH. Note that for PCPCH, the AICH either corresponds to an access preamble or a CD preamble. The AICH corresponding to the access preamble is an AP AICH and the AICH corresponding to the CD preamble is a CD AICH. The AP AICH and CD AICH use different channelization codes, see further[4], Section 4.3.3.2.

Figure 19 illustrates the structure of the AICH. The AICH consists of a repeated sequence of 15 concecutive *access slots* (AS), each of length 40 bit intervals. Each access slot consists of two parts, an *Acquisition-Indicator* (AI) part consisting of 32 real-valued symbols $a_0, ..., a_{31}$ and an unused part consisting of 8 real-valued symbols $a_{32}, ..., a_{39}$.

The phase reference for the AICH is the Primary CPICH.

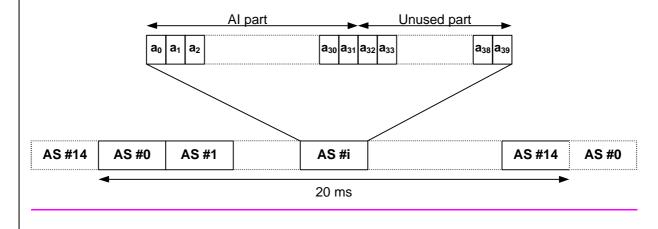


Figure 19: Structure of Acquisition Indicator Channel (AICH)

The real-valued symbols a₀, a₁, ..., a₃₁ in Figure 19 are given by

$$\mathbf{a}_{j} = \sum_{s=0}^{15} \mathbf{A}\mathbf{I}_{s}\mathbf{b}_{s,j}$$

where AI_s, taking the values +1, -1, and 0, is the acquisition indicator corresponding to signature s and the sequence $b_{s,0}, ..., b_{s,31}$ is given by Table 20.

The real-valued symbols a₃₂, a₃₃, ..., a₃₉ in Figure 19 are undefined.

In case STTD-based open-loop transmit diversity is applied to AICH, STTD encoding according to section 5.3.1.1.1 is applied to each sequence $b_{s,0}$, $b_{s,1}$, ..., $b_{s,31}$ separately before the sequences are combined into AICH symbols a_0 , ..., a_{31} .

Table 20: AICH signature patterns

s	b _{s,0} , b _{s,1} , b _{s,31}																															
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 <u>-3,0,</u>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1
2	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1
3	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1
4	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1
5	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1
6	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1
7	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
9	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
10	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
11	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1
12	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
13	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1
14	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1
15	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1

5.3.3.8 Page Indicator Channel (PICH)

6 Mapping of transport channels onto physical channels

Figure 21 summarises the mapping of transport channels onto physical channels.

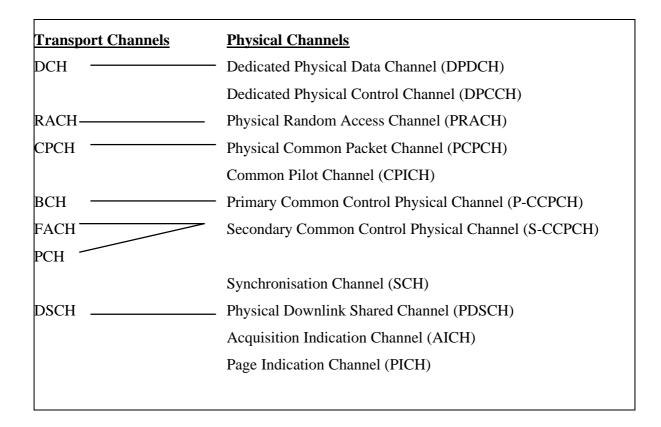


Figure 21: Transport-channel to physical-channel mapping

The DCHs are coded and multiplexed as described in [3], and the resulting data stream is mapped sequentially (first-in-first-mapped) directly to the physical channel(s). The mapping of BCH and FACH/PCH is equally straightforward, where the data stream after coding and interleaving is mapped sequentially to the Primary and Secondary CCPCH respectively. Also for the RACH, the coded and interleaved bits are sequentially mapped to the physical channel, in this case the message part of the random access burst on the PRACH.

7.4 PCPCH/AICH timing relation

Transmission of random access bursts on the PCPCH is aligned with access slot times. The timing of the access slots is derived from the received Primary CCPCH timing The transmit timing of access slot n starts $n \times 20/15$ ms after the frame boundary of the received Primary CCPCH, where n = 0, 1, ..., 14. In addition, transmission of access preambles in PCPCH is limited to the allocated access slot subchannel group which is assigned by higher layer signalling to each CPCH set. Twelve access slot subchannels are defined and PCPCH may be allocated all subchannel slots or any subset of the twelve subchannel slots. The access slot subchannel identification is identical to that for the RACH and is described in table 6 of section 6.1 of [5]. Everything in the previous section [PRACH/AICH] applies to this section as well. The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationship between CD-Preamble and CD-AICH is identical to RACH Preamble and AICH. The timing relationship between CD-AICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is

set to zero or one, the following PCPCH/AICH timing values apply.<u>+</u>. Note that the following apply when the RACH and CPCH preamble resources are not shared:

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-AICH.

 τ_{p-p} = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

 $\tau_{p-al} = Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on <math>T_{cpch}$

- $\tau_{a1-cdp} =$ <u>Minimum t</u>Time between receipt of AP-AICH and transmission of the CD Preamble has one value: 7680 chips.
 - $\tau_{p-cdp} =$ <u>Maximum t</u>Time between the last AP and CD Preamble. is either 3 or 4 access slots, depending on T_{cpch}
 - $\tau_{cdp-a2} =$ Time between the CD Preamble and the CD-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}
 - $\tau_{cdp-pcp} =$ Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on $T_{cpch.}$

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 25 illustrates the PCPCH/AICH timing relationship when T_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.

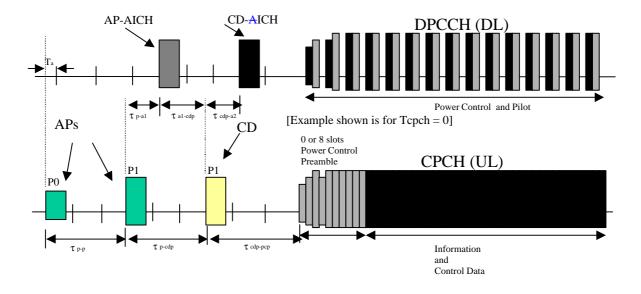


Figure 25: Timing of PCPCH and AICH transmission as seen by the UE, with $T_{\mbox{\scriptsize cpch}}\mbox{=}0$