TSG-RAN Working Group 1 meeting #11 **TSGR1#11(00)0289**

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Agenda Item:
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To: TSG RAN WG1
Title: Uplink synchronization for low chip rate TDD option
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Introduction

Uplink synchronisation is one of the most important features of low chip rate TDD option. It will lead to higher capacity and simplify the demodulator in Node B.

This paper gives an introduction to the establishment and maintenance of the uplink synchronization .

Uplink Synchronisation

1.The establishment of uplink synchronisation

1.1 Preparation of uplink sychronisation (downlink synchronisation)

When a UE is powered on, it will search the operating frequency band and try to find several strongest SYNC sequences in downlink pilot time slot DwPTS from the nearby Node Bs. After read the cell broadcast information in BCH followed by DwPTS, the UE will keep downlink synchronization with DwPTS. This period is establishment of downlink synchronisation. Only after the downlink synchronisation is established, the UE can start to establish the uplink sychronisation.

1.2 Open- and closed- loop uplink synchronisation

Although the UE can receive the downlink synchronization signal from the Node B at this moment, the distance to Node B is still uncertain which may lead to unsynchronized uplink trasmission. The transmission power and timing advance used for the first transmission of the UE are set according to the received power level and the transmission power of Node B (open loop control). If the Node B detect the UE's transmission in the searching window, it will evaluate the received power level and timing. In the next down link time slot, the Node B will send the adjustment information to UE to modify the timing and power level for transmission and establish the uplink synchronisation procedure (closed loop control).

The procedure of establishing uplink synchronisation usually is used in access procedure. It also can be used to re-establish the the uplink synchronisation when uplink is out of synchronisation.

2. Maintenance of uplink synchronisation

The maintenance of the uplink synchronization is important in the proposed system, the midamble field in frame structure is used in each traffic channel of each main uplink time slot.
In each main uplink time slot, the midamble in each code channel is different. The BS can estimate the power level and timing shift by measuring the midamble field of each code channel in

the same time slot. Then in the following downlink time slot, the BS will send the L1 control signalling of power control (PC) and Timing Advance (TA) by this mechanism, and then enable the UE to adjust its Tx time correctly. These procedures guarantee the reliability of the uplink synchronisation.The uplink synchronization can be checked once per TDD sub-frame. The accuracy in uplink synchronization remains in 1/2 chip duration.

3. The estimation of the distance between Node B and UE

The uplink synchronization asks the UE to transmit in advance a time shift (ΔT), which depends upon the distance between Node B and the UE. Obviously, one may estimate the distance between Node B and the UE by using the known time shift that:

$$d = C * \Delta T \qquad (2)$$

where C is the speed of light.

It is obviously that uplink synchronization can reduce the Multiple-Access-Interference and increase the capacity (theoretically 3dB when multipath could be negligible) . And for other features adopted in the low chip rate system , such as smart antenna , uplink synchronisation will provide a simple solution , the detail is given in another proposal by CWTS.

Conclusion

The low chip rate TDD option of 1.28Mcps has already included in the specification. Based on the descriptions above and to enable the low chip rate with its specific properties, it's proposed to include this new feature for low chip rate TDD option in new clause 8.3.1 of TR 25.928.

---------- changes to 25.928 begin ----------

8.3 Synchronisation and Cell Search Procedures

8.3.1 Uplink Synchronisation

8.3.1.1 The establishment of uplink synchronisation

8.3.1.1.1 Preparation of uplink sychronisation (downlink synchronisation)

When a UE is powered on, it will search the operating frequency band and try to find several strongest SYNC sequences in downlink pilot time slot DwPTS from the nearby Node Bs. After read the cell broadcast information in BCH followed by DwPTS, the UE will keep downlink synchronization with DwPTS. This period is establishment of downlink synchronisation. Only after the downlink synchronisation is established, the UE can start to establish the uplink sychronisation.

8.3.1.1.2 Open- and closed- loop uplink synchronisation

Although the UE can receive the downlink synchronization signal from the Node B at this moment, the distance to Node B is still uncertain which may lead unsynchronized uplink trasmission. The transmission power and timing advance used for the first transmission of the UE are set according to the received power level and the transmission power of Node B (open loop control). If the Node B detect the UE's transmission in the searching window, it will evaluate the received the power level and timing. In the next down link time slot, the Node B will send the adjustment information to UE to modify the timing and power level for transmission and establish the uplink synchronisation procedure (closed loop control).

The establishing procedure of uplink synchronisation usually used in access procedure. It also can be used for the re-establish of the uplink synchronisation when uplink is out of synchronisation.

8.3.1.2 Maintenance of uplink synchronisation

The maintenance of the uplink synchronization is important in the proposed system, the midamble field in frame structure is used in each traffic channel of each main uplink time slot.
In each main uplink time slot, the midamble in each code channel is different. The BS can estimate the power level and timing shift by measuring the midamble field of each code channel in the same time slot. Then in the following downlink time slot, the BS will send the L1 control signalling of power control (PC) and Timing Advance (TA) by use of this mechanism. and then enable the UE to adjust its Tx time correctly. These procedures guarantee the reliability of the uplink synchronisation.The uplink synchronization can be checked once per TDD sub-frame. The accuracy in uplink synchronization remains in 1/2 chip duration.

8.3.1.3. The estimation of the distance between Node B and UE

The uplink synchronization asks the UE to transmit in advance a time shift (ΔT), which depends upon the distance between Node B and the UE. Obviously, one may estimate the distance between Node B and the UE by use the known time shift that:

$$d = C * \Delta T \qquad (2)$$

where C is the speed of light.

---------- changes to 25.928 end ----------