help.doc

e.g. for 3GPP use the format TP-99xxx or for SMG, use the format P-99-xxx

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Form: CR cover sheet, version 2 for 3GPP and SMG The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc Proposed change affects: (U)SIM ME X UTRAN / Radio X Core Network (at least one should be marked with an X) (U)SIM ME X UTRAN / Radio X Core Network									
Source:	Siemens						Date:	2000-02-	21
Subject:	Mapping of	Physical Channel	s and L1	Signalli	ng Chan	nels			
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3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AICH	Acquisition Indicator Channel
AP	Access Preamble
BCH	Broadcast Control Channel
CCPCH	Common Control Physical Channel
CD	Collision Detection
CPCH	Common Packet Channel
CPICH	Common Pilot Channel
DCH	Dedicated Channel
DPCH	Dedicated Physical Channel
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
FDD	Frequency Division Duplex
Mcps	Mega Chip Per Second
N-ICH	Non Slotted Indicator Channel
OVSF	Orthogonal Variable Spreading Factor (codes)
PDSCH	Physical Dedicated Shared Channel
PICH	Page Indication Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
SCH	Synchronisation Channel
S-ICH	Slotted Indicator Channel
SSC	Secondary Synchronisation Code
SF	Spreading Factor
UE	User Equipment
USTS	Uplink Synchronous Transmission Scheme

4 Uplink spreading and modulation

4.1 Overview

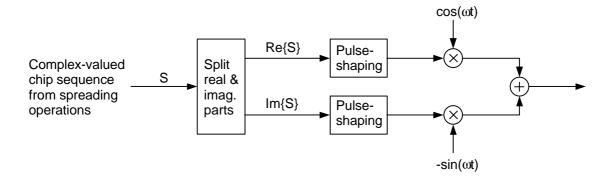
Spreading is applied to the physical channels. It consists of two operations. The first is the channelization operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation, where a scrambling code is applied to the spread signal.

With the channelization, data symbols on so-called I- and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I- and Q-branches are further multiplied by complex-valued scrambling code, where I and Q denote real and imaginary parts, respectively.

4.2 Spreading

4.2.1 DPCCH/DPDCH)

Figure 1 illustrates the principle of the uplink spreading of DPCCH and DPDCHs. The binary DPCCH and DPDCHs to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value -1. The DPCCH is spread to the chip rate by the channelization code c_c , while the *n*:th DPDCH called DPDCH_n is spread to the chip rate by the channelization code $c_{d,n}$. One DPCCH and up to six parallel DPDCHs can be transmitted simultaneously, i.e. $0 \le n \le 6$.



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The pulse-shaping characteristics are described in [3].

5 Downlink spreading and modulation

5.1 Spreading

Figure 8 illustrates the spreading operation for all downlink physical channels except SCH, i.e. for P-CCPCH, S-CCPCH, CPICH, A<u>S</u>-ICH, <u>PN-</u>ICH, and downlink DPCH. The non-spread physical channel consists of a sequence of real-valued symbols. For all channels except <u>AS</u>-ICH, the symbols can take the three values +1, -1, and 0, where 0 indicates DTX. For <u>AS</u>-ICH, the symbol values depend on the exact combination of acquisition indicators to be transmitted, compare [2] Section 5.3.3.6.

Each pair of two consecutive symbols is first serial-to-parallel converted and mapped to an I and Q branch. The mapping is such that even and odd numbered symbols are mapped to the I and Q branch respectively. For all channels except A<u>S</u>-ICH, symbol number zero is defined as the first symbol in each frame. For A<u>S</u>-ICH, symbol number zero is defined as the first symbol in each frame. For A<u>S</u>-ICH, symbol number zero is defined as the first symbol in each frame. For A<u>S</u>-ICH, symbol number zero is defined as the first symbol in each access-slot. The I and Q branches are then spread to the chip rate by the same real-valued channelization code $C_{ch,SF,m}$. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips is scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. In case of P-CCPCH, the scrambling code is applied aligned with the P-CCPCH frame boundary, i.e. the first complex chip of the spread P-CCPCH frame is multiplied with chip number zero of the scrambling code. In case of other downlink channels, the scrambling code is applied aligned with the scrambling code applied to the P-CCPCH. In this case, the scrambling code is thus not necessarily applied aligned with the frame boundary of the physical channel to be scrambled.