TSG-RAN Working Group 1 meeting #11
San Diego, CA, USA
February 29 – March 3, 2000

TSGR1#11(00)0239

Agenda item:

Source: Ericsson

Title: CR 25.211-028r1: Timing of PDSCH

Document for: Approval

In R1-00-0100, CR 25.211-028, it was proposed to change the timing of the PDSCH to start earliest 15 slots after the start of the associated DPCH frame.

It has then been further proposed to move the timing to start earliest 18 slots after the start of the DPCH frame (i.e. 3 slots after the end of the DPCH frame), to leave more time for processing of the TFCI. This CR is an revision of the CR in R1-00-0100, with an updated timing relation that changes 15 slots delay into 18 slots.

3GPP TSG RAN WG1 Meeting #11
San Diego, CA, USA, Feb 29 – Mar 3, 2000

Document ????99???
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	028r1	Current Version:	3.1.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #7	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*

(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source: Ericsson **Date:** 2000-02-21

Subject: Timing of PDSCH

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: The relative timing between the start of a DPCH frame and the associated PDSCH frame should be increased in order to lower the complexity of the terminal.

Clauses affected: 7.5

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 28.

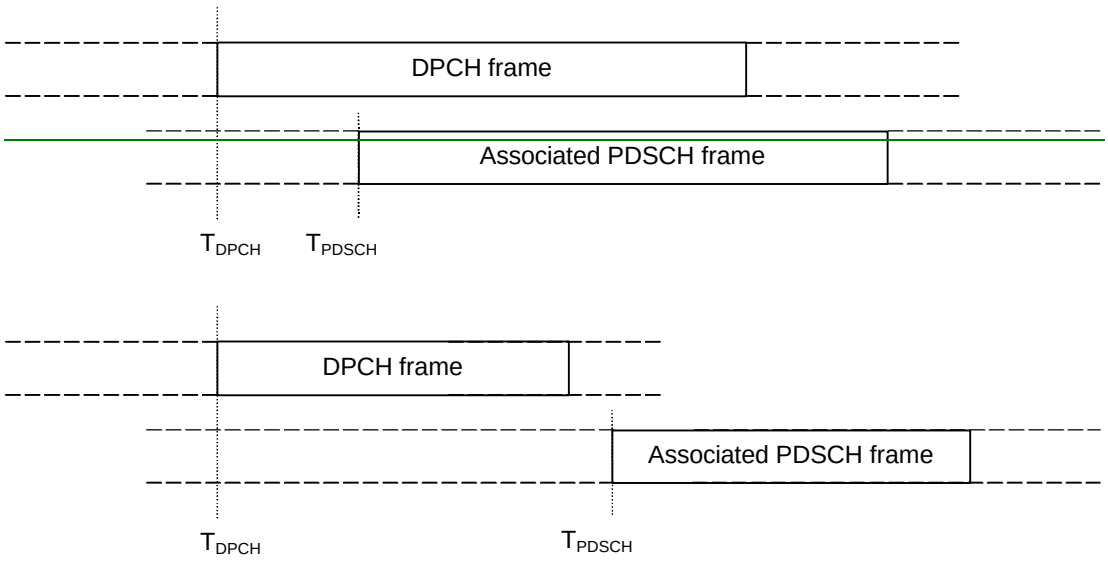

Figure 28: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation ~~35840 chips < T_{DPCH} - T_{PDSCH} ≤ 2560 chips~~ 46080 chips ≤ T_{PDSCH} - T_{DPCH} < 84480 chips, i.e. the associated PDSCH frame starts anywhere between three slot after the end of the DPCH frame~~1 slot before or~~ up to 18~~4~~ slots behind the end of the DPCH frame.