TSG-RAN Working Group 1 meeting #11 **_TSGR1#11-00-0235_**
San Diego, USA, Feb. 29th – March 3rd , 2000

Agenda Item : AH 04, 14

Source : LG Information & Communications, Ltd.

Title : CR 25.212-047: TFCI coding for FDD

Document for : Approval

Abstract

According to current TFCI basis, in the case of non-split TFCI there is minimum Hamming distance loss by 2 and in the case of split mode there is minimum Hamming distance loss by 1 after puncturing.

This contribution proposes the TFCI coding, which minimizes the minimum Hamming distance loss after puncturing by simply changing the TFCI basis. By using the proposed change of basis, we see there is no minimum distance loss after 2 bits puncturing when the number of TFCI information bits is 2 ~ 4 and there is only one loss when the number of TFCI information bits is 5. Similarly, in the case of (16,5) split mode we also see no minimum distance loss after 1 bit puncturing when TFCI information is 2~4.

1. Introduction

There were some discussions about the order of TFCI basis and the real size of TFCS though e-mail discussion after WG1#10 meeting. According to table 1 of section 5 of TR25.926 V1.0.0(1999-12), 3GPP TSGR Access Network; UE Radio Access Capabilities, we see that the size of the TFCI to TFCS mapping table to be handled by the UE is "16,32,48,64,96,128,256,512,1024" in the case of downlink and "4,8,16,32,48,64,96,128,256,512,1024" in the case of uplink.

Through e-mail discussion we found that the minimization of minimum Hamming distance loss after puncturing can be obtained by simply changing the TFCI basis. Thus there is no reason not to take this advantage since the performance TFCI is so important. For the safe solution, this contribution also includes the TFCI coding considering the case of the number of TFCI bit is one.

2. Proposed TFCI coding

This contribution proposes the optimized TFCI coding which maximize the minimum Hamming distance after puncturing. The proposed TFCI coding is based on the followings

- change of TFCI basis order (movement of all “1” basis)
- code repetition is used for coding when the number of TFCI bit is one

2.1. Non-split mode

The TFCI bits are encoded using a (32, 10) sub-code of the second order Reed-Muller code. The coding procedure is as shown in figure 1.

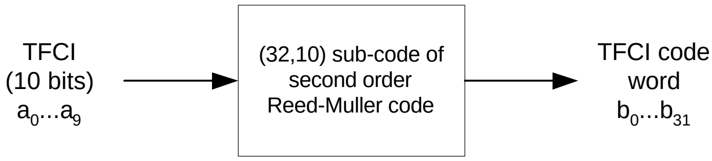


Figure 1: Channel coding of TFCI bits

If the TFCI consist of less than 10 bits, it is padded with zeros to 10 bits, by setting the most significant bits to zero. The length of the TFCI code word is 32 bits. The code words of the (32,10) sub-code of second order Reed-Muller code are linear combination of 10 basis sequences of TS 25.212 V.3.1.1. The basis sequences are listed in table 7 of TS 25.212 V.3.1.1.

In the case of non-split mode, we propose the movement of $M_{i,0}$ (All “1”) basis to the position between $M_{i,5}$ and $M_{i,6}$. If the number of TFCI bit is one, repetition is used for coding, that is, a_0 is repeated 32 times. By doing this we can maximize the minimum Hamming distance after 2 bits puncturing.

Table 1. The minimum Hamming distance in non-split mode after 2 bits puncturing

# of TFCI bits	Current	Proposed	Gain in d_{min}
1	30	30	0
2	14	16	2
3	14	16	2
4	14	16	2
5	14	15	1
6	14	14	0
7 - 10	12	12	0

2.1. Split mode

The TFCI bits are encoded using a (16, 5) bi-orthogonal (or first order Reed-Muller) code. The coding procedure is as shown in figure 2.

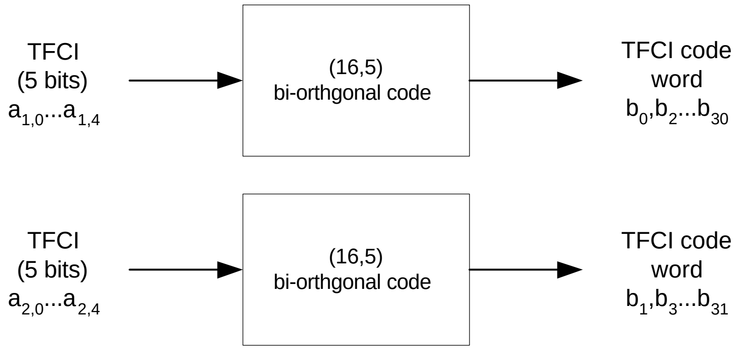


Figure 2: Channel coding of split mode TFCI bits

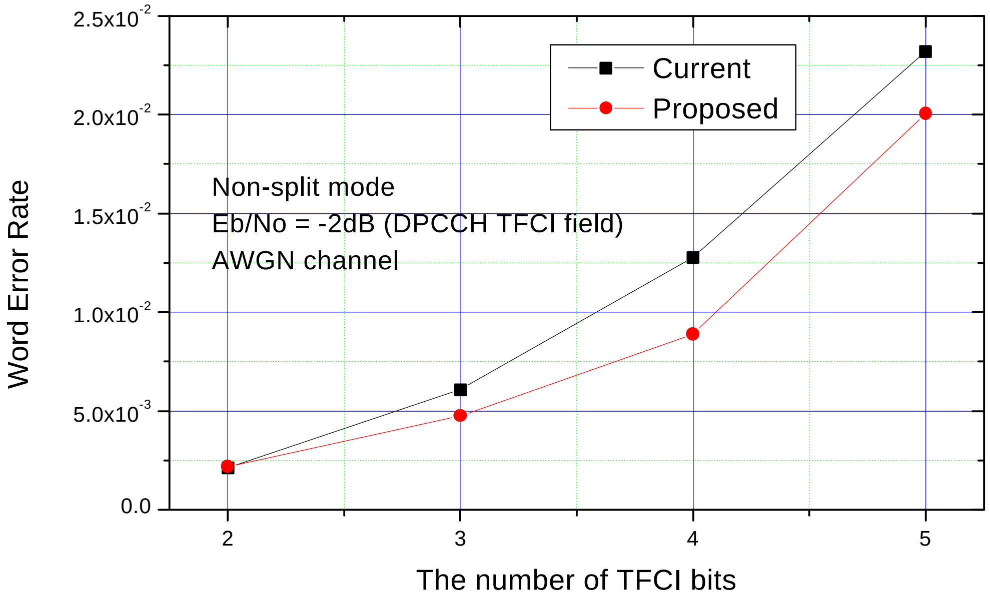
The code words of the (16,5) bi-orthogonal code are linear combinations of 5 basis sequences as defined in table 8 of TS 25.212 V3.1.1.

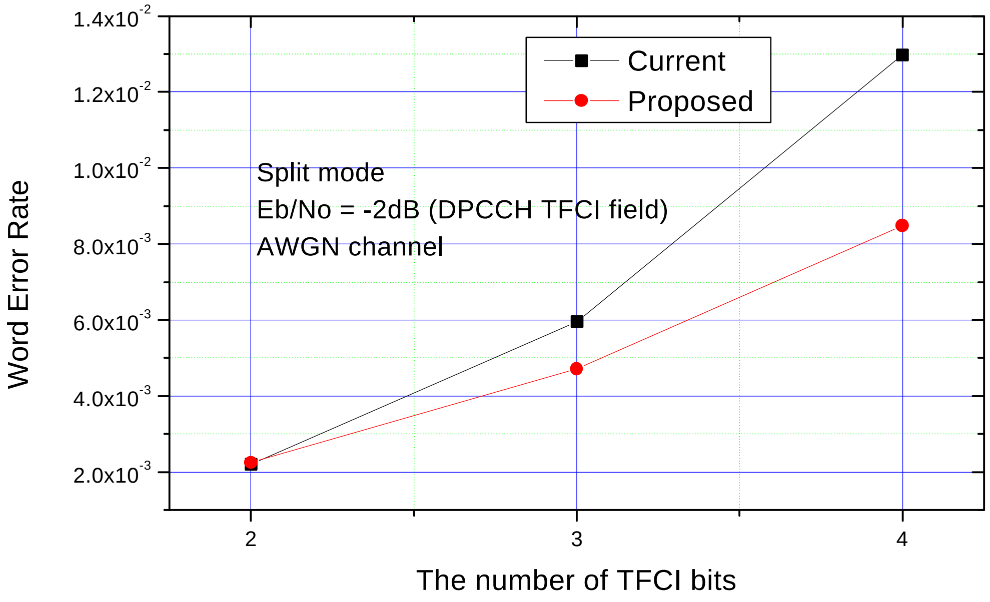
In the case of split mode, we propose the movement of $M_{i,0}$ basis to the end position after $M_{i,4}$. If the number of TFCI bit is one, repetition is used for coding, that is, $a_{1,0}$ is repeated 16 times for b_{2i} and $a_{2,0}$ is repeated 16 times for b_{2i+1}, where $i = 0,1,...,15$. By doing this we find that there will be no minimum Hamming distance loss after puncturing.

Table 2. The minimum Hamming distance in split mode after 1 bit puncturing

# of TFCI bits	Current	Proposed	Gain in d_{min}
1	15	15	0
2	7	8	1
3	7	8	1
4	7	8	1
5	7	7	0

3. Simulation results





4. Conclusion

We proposed the TFCI coding which maximizes the minimum Hamming distance and we found performance gain. The only hardware increase is bit repetition when the number of TFCS is 2. Thus, we conclude that the current TFCI coding should be replaced with the proposed one.

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e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.212 CR 047 Current Version: V3.1.1

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to: TSG RAN #7	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑	for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]
(at least one should be marked with an X)

Source: LGIC **Date:** 2000-2-29

Subject: TFCI coding for FDD

Work item:

Category:				**Release:**	
	F	Correction	X	Phase 2	
	A	Corresponds to a correction in an earlier release		Release 96	
(only one category	B	Addition of feature		Release 97	
Shall be marked	C	Functional modification of feature		Release 98	
With an X)	D	Editorial modification		Release 99	X
				Release 00	

Reason for change: The current TFCI coding is not optimized in terms of minimum Hamming distance. This contribution changes the order of TFCI basis and proposes the optimized TFCI coding in FDD, which maximizes the minimum Hamming distance.

Clauses affected: 4.3.3, 4.3.4

Other specs Affected:			
	Other 3G core specifications		→ List of CRs:
	Other GSM core specifications		→ List of CRs:
	MS test specifications		→ List of CRs:
	BSS test specifications		→ List of CRs:
	O&M specifications		→ List of CRs:

Other comments:

4.3.3 Coding of Transport-Format-Combination Indicator (TFCI)

The TFCI bits are encoded using a (32, 10) sub-code of the second order Reed-Muller code. The coding procedure is as shown in figure 10.

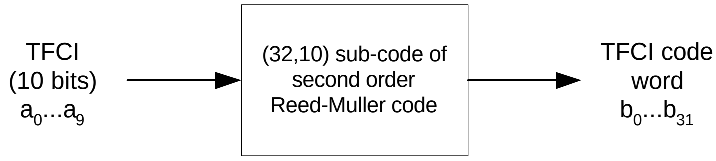

Figure 10: Channel coding of TFCI bits

If the TFCI consist of less than 10 bits, it is padded with zeros to 10 bits, by setting the most significant bits to zero. The length of the TFCI code word is 32 bits.
The code words of the (32,10) sub-code of second order Reed-Muller code are linear combination of 10 basis sequences. The basis sequences are as in the following table 7.

Table 7: Basis sequences for (32,10) TFCI code

i	$M_{i,0}$	$M_{i,1}$	$M_{i,2}$	$M_{i,3}$	$M_{i,4}$	$M_{i,5}$	$M_{i,6}$	$M_{i,7}$	$M_{i,8}$	$M_{i,9}$
0	1~~1~~	0~~1~~	0~~0~~	0~~0~~	0~~0~~	1~~0~~	0	0	0	0
1	0~~1~~	1~~0~~	0~~1~~	0~~0~~	0~~0~~	1~~0~~	1	0	0	0
2	1~~1~~	1~~1~~	0~~1~~	0~~0~~	0~~0~~	1~~0~~	0	0	0	1
3	0~~1~~	0~~0~~	1~~0~~	0~~1~~	0~~0~~	1~~0~~	1	0	1	1
4	1~~1~~	0~~1~~	1~~0~~	0~~1~~	0~~0~~	1~~0~~	0	0	0	1
5	0~~1~~	1~~0~~	1~~1~~	0~~1~~	0~~0~~	1~~0~~	0	0	1	0
6	1~~1~~	1~~1~~	1~~1~~	0~~1~~	0~~0~~	1~~0~~	0	1	0	0
7	0~~1~~	0~~0~~	0~~0~~	1~~0~~	0~~1~~	1~~0~~	0	1	1	0
8	1~~1~~	0~~1~~	0~~0~~	1~~0~~	0~~1~~	1~~0~~	1	1	1	0
9	0~~1~~	1~~0~~	0~~1~~	1~~0~~	0~~1~~	1~~0~~	1	0	1	1
10	1~~1~~	1~~1~~	0~~1~~	1~~0~~	0~~1~~	1~~0~~	0	0	1	1
11	0~~1~~	0~~0~~	1~~0~~	1~~1~~	0~~1~~	1~~0~~	0	1	1	0
12	1~~1~~	0~~1~~	1~~0~~	1~~1~~	0~~1~~	1~~0~~	0	1	0	1
13	0~~1~~	1~~0~~	1~~1~~	1~~1~~	0~~1~~	1~~0~~	1	0	0	1
14	1~~1~~	1~~1~~	1~~1~~	1~~1~~	0~~1~~	1~~0~~	1	1	1	1
15	1~~1~~	0~~1~~	0~~0~~	0~~0~~	1~~0~~	1~~1~~	1	1	0	0
16	0~~1~~	1~~0~~	0~~1~~	0~~0~~	1~~0~~	1~~1~~	1	1	0	1
17	1~~1~~	1~~1~~	0~~1~~	0~~0~~	1~~0~~	1~~1~~	1	0	1	0
18	0~~1~~	0~~0~~	1~~0~~	0~~1~~	1~~0~~	1~~1~~	0	1	1	1
19	1~~1~~	0~~1~~	1~~0~~	0~~1~~	1~~0~~	1~~1~~	0	1	0	1
20	0~~1~~	1~~0~~	1~~1~~	0~~1~~	1~~0~~	1~~1~~	0	0	1	1
21	1~~1~~	1~~1~~	1~~1~~	0~~1~~	1~~0~~	1~~1~~	0	1	1	1
22	0~~1~~	0~~0~~	0~~0~~	1~~0~~	1~~1~~	1~~1~~	0	1	0	0
23	1~~1~~	0~~1~~	0~~0~~	1~~0~~	1~~1~~	1~~1~~	1	1	0	1
24	0~~1~~	1~~0~~	0~~1~~	1~~0~~	1~~1~~	1~~1~~	1	0	1	0
25	1~~1~~	1~~1~~	0~~1~~	1~~0~~	1~~1~~	1~~1~~	1	0	0	1
26	0~~1~~	0~~0~~	1~~0~~	1~~1~~	1~~1~~	1~~1~~	0	0	1	0
27	1~~1~~	0~~1~~	1~~0~~	1~~1~~	1~~1~~	1~~1~~	1	1	0	0
28	0~~1~~	1~~0~~	1~~1~~	1~~1~~	1~~1~~	1~~1~~	1	1	1	0
29	1~~1~~	1~~1~~	1~~1~~	1~~1~~	1~~1~~	1~~1~~	1	1	1	1
30	0~~1~~	0~~0~~	0~~0~~	0~~0~~	0~~0~~	1~~0~~	0	0	0	0
31	0~~1~~	0~~0~~	0~~0~~	0~~0~~	1~~0~~	1~~1~~	1	0	0	0

For TFCI information bits a_0 , a_1 , a_2 , a_3 , a_4 , a_5 , a_6 , a_7 , a_8 , a_9 (a_0 is LSB and a_9 is MSB), the output code word bits b_i are given by:

$$b_i = \sum_{n=0}^{9} (a_n \times M_{i,n}) \bmod 2$$

where i=0…31.
If the TFCI consist of 1 bit, repetition is used for coding, that is, a_0 is repeated 32 times.
The output bits are denoted by b_k, $k = 0, 1, 2, \ldots, 31$.
In downlink, when the SF <128 the encoded TFCI code words are repeated yielding 8 encoded TFCI bits per slot in normal mode and 16 encoded TFCI bits per slot in compressed mode. Mapping of repeated bits to slots is explained in section 4.3.5.

4.3.4 Operation of Transport-Format-Combination Indicator (TFCI) in Split Mode

In the case of DCH in Split Mode, the UTRAN shall operate with as follows:

- If one of the links is associated with a DSCH, the TFCI code word may be split in such a way that the code word relevant for TFCI activity indication is not transmitted from every cell. The use of such a functionality shall be indicated by higher layer signalling.

The TFCI bits are encoded using a (16, 5) bi-orthogonal (or first order Reed-Muller) code. The coding procedure is as shown in figure 11.

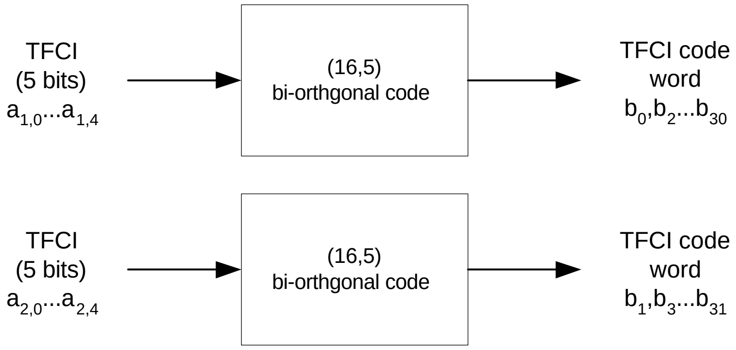

Figure 11: Channel coding of split mode TFCI bits

The code words of the (16,5) bi-orthogonal code are linear combinations of 5 basis sequences as defined in table 8 below.

Table 8: Basis sequences for (16,5) TFCI code

i	$M_{i,0}$	$M_{i,1}$	$M_{i,2}$	$M_{i,3}$	$M_{i,4}$
0	1~~1~~	0~~1~~	0~~0~~	0~~0~~	1~~0~~
1	0~~1~~	1~~0~~	0~~1~~	0~~0~~	1~~0~~
2	1~~1~~	1~~1~~	0~~1~~	0~~0~~	1~~0~~
3	0~~1~~	0~~0~~	1~~0~~	0~~1~~	1~~0~~
4	1~~1~~	0~~1~~	1~~0~~	0~~1~~	1~~0~~
5	0~~1~~	1~~0~~	1~~1~~	0~~1~~	1~~0~~
6	1~~1~~	1~~1~~	1~~1~~	0~~1~~	1~~0~~
7	0~~1~~	0~~0~~	0~~0~~	1~~0~~	1~~1~~
8	1~~1~~	0~~1~~	0~~0~~	1~~0~~	1~~1~~
9	0~~1~~	1~~0~~	0~~1~~	1~~0~~	1~~1~~
10	1~~1~~	1~~1~~	0~~1~~	1~~0~~	1~~1~~
11	0~~1~~	0~~0~~	1~~0~~	1~~1~~	1~~1~~
12	1~~1~~	0~~1~~	1~~0~~	1~~1~~	1~~1~~
13	0~~1~~	1~~0~~	1~~1~~	1~~1~~	1~~1~~
14	1~~1~~	1~~1~~	1~~1~~	1~~1~~	1~~1~~
15	0~~1~~	0~~0~~	0~~0~~	0~~0~~	1~~0~~

For TFCI information bits for DCH $a_{1,0}$, $a_{1,1}$, $a_{1,2}$, $a_{1,3}$, $a_{1,4}$ ($a_{1,0}$ is LSB and $a_{1,4}$ is MSB) and for DSCH $a_{2,0}$, $a_{2,1}$, $a_{2,2}$, $a_{2,3}$, $a_{2,4}$ ($a_{2,0}$ is LSB and $a_{2,4}$ is MSB), the output code word bits b_0, b_1, ..., b_{31}, are given by:

$$b_{2i} = \sum_{n=0}^{4} (a_{1,n} \times M_{i,n}) \bmod 2 ; \qquad b_{2i+1} = \sum_{n=0}^{4} (a_{2,n} \times M_{i,n}) \bmod 2$$

where i=0…15, j=0,1.
The output bits are denoted by b_k, k = 0, 1, 2, …, 31.
If the TFCI consist of 1 bit, repetition is used for coding, that is, $a_{1,0}$ is repeated 16 times for b_{2i} and $a_{2,0}$ is repeated 16 times for b_{2i+1}.