**3GPP TSG RAN WG1 Meeting #104-e R1-21XXXXX**

**e-Meeting, January 25th – February 5th, 2020**

**Source: Moderator (Lenovo)**

**Title: Feature lead summary #1 on multi-cell scheduling via a single DCI**

**Agenda item:** **8.13.2**

**Document for:** **Discussion and Decision**

# Introduction

This document summarizes the contributions submitted under the “**Multi-cell PDSCH scheduling via a single DCI**” agenda item of the Rel-17 work item on “Dynamic spectrum sharing (DSS)”.

The revised DSS WID [1] contains the following objective related to this agenda item:

|  |
| --- |
| This work item is limited to FR1, and includes the following objectives for NR Dynamic Spectrum Sharing (DSS):   * PDCCH enhancements for cross-carrier scheduling including [RAN1, RAN2]   + PDCCH of SCell scheduling PDSCH or PUSCH on P(S)Cell   + Study, and if agreed specify PDCCH of P(S)Cell/SCell scheduling PDSCH on multiple cells using a single DCI     - The number of cells can be scheduled at once is limited to 2     - The increase in DCI size should be minimized * Note: The total PDCCH blind decoding budget should not be changed as a result of this work * Note: These enhancements are not specific to DSS and are generally applicable to cross-carrier scheduling in carrier aggregation |

In Section 2, for multi-cell PDSCH scheduling, evaluation assumptions and evaluation results are summarized. Companies’ views on whether to support this feature are also summarized at the end of Section 2. Based on majority companies’ views, some proposals are listed for discussion purpose.

In Section 3, the standard impacts on DCI format design and HARQ-ACK codebook determination are summarized. Since the main task at this stage is to determine whether to support the feature of using a single DCI scheduling two PDSCHs on two carriers, the standard impact issues can be discussed as soon as RAN1 agrees to support this feature.

In Section 4, miscellaneous issues are listed which can be treated in low priority.

In Section 6, the agreements made in previous RAN1 meetings are listed for reference.

# Summary of contributions

The section summarises key proposals and observations from submitted contributions.

## Simulation assumptions

Agreements:

Further study with below simulation assumptions:

Simulation scenarios:

* For two-cell scheduling via a single DCI, PDCCH transmitted on a first cell schedules one PDSCH on the first cell and another PDSCH on a second cell.
* For single-cell scheduling (baseline), one PDCCH transmitted on a first cell schedules one PDSCH on the first cell via self-scheduling and another PDCCH transmitted on the first cell schedules another PDSCH on a second cell via cross-carrier scheduling.
  + Companies can optionally compare to the case of PDCCH transmitted on each of the two cells via self-scheduling. In this case, company should provide details on how to calculate the PDCCH blocking rate.

Simulation assumptions on carrier frequency, SCS, antenna configuration, carrier bandwidth as well as CORESET configuration

* Combination 1: 2 GHz, 15 kHz SCS, 2 Tx, 2 Rx, 20 MHz carrier BW, 2-symbol CORESET with 96RBs
* Combination 2: 4 GHz, 30 kHz SCS, 4 Tx, 4 Rx, 100 MHz carrier BW, 1-symbol CORESET with 270RBs
* [Combination 3: 700MHz, 15 kHz SCS, 2 Tx, 2 Rx, 10 MHz carrier BW, 3-symbol CORESET with 48RBs]
* [Combination 4: 4GHz, 30 kHz SCS, 4 Tx, 4 Rx, 40 MHz carrier BW, 2-symbol CORESET with 96RBs]

Payload size of two-cell scheduling DCI (excluding CRC):

* 60 for single-cell scheduling DCI (baseline).
* 72/84/96/108 for two-cell scheduling DCI.
* Companies are encouraged to report how the values are obtained, e.g., via separate or shared fields in DCI format.

Target BLER for two-cell scheduling DCI: 1% (baseline), 0.5%(optional)

* ~~Option 1: 1%.~~
* ~~Supported by OPPO, vivo, Nokia, Qualcomm, CATT, Ericsson, Huawei, Lenovo, Intel, MediaTek~~
* ~~Option 2: 0.5%.~~
* ~~Supported by Samsung, LG~~

Regarding the CCE-to-REG mapping, based on the agreed interleaved CCE-to-REG mapping, whether to adopt non-interleaved CCE-to-REG mapping is up to the proponent.

Agreements:

* Further study with below simulation assumptions:

Table 2: System level simulation assumptions

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Carrier frequency | For scheduling cell, follow agreed link level simulation assumptions  For scheduled cell, consider 700MHz/2GHz with 10/20MHz BW (LTE overhead on DSS carrier can be optionally provided, up to proponent) |
| SCS |
| Simulation bandwidth |
| BS antenna height | 25 m |
| UE height | 1.5m |
| TRP transmit power | 46 dBm for 10MHz |
| Scenario | Urban Macro |
| ISD | 500m |
| TRP antenna configuration | (M,N,P,Mg,Ng;Mp,Np)= (1,2,2,1,1;1,1) for 700MHz  (M,N,P,Mg,Ng;Mp,Np)= (2,8,2,1,1;1,1) for 2GHz  (M,N,P,Mg,Ng;Mp,Np)= (8,4,2,1,1;1,1) for 4GHz |
| UE antenna configuration | (M,N,P,Mg,Ng;Mp,Np)= (1,1,2,1,1;1,1) for 700MHz/2GHz  (M,N,P,Mg,Ng;Mp,Np)= (1,2,2,1,1;1,1) for 4GHz |
| Device deployment | 80% indoor, 20% outdoor |
| UE speeds of interest | Indoor users: 3km/h |
| Outdoor users (in-car): 30 km/h |
| BS noise figure | 5 dB |
| BS antenna element gain | 8 dBi |
| UE noise figure | 9 dB |
| Thermal noise level | -174 dBm/Hz |
| Traffic | Full Buffer(baseline), FTP model 1 or 3 up to company |
| Macro sites | 19 |
| Number of UEs per cell | 10/15/20 UEs |
| Downtilt | 102° |
| Minimum BS to UE distance | 35m |

## Simulation results

Based on agreed simulation assumptions, total 13 companies provide simulation results in terms of CCE saving, PDCCH blocking probability and PDSCH throughput.

### CCE saving and PDCCH blocking probability

Since NR transmission can’t use REs occupied by LTE CRS and LTE PDCCH region on a carrier shared with LTE, NR PDCCH capacity on this shared carrier is limited especially when this shared carrier is configured as PCell for NR. The insufficient NR PDCCH capacity on the NR PCell will lead to system performance degradation especially when more NR devices are camped on the NR PCell.

Supporting cross-carrier scheduling from NR SCell to NR PCell results in requiring additional PDCCH capacity of the scheduling SCell due to the need for self-scheduling on the SCell as well cross-carrier scheduling on the (shared carrier) PCell. Thus, the PDCCH capacity on the SCell may be a potential issue when a large number of UEs are configured on the SCell or the SCell is not configured with a large enough bandwidth. This issue may be addressed by allowing a single DCI on one carrier to schedule PDSCHs on two carriers. In detail, two PDSCHs on two carriers are scheduled by a single DCI format, which may save PDCCH scheduling overhead compared to scheduling two PDSCHs on two carriers by two DCI formats. Since the number of required PDCCHs is reduced, many companies observe the PDCCH blocking probability is reduced. However, the evaluations did not consider an increase in the blocking probability if the single DCI format is also used to schedule a single PDSCH reception with an obviously smaller payload compared to the PDCCH for 2-cell scheduling, or if the size of UL DCI format is smaller and needs to be padded in order to maintain the “3+1” budget for DCI format sizes. Further, the evaluations did not consider use of multiple CORESETs on the scheduling cell in a slot which reduce PDCCH blocking probability. Also, most evaluations assumed that at least 5 CA UEs are to be scheduled in every slot on sub-GHz carriers.

On the other hand, in inter-band CA, the payload size of the single DCI increases significantly when it schedules two PDSCHs on two carriers due to different channel conditions. Some companies think it may increase PDCCH blocking rate since a high AL is needed for this DCI. For intra-band CA, some companies think the payload size of the single DCI does not increase significantly by sharing many fields of the DCI.

Regarding PDCCH blocking probability, companies’ views are summarized as below:

|  |  |
| --- | --- |
| Company | Key Proposals/Observations |
| ZTE | Observation 1: For inter-band CA case,   In case of 700M and 4G, the average gain of PDCCH blocking rate for DCI size 72 bits, 84 bits 96 bits and 108 bits of the one-to-two scheduling DCI is about 5.7%, 4.0%, 1.4% and 0.6%, respectively.   In case of 700M and 2G, the average gain of PDCCH blocking rate for DCI size 72 bits, 84 bits 96 bits and 108 bits of the one-to-two scheduling DCI is about 11.1%, 9.3%, 6.1% and 4.8%, respectively.  Observation 3: For intra-band (2GHz) CA case, the average gain of PDCCH blocking rate for DCI size 72 bits, 84 bits, 96 bits and 108 bits of the one-to-two scheduling DCI is about 9.5%, 7.5%, 5.6% and 4.6%, respectively. |
| OPPO | Observation 1: CCE saving ratio is more than 10% for any DCI size even CA ratio is not large, e.g. CA ratio=30%. And for different combination scenarios, there is no significant difference in CCE saving ratio.  Observation 2: One-to-two scheduling can reduce PDCCH blockage significantly. |
| Huawei, HiSilicon | Observation 1: From link level evaluations, for one PDCCH scheduling PDSCH(s) on two cells, with respect to different PDCCH payloads in the range of 108~72 bits, significant number of CCEs can be saved for all evaluated scenarios   * 27.74%~42.95% average CCE saving ratio for Combination 1 * 23.53%~45.02% average CCE saving ratio for Combination 2 * 21.53%~41.89% average CCE saving ratio for Combination 3 * 21.3%~43.29% average CCE saving ratio for Combination 4   Observation 2: Single DCI scheduling PDSCH(s) on two cells can reduce the PDCCH blocking probability obviously. |
| CATT | Based on the results in Figure 1 – Figure 4 and Table 5 – Table 8, we can have the following observations:   * Multi-cell scheduling via a single DCI can significantly increase the PDCCH capacity. In the other words, possibility of PDCCH blocking is reduced remarkably.   + The benefits harvested from DSS-DCI in terms of PDCCH capacity increases as the ratio of DSS-UE goes up * The benefits harvested from DSS-DCI in terms of PDCCH capacity is impacted on the DCI design, i.e. the smaller size the DSS-DCI has, the more significant benefit can be got.   + Even the size of the DSS-DCI is doubled compared to the legacy-DCI, PDCCH capacity can still be enhanced. The improvement comes from:     - The 24 bits CRC can be saved.     - Even the payload is doubled, the requirement on large aggregation level such as 8 and 16 still keeps a low level. |
| vivo | Observation 1. Compared with using single-cell-DCI, a joint-DCI scheduling two PDSCHs on two cells brings more than  - 33.09% CCE saving for combination 1,  - 28.13% CCE saving for combination 2,  - 32.59% CCE saving for combination 3,  - 18.14% CCE saving for combination 4,  and the CCE saving gain becomes more significant if the compression rate of joint-DCI size increases.  Observation 2. With the same CORESET bandwidth, a joint-DCI with size (excluding CRC) =108 bits brings around  - 8.22%~8.84% reduction in PDCCH blocking rate for combination1,  - 5.2%~8.05% reduction in PDCCH blocking rate for combination2,  - 6.49%~9.07% reduction in PDCCH blocking rate for combination3,  - 2.37%~5.66% reduction in PDCCH blocking rate for combination4  compared with using single-cell-DCI, and the reduction in PDCCH blocking rate becomes more significant if the joint-DCI size decreases.  Proposal 1. The design of joint-DCI should achieve a good trade-off between system capacity improvement due to CCE saving/PDCCH blocking rate reduction and the spectrum efficiency loss due to the coarser scheduling granularity and degraded scheduling flexibility. |
| Lenovo, Motorola Mobility | Observation 1: The payload size of a single DCI scheduling two PDSCHs on two carriers can be in a range of 80~110 and further reduced if some fields are configured with less bits.  Observation 2: Compared to a single DCI scheduling a single PDSCH, the payload size of a single DCI scheduling two PDSCHs on two carriers needs to be increased about 21~54%.  Observation 3: Compared to two DCIs scheduling two PDSCHs, the payload size of a single DCI scheduling two PDSCHs on two carriers can save 23% ~ 39% overhead.  Observation 4: Two-cell scheduling DCI has lower PDCCH blocking rate compared with using two single-cell scheduling DCIs. |
| Intel | Observation 2: Based on the required SINR values and geometry curves obtained by LLS and SLS   * The ratio of CCE saving is about 20~40%; * The reduced PDCCH blocking ratio is observed. |
| Samsung | Observation 7: For a DCI format scheduling two PDSCH receptions where only fields not affecting scheduling are not duplicated, the blocking probability is larger than for one DCI format scheduling one PDSCH reception. |
| Nokia, NSB | Observation 5:  The Average PDCCH Blocking probabilities for interleaved and non-interleaved cases are presented in Figure 4 and Figure 5. From these figures we can make the following observations:   1. As the number of users are increasing it is evident that the blocking probability is also increasing. 2. In Interleaved case for DCI size 60/72/84/96 bits the blocking probability curves are very similar while for Non-Interleaved case the differences are slightly larger. 3. For DCI size 108, the blocking probability is slightly higher in case of Non-Interleaved vs Interleaved. 4. As observed in the figures, the blocking probability increases with the number of users, the blocking probability for scheduling X DCIs with 108 bit Multi-DCI scheduling will be significantly lower than the blocking probability for 2\*X DCIs with 60 bit DCI, regardless of Interleaved or non-interleaved mapping. 5. For the given scenario of 2GHz, only two DCIs can be supported per PDCCH with below 1% blocking probability for any DCI size. |
| InterDigital | Observation 1: Supporting a single PDCCH scheduling multiple cells enables efficient spectrum sharing and reduces the downlink control channel overhead on the shared spectrum.  Observation 2: PDCCH blocking probability and CCE utilization can be reduced by using a single DCI scheduling PDSCH on two cells. |
| Qualcomm | Observation 1: The overhead saving gain from multi-cell PDSCH scheduling compared to single-cell PDSCH scheduling in inter-band CA for DSS scenario is mainly comes from the omission of 24-bit CRC. In intra-band CA scenario, higher gain would be achievable by compressing some DCI fields.  Observation 2: The PDCCH blocking probability improvement from multi-cell PDSCH scheduling compared to single-cell PDSCH scheduling highly depends on whether the DCI size can be compressed aggressively. |
| Ericsson | Observation 3   * For scenario 1 (i.e., 20MHz carrier at 2GHz used for scheduling PCell PDSCH/PUSCH on another low-band DSS carrier),   + in slots where PDSCH is scheduled on both cell1 and cell 2, mc-DCI can achieve similar blocking performance as baseline case with reduced CCE allocation. The amount of possible CCE reduction depends on loading, i.e., 8 CCEs for low load and smaller for higher loads. If CCE allocation is reduced any further, performance of mc-DCI is worse.   + Assuming 50% of slots have two-PDSCH scheduling with cell1 scheduling PDSCH on both cell1 and cell2 (optimistic assumption for scenario 1 if one of the scheduled carriers is shared with LTE), and 10 symbols available for data scheduling on scheduling cell (2 DMRS symbols), an overhead reduction of < 2.5% is expected with other optimistic assumptions that rate-matching of PDSCH around PDCCH can reclaim all the saved resources (which is unlikely when there are other DCIs in the Coreset), and that there is no performance loss due to lower flexibility when scheduling with mc-DCI. Under realistic assumptions, no gains are expected.   Observation 4   * For scenario 2 (i.e., 100MHz mid-band 4GHz carrier used for scheduling PCell PDSCH/PUSCH on a low-band DSS carrier),   + using mc-DCI is not expected to provide performance gains as the blocking performance for scheduling up to 10 UEs is close to zero even for baseline case of two legacy DCIs.   Observation 5   * Evaluations indicate that single DCI scheduling PDSCH on two cells (mc-DCI) provides marginal or no performance gains. |

### PDSCH throughput improvement

For one DCI scheduling two PDSCHs on two carriers, it is expected that CCE resources are saved compared to using two DCIs scheduling two PDSCHs. The saved CCE resources can be used for allocating more PDCCHs to further schedule more users/PDSCHs with/without multiplexing on the same PDSCH resources. Or under certain conditions, the saved CCE resources can be used for PDSCH transmission for improving PDSCH throughput. Such a condition for the latter case is that the only PDCCH transmitted in the CORESET is the one scheduling the PDSCH transmission (i.e. there is no other PDCCH for another PDSCH transmission, or for any PUSCH transmission, or for common search space that is transmitted in the CORESET). CORESET based rate matching and CCE level rate matching are specified in Rel-15.

On the other hand, if it is possible to share some of the DCI fields between two carriers without throughput loss, the PDCCH blocking probability is reduced while the scheduling flexibility may be restricted. A trade-off between the DCI payload size and the PDSCH throughput is needed.

Regarding PDSCH throughput, companies’ views are summarized as below:

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| --- | --- |
| Company | Key Proposals/Observations |
| ZTE | Observation 2:  For inter-band (700MHz + 4GHz) CA case,   * In case of 108 bits of one-to-two scheduling DCI, the throughput is similar as the baseline. * In case of 84 bits of one-to-two scheduling DCI, the throughput is reduced by 13.4% compared with the baseline.   For inter-band (700MHz + 2GHz) CA case,   * In case of 108 bits of one-to-two scheduling DCI, the throughput is similar as the baseline. * In case of 84 bits of one-to-two scheduling DCI, the throughput is reduced by 9.9% compared with the baseline.   Observation 4: For intra-band (2GHz) CA case,   * In case of 108 bits of one-to-two scheduling DCI, the throughput is similar as the baseline. * In case of 84 bits of one-to-two scheduling DCI, the throughput is reduced by 8.7% compared with the baseline. |
| Huawei, HiSilicon | Observation 3: For the two carriers of combination 1 and combination 3, the single DCI scheduling PDSCHs on two carriers can achieve  − up to 8.29% throughput gain when payload size of single DCI is 108bits  − up to 10% throughput gain when payload size of single DCI is 96bits.  Observation 4: For two carriers of combination 1 and combination 1, the single DCI scheduling PDSCHs on two carriers can achieve  − up to 8.93% throughput gain when payload size of single DCI is 108bits  − up to 10.88% throughput gain when payload size of single DCI is 96bits.  Observation 5: The throughput gain by joint scheduling increases as the LTE overhead/traffic load increases on a DSS carrier.  Observation 6: PDCCH coverage is not a concern with single DCI scheduling PDSCH(s) over two cells. |
| vivo | Observation 3. Joint-DCI requires fewer CORESET RBs to achieve the same scheduling opportunities as single-cell-DCI, thus gNB can provide a CORESET with less PRBs for joint-DCI scheduling than single-cell-DCI scheduling. These saved RBs can be reused for PDSCH to improve throughput.  Observation 4. Compared with using single-cell-DCI, joint-DCI brings around - 24~27 RB reduction in CORESET BW and <=3.24% theoretical throughput gain for combination1,  - 42~54 RB reduction in CORESET BW and <=3.32% theoretical throughput gain for combination2, - 12~16 RB reduction in CORESET BW and <=3.66% theoretical throughput gain for combination3, - 6~12 RB reduction in CORESET BW and <=4.79% theoretical throughput gain for combination4.  Observation 5. Joint-DCI with size=96bits~108 bits can bring - <=2.44% throughput gain compared with single-cell-DCI for combiantion1 in practical scenarios - <=2.32% throughput gain compared with single-cell-DCI for combiantion2 in practical scenarios - <=3.12% throughput gain compared with single-cell-DCI for combiantion3 in practical scenarios compared with single-cell-DCI.  Observation 6. When the number of UE is 10, joint-DCI with size=96bits~108 bits can bring <=1.42% throughput gain compared with single-cell-DCI for combiantion4 in practical scenarios. However, it can also bring 0.2%~0.31% throughput loss if the number of UE increases to 15/20. |
| MediaTek | Observation 1: In both full-buffer and FTP traffic, a UE with 2-cell CA is not always scheduled with PDSCHs over 2 cells whenever there is data packet   * Full-buffer traffic (2GHz)   + 1 scheduled cell: 70% of slots   + 2 scheduled cells: 30% of slots * FTP traffic with a packet size of 20Kbytes (2GHz)   + 1 scheduled cell: 30% of slots   + 2 scheduled cell: 70% of slots   Observation 2: Compared to legacy scheme, scheme #1/2/3 provide non-negligible UE throughput gain in both full-buffer and FTP traffic  Observation 3: For FTP traffic, the mean/cell-edge UE throughput gain for 700MHz is larger than that for 2GHz due to larger RU reduction resulted from CORESET overhead reduction  Observation 4: DCI aggregation for cross-carrier scheduling provides higher cell-edge UE throughput gain than mean UE throughput gain  Observation 5: Compared to scheme #1/2 (i.e. 1-stage DCI aggregation), scheme #3 (i.e. 2-stage DCI aggregation) provides larger mean and cell-edge UE throughput gain for 700MHz |
| Samsung | Observation 1: The maximum throughput gain for Combination 1 is 1.07%.  Observation 2: The maximum throughput gain for Combination 2 is 0.084%.  Observation 3: The scenario for Combination 3 is atypical and problematic and does not affect conclusions for use of a DCI format scheduling PDSCH receptions on two cells.  Observation 4: For a DCI format scheduling PDSCH receptions on two cells (DCI format X):   1. Residual resources in a CORESET cannot be used for PDSCH if the PDCCH is not the only one in the CORESET. 2. Overhead increase occurs as either DCI format 0\_1 needs to be size-matched with DCI format 1\_1, or DCI format X needs to also be used for scheduling PDSCH reception on only one cell.   Observation 5: Joint applicability on two cells for a field serving to maximize throughput per cell would result in throughput loss that is at least an order of magnitude larger than any gain from saving a few bits in the DCI format.  Observation 6: Contiguous spectrum below 2 GHz is typically limited to less than 20 MHz and there is no need to divide that spectrum among multiple cells. |

### UE blind detection reduction and power saving

Using a single DCI format scheduling two PDSCHs on two carriers can save UE’s power consumption since UE needs to monitor the DCI in the search space of only one carrier where the DCI format is transmitted. This is especially true when the scheduling cell is configured with small bandwidth and the scheduled cell has ultra-wide carrier.

Regarding UE power saving, companies’ views are summarized as below:

|  |  |
| --- | --- |
| Company | Key Proposals/Observations |
| Huawei, HiSilicon | Observation 10: A single PDCCH scheduling PDSCH over two cells can save up to 6.67%~15% power consumption comparing with two separate PDCCHs for scheduling.  Observation 11: Using single DCI scheduling multi-carriers can achieve more gain for the scenario that multi-TRP and/or mini-slot based CORESET is configured on the scheduled cell. |
| Lenovo, Motorola Mobility | Observation 5: Using single DCI scheduling two PDSCHs on two carriers can save UE’s power consumption. |
| Nokia, NSB | Observation 2: Two-cell DCI format may reduce UEs monitoring burden as UE needs to monitor search-space set(s) of only single scheduling cell compared to R16, given that design is based on DCI format 1\_1. |

### Whether to support multi-cell PDSCH scheduling by single DCI?

Regarding whether to support multi-cell PDSCH scheduling by a single DCI, companies’ views are summarized in below table.

**Company views:**

|  |  |
| --- | --- |
| **Company** | **Key Proposals/Observations** |
| ZTE | Observation 11: For both inter-band CA and intra-band CA scenario,   * If most of the fields are separately indicated for one-to-two scheduling DCI, the gain of PDCCH blocking rate is marginal. * If most of the fields are shared for one-to-two scheduling DCI, throughput performance loss is observed.   Observation 12: SCell-schedule-PCell in DSS WI and multi-PDSCH scheduling with one single DCI in 52.6GHz-71GHz WI can effectively resolve the PDCCH capacity issue on PCell i.e. usually a shared carrier in DSS scenario, which is the major issue to be addressed in this WI.  Proposal 1: RAN1 further discusses the necessity, potential gain, open issues and possibility of timely completion of single DCI scheduling two PDSCHs on two carriers. |
| OPPO | Proposal 1: Considering performance from CCE saving ratio and PDCCH blockage reduction, One-to-two scheduling should be supported. |
| CATT | Proposal 1: Multi-cell PDSCH scheduling via a single DCI should be supported considering it can bring significant benefits in terms of PDCCH capacity, PDSCH throughput and network flexibility. |
| LG | Proposal #1: It is necessary to clarify/justify first on the technical motivation and benefits by introducing the single DCI based multi-cell PDSCH scheduling, on top of specifying the cross-CC PDSCH/PUSCH scheduling from Scell to Pcell. |
| ASUSTeK | Proposal 1: NR DSS supports PDCCH scheduling PDSCHs on two cells using a single DCI |
| Samsung | Proposal: A DCI format that schedules PDSCH receptions on two cells is not introduced. |
| Apple | Proposal 1: We do not observe enough justification and motivation to allow single DCI to schedule PDSCH on multiple cells. |
| Lenovo, Motorola Mobility | Proposal 1: Support using a single DCI to schedule two PDSCHs on two cells.  Proposal 2: Further study payload size reduction for the two-cell scheduling DCI. |
| MediaTek | Proposal 1: Conclude in RAN1 that multi-cell PDSCH scheduling via single DCI provides significant system benefits in terms of UE throughput, UE PDCCH blind decoding complexity and UE power consumption for PDCCH blind decoding.  Proposal 2: Continue to work on detailed design of multi-cell PDSCH scheduling via single DCI with the following design considerations.   * PDCCH blind decoding complexity is not worse than Rel-16 * Scalable DCI size based on the number of scheduled cells * Switch of same/different TDRA/FDRA across the scheduled cells * Forward compatibility to CA with more than 2 cells |
| Nokia, NSB | Proposal 1: Support multi-cell DCI in R17, focus on multiple SCell (2 or more) with the same/similar carrier size and SCS first. |
| InterDigital | Proposal 1: Support a single DCI to schedule two PDSCH in different cells. |
| Qualcomm | Proposal: Conclude not to support multi-cell PDSCH scheduling via a single DCI as part of Rel.17 DSS work item. It can be discussed in future potential work items. |
| NTT DOCOMO | Proposal 1:   * The following both scheduling options should be supported if multi-cell PDSCH scheduling via single DCI is supported.   + Option.1: cross-carrier and self-carrier scheduling PDSCHs via a single DCI   + Option.2: only cross-carrier scheduling PDSCHs via a single DCI |
| Apple | Not to support single DCI to schedule two PDSCH in different cells |

### Summary of observations

For this agenda, total 18 contributions are submitted, and 13 contributions provide simulation results. Basically, there are three metrics evaluated according to the agreed simulation assumptions, CCE saving, PDCCH blocking probability and PDSCH throughput.

On CCE saving by using a single DCI to schedule multiple PDSCHs on multiple carriers, simulation results are summarized below:

* 7 companies [OPPO, Huawei, HiSilicon, Intel, InterDigital, vivo, MediaTek, CATT] observe reduced CCE consumptions via simulation.
  + OPPO: CCE saving ratio is more than 10% for any DCI size even CA ratio is not large.
  + Huawei, HiSilicon: for DCI size in range of 108~72 bits,
    - 27.74%~42.95% average CCE saving ratio for Combination 1
    - 23.53%~45.02% average CCE saving ratio for Combination 2
    - 21.53%~41.89% average CCE saving ratio for Combination 3
    - 21.3%~43.29% average CCE saving ratio for Combination 4
  + Intel: The ratio of CCE saving is about 20~40%.
  + Vivo: joint-DCI scheduling brings more than
    - 33.09% CCE saving for combination 1,
    - 28.13% CCE saving for combination 2,
    - 32.59% CCE saving for combination 3,
    - 18.14% CCE saving for combination 4,
  + MediaTek: for Combination 1, saving rate is 21.3% for 84 bits DCI, 20.6% for 96 bits DCI.
  + CATT: for a DSS-DCI with payload size 60 bits – 108 bits,
    - 28% - 45% average CCE saving ratio for combination 1
    - 22.5%- 45% average CCE saving ratio for combination 2
    - 26.4% - 41.7% average CCE saving ratio for combination 3
    - 21.1% - 42.1% average CCE saving ratio for combination 4

On PDCCH blocking probability using a single DCI to schedule multiple PDSCHs on multiple carriers, simulation results are summarized below:

* 12 companies [OPPO, Huawei, HiSilicon, Intel, InterDigital, CATT, vivo, Nokia, NSB, Lenovo, Motorola Mobility, Qualcomm] observe decreased PDCCH blocking probability via simulation.
* 2 companies [ZTE, Ericsson] observed marginal performance gain in PDCCH blocking.
* 1 company [Samsung] observe higher PDCCH blocking compared to two DCIs scheduling two PDSCHs.

On PDSCH throughput, simulation results are summarized below:

* 4 companies [Huawei, HiSilicon, vivo, MediaTek] observe non-negligible PDSCH throughput gain via simulation.
  + Huawei, HiSilicon: 8~10% throughput gain for 108bits DCI or 96bits DCI.
  + Vivo: 2.32~3.12% throughput gain for 96bits DCI or 108bits DCI for combination 1/2/3, 1.42% throughput gain for combination4, but if the number of UE increases to 15 or 20, using single DCI to schedule multiple PDSCH may bring 0.2%~0.31% throughput loss for combination4 as the loss caused by increased scheduling granularity cannot be compensated by throughput gain brought by the saved PDCCH resources.
  + MediaTek: For 96bits DCI, 16.7%/32.7% mean/cell-edge UE throughput gain for 2GHz and 29~34%/63~100% mean/cell-edge UE throughput gain for 700MHz.
* 1 company [Samsung] observe marginal throughput gain 1.07% for Combination 1 and 0.084% for Combination 2 for 108bits DCI via estimation.
* 1 company [ZTE] observe 13.4 or 8.7% loss for inter-band case and intra-band case for 84 bits DCI via simulation.

On UE blind detection reduction and power saving, companies’ simulation results and views are summarized below:

* 6 companies [Huawei, HiSilicon, Lenovo, Motorola Mobility, Nokia, NSB] observe UE power saving by using a single DCI to schedule multiple PDSCHs on multiple carriers.
  + Huawei, HiSilicon: save up to 6.67%~15% power consumption.

Companies’ views on whether to support multi-cell scheduling via a single DCI are summarized below:

* Support (12): OPPO, CATT, Huawei, HiSilicon, ASUSTeK, Lenovo, Motorola Mobility, MediaTek, Nokia, NSB, InterDigital, DoCoMo, Intel
* FFS (2): ZTE, LG
* Not support (3): Samsung, Apple, Qualcomm, Ericsson

Regarding above summary, companies are encouraged to provide comments in the table below.

|  |  |
| --- | --- |
| **Company** | **View** |
| Intel | Based on our evaluation results on CCE saving and blocking ratio reduction, we support to introduce multi-cell scheduling. We think it is enough to support one DCI to schedule transmission on up to two cells. |
| Qualcomm | The CCE saving ratio is not necessary. It is important to observe the real gain(s) the solution offers. In this sense, the observations should be made based on PDCCH blocking probability and DL throughput.  Regarding PDCCH blocking probability, it should be clear for which scenario what amount of gain can be achieved (at least roughly). Note that the operation point of PDCCH blocking probability should be not higher than 10%, which should be taken into account for the discussion.  Regarding DL throughput, there should be a trade-off between the gain and pain; there could be an improvement through PDCCH overhead reduction while could be a degradation due to lower resource allocation granularity because of DCI field compression. From the evaluation results, three companies (Huawei, HiSilicon, MediaTek) observed substantial (8% or higher) gains while three companies (vivo, Samsung, ZTE) observed little (less than 4%) gains or degradation. This should be stated. By the way, on the MediaTek’s result, we wonder why 63~100% mean/cell-edge UE throughput gain is achievable by just reducing PDCCH overhead?  Regarding UE power saving, the gain would be achievable if the UE does not monitor a DCI format for single-cell PDSCH scheduling when the UE is configured with monitoring a DCI for multi-cell PDSCH scheduling. This condition should be captured. |
| CATT | Add our observation on CCE saving ratio from our simulation results in the above.  We share the same view with Intel. The benefits of multi-cell scheduling are obvious in several aspects.  From our understanding, the CCE saving ratio is meaningful although it may not be so practical as mentioned by Qualcomm. In theory, gNB can use each available CCE for PDCCH transmission considering the number of UEs staying in the cell is large enough. It can reflect the PDCCH capacity with exclude the bias caused by configuration and simulation. |
| ZTE | Note: Our tdoc has been updated to R1-2101789, which further includes the simulation resultsof 700MHz+2GHz CA. We have added the updated observations in Section 2.2.1 and 2.2.2 of this FL summary.  First of all, CCE saving ratio is not necessary because only parts of the saved CCE can be reused for PDCCH and PDSCH, which can already be reflected via PDCCH blocking rate and PDSCH throughput, respectively.  Regarding power saving, from our perspective, the potential gain observed by companies is from reduced BD/CCE limits. However, it is still not clear whether the BD/CCE budget can be reduced subject to further discussion.  Thus, overall, from our perspective, we should focus on **PDCCH blocking rate and PDSCH throughput**.  Regarding PDCCH blocking rate, most of companies simulated different DCI sizes. We can try to summarize and make some observations regarding the detailed results from each company. Practically, the DCI size of joint-DCI can NOT be too small. It would be more reasonable to only consider the gain of a moderate DCI size or large DCI size, e.g., 84bits, 96bits and 108bits.  Regarding PDSCH throughput, different companies use different assumptions. Some assume that we can use a smaller CORESET to scheduling PDSCH, some assume that all the unused REs in the CORESET can be reused by PDSCH, etc. If a smaller CORESET is used, it should be clear that the gain of PDCCH blocking rate is gone in this case. On the other hand, currently, the rate-matching is performed in the granularity of CORESET, it is not clear how network can reuse all the unused REs in CORESET for PDSCH throughput. We would propose to make some detailed observations on the PDSCH throughput gain taking the detailed assumptions into account.  Overall, different companies use different simulation assumptions, even different simulation methodologies, we propose to make some detailed observations taking these different assumptions and methodologies into account. |
| Samsung | The maximum throughput gain, for the best-case scenario, is about 1%. That gain will not be realized in practice because:   1. It is not always possible to use CCEs of a CORESET for PDSCH. 2. Scheduling on two cells will not happen in every slot. When scheduling is on one cell, any gains need to be scaled down by the proportion of time scheduling is on two cells. The mechanism may actually result to throughput loss (either because single-cell scheduling and dual-cell scheduling use same DCI or because single-cell DCI uses padding to keep the “3+1” DCI sizes). 3. Regardless of whether or not the scheme is extended to the UL (not in scope), a UE need not be configured/support both DL CA and UL CA. In case of single UL cell, gains from scheduling on two cells need to be further scaled down and may be negative. 4. Blocking is not an issue, especially because the number of UEs with DL CA scheduled per slot on a 5/10 MHz carrier is small (e.g. it is typically 1 UE and rarely 2 UEs). 5. There is no impact on UE power consumption. |
| Huawei | Support to capture CCE saving ratio as intermediate LLS results. It is important to understand how some gains are presented while the gain is different when considering real scheduling as Qualcomm/ZTE mentioned, thus a common understanding of ‘optimistic gain’ would be useful for future discussion.  For PDCCH blocking rate and/or DL throughput, support to capture necessary clarification as many companies mentioned, for all presented simulation results, e.g.   * For PDCCH blocking   + One source result showing marginal gain uses UE geometry very different from many others.   + One source results showing marginal gain assumes “a roughly 2x CCE AL for DCI format X” and “probability distribution to CCE ALs of [1 2 4 8 16] of [20 20 20 20 0]% for DCI format 1\_1 and [0 20 20 20 20]% for DCI format X”, which is not acquired from LLS/SLS (while should be). * For PDSCH throughput   + One source result showing marginal gain assumes that “scheduling information of SCell reuses that of PCell”, although there is much room for the DCI of joint scheduling not to share scheduling information like MCS, FDRA.   + One source result showing no gain is analysis-based without SLS simulation   We disagree with the statement that “If a smaller CORESET is used, it should be clear that the gain of PDCCH blocking rate is gone in this case” since the system gain naturally comes from (1) using a smaller CORESET that is enjoying the single-DCI joint-scheduling PDCCH with similar PDCCH blocking rate, or (2) same CORESET configuration but with reduced PDCCH blocking rate. The network shall not be mandated to use large CORESET if there is PDCCH resource saving achieved already.  We have also clarified in our results that even with CORESET level rate matching, almost the same throughput gain can be achieved. This can also be captured.  Regarding SS comments above:   1. Explained in our contribution 2. Not necessarily true. Scheduling can/will usually be FDMed and the targeting scenario is with PDCCH capacity concern. Note our simulation is based on slot based scheduling while the potential gain can be increased if with span based CORESET (i.e. more CORESETs within a slot). 3. The gain will be increased if UL CA also supports joint scheduling using single DCI. The gain can be further increased if more carriers are supported with joint scheduling. 4. Similar to b). Again, the motivation of DSS is to ensure sufficient PDCCH capacity. There will be no need to do any enhancement since LTE to NR including specifying SCell scheduling PCell, if a network always has only one CA user. |
| OPPO | Considering performance from CCE saving ratio and PDCCH blockage reduction, One-to-two scheduling should be supported. |
| MediaTek | In our SLS simulation, CCE saving rate is used to derive the applied CORESET size for enhanced scheme based on legacy CORESET size, assuming the RU rate for DL control region is the same across legacy and enhanced schemes.   * For full-buffer traffic, the main UE throughput gain comes from overhead reduction. * For FTP traffic, the main UE throughput gain comes from RU reduction for PDSCH, assuming the same traffic arrival rate, e.g. RU reduction from ~46% to ~40% for 2GHz carrier frequency and from ~53% to ~37% for 700MHz carrier frequency. * This is why we observe higher UE throughput gain in FTP traffic than in full-buffer traffic, especially for cell-edge UEs. Because cell-edge UEs are more sensitive to RU rate due to inter-cell interference. * We also observe in the SLS results that a UE is not always scheduled with PDSCHs over 2 cells (30% of slots for full buffer traffic; 70% of slots for FTP traffic).   We’re supportive to this feature because we still see certain benefits for 2-cell CA case.  We also understand that it can provide more system benefits if current scope can be extended to cover CA with more than 2 cells and DCI for PUSCH so forward compatibility needs to be considered for detailed design if we decide to go for this feature in Rel-17 DSS. |
| vivo | *Some observations in our paper were omitted, I added the omitted part in 2.2.5.*  CCE saving alone is not a reasonable metric for concluding whether joint scheduling is beneficial.  Joint scheduling is considered truly beneficial only when the savings in CCE resources and reductions in blocking rates can bring an increase in overall throughput. Therefore, we suggest to focus on the evaluation of throughput gains. |
| Ericsson | On “CCE savings” we do not support capturing observations using such intermediate metric as it does not provide useful information without proper context. For example, a saving from 2 CCEs to 1 CCE would show as 100% reduction in “CCE savings” when overall impact would be <<1%.  On observations related to PDSCH throughput, it is not clear from the proposed observations what is gain shown by each proponent for agreed Combination 1 and agreed Combination 2.  Also, considering some of the proposed observations more specifically   * “MediaTek: For 96bits DCI, 16.7%/32.7% mean/cell-edge UE throughput gain for 2GHz….”   + Considering R1-2100611, this seems to be for the case of FTP traffic where 3symbol CORESET is assumed for 20MHz channel BW (in Table 2).   + Table 1 in R1-2100611 shows Avg. CCE = 7.08 for FTP traffic (legacy scheme) and Avg. CCE = 4.36 for FTP traffic (1stage DCI 96 bits) for 3 symbol coreset. Then 3sym CORESET at 15kHz SCS and 20MHz channel BW results in 48 available CCEs, with such large available CCEs, PDCCH blocking issues are not expected, then it is unclear how a CCE reduction from 7CCEs to 4CCEs provides a overall throughput gain of 16% or 32%. We request MTK to please clarify this.   + Also, the 3 symbol coreset for 20MHz channel BW is not aligned with any of the agreed combinations. * “Vivo: 2.32~3.12% throughput gain for 96bits DCI or 108bits DCI.”   + Considering R1-2100474, observation 5 says <=2.44% throughput gain for combination 1 and <=2.32% throughput gain for combination 2. The proposed observation should be modified to reflect that these are upper limits.   + Further, according to R1-2100474 - “…*We performed SLS based on this scheduling restriction (i.e., the determined RBG size) and the overhead reduction gain (i.e., the required CORESET BW in the above Tables)….”.* We request vivo to clarify if observation 5 is based on overhead reduction being available in every slot or only in some slots?     - As discussed in our (and other) contributions there are many slots where only 1CC is scheduled and for such slots there is no gain with single DCI.   Overall, as discussed in our contribution we expect single DCI scheduling PDSCH on two cells to provide marginal or no performance gain.  [vivo-reply] In our simulation, we assumed that there are two PDSCHs to be scheduled on each slot. So observation 5 is based on the overhead reduction being available for each slot. |
| Moderator | (1) Regarding the observations on CCE saving, many companies provide simulation results on CCE saving. Although CCE saving leads to reduced PDCCH blocking probability, I think it is no harm to discuss or even capture the related observations.  (2) Regarding the detailed performance gain in term of PDCCH blocking probability, most companies show the curves and do not provide the concrete value in reduced PDCCH blocking probability. We can discuss further whether to use a template for collecting companies’ results.  (3) Regarding the PDSCH throughput, I think the current simulation results are quite diverse. We can further discuss the simulation assumptions for SLS, e.g., how to evaluate the impact on PDSCH throughput gain by configuring a smaller CORESET or reusing the available CCEs for PDSCH transmission, how to evaluate the impact on PDSCH throughput loss when the scheduling PDCCHs are dropped due to PDCCH blocking.  (4) Regarding the simulation results which I captured in the above observations, please companies check them and make update if needed. |
| Nokia, NSB | We see the core benefit of the feature in intra-band or inter-band CA with the same SCS, where multi-cell DCI can mimic a wider channel bandwidth. The benefits in DSS configuration might alone justify the additional feature.  On Samsung’s results, is it a correct understanding that the aggregation level (CCE consumption) is always 2x for the new larger DCI than the reference DCI? “**Figure 3** presents the blocking probability assuming a roughly 2x CCE AL for DCI format X and probability distribution to CCE ALs of [1 2 4 8 16] of [20 20 20 20 0]% for DCI format 1\_1 and [0 20 20 20 20]% for DCI format X” If this is true, that would explain the increase in blocking probability, but seems to be contrary to the CCE consumption evaluation earlier in the document.  We think capturing blocking probability improvement is a relevant metric, and perhaps a template for this can be used, but here it should be clear that blocking probability based on realistic AL distribution rather than a completely hypothetical one should be used. |
| MediaTek | On Ericsson’s question:  In Table 2 of R1-2100611, there are two tables for 2GHz.   * 1st table assumes 2-symbol CORESET * 2nd table assumes 3-symbol CORESET   The UE throughput gain Ericsson refers to is from the 2nd table. However, in the 1st table, the average/cell-edge UE throughput gain is 8.2/22.4% for FTP 3 traffic with packet size of 20Kbytes & 10 packets/s per UE. |

## Proposals for 1st GTW session

FL Proposal#1:

* Take above observations as conclusions

Regarding above proposal, companies are encouraged to provide comments in the table below.

|  |  |
| --- | --- |
| **Company** | **View** |
| Intel | Agree with moderator’s proposal |
| Qualcomm | Discussions on the observations are necessary |
| CATT | Majority companies observe there are significant benefits from multi-cell scheduling via single DCI from several aspects. The above observations are long text, which is not friendly for reading. Maybe we can try the following wording:  *Multi-cell scheduling via single DCI is beneficial at least for reducing CCE consumption, reducing PDCCH blocking possibility, increasing PDSCH throughput, reducing PDCCH blind detection and power consumption.* |
| Samsung | Need to discuss the various issues and draw conclusive observations. |
| Huawei | Support the approach to capture observations with necessary clarification. FL observations canbe starting point. |
| OPPO | Agree with moderator’s proposal |
| MediaTek | Support to capture concise observations based on the submitted simulation results as a starting point. |
| vivo | Please see our comments in 2.2.5. We are not sure if we need to capture all above observations in the chairman note. We suggest to draw some conclusive observations. |
| Lenovo, Motorola Mobility | Generally Ok with the conclusive observation. |
| Ericsson | More discussion and updates are needed for the proposed observations |
| DOCOMO | Support |
| LG | Same view with other companies.  Need discussions on the possible conclusive observations. |
| Nokia, NSB | In general agree with the Feature Lead proposal. We should aim at deriving observations and conclusions for RAN#91 to take the final decision on whether to proceed with the design based on RAN1 findings rather than just ending up counting companies. |

## Proposals for 2nd round of discussion

FL Proposal#1:

* Further discuss the below observations:

On CCE saving by using a single DCI to schedule multiple PDSCHs on multiple carriers, simulation results are summarized below:

* 8 companies [OPPO, Huawei, HiSilicon, Intel, InterDigital, vivo, MediaTek, CATT] observe reduced CCE consumptions via simulation.
  + OPPO: CCE saving ratio is more than 10% for any DCI size even CA ratio is not large.
  + Huawei, HiSilicon: for DCI size in range of 108~72 bits,
    - 27.74%~42.95% average CCE saving ratio for Combination 1
    - 23.53%~45.02% average CCE saving ratio for Combination 2
    - 21.53%~41.89% average CCE saving ratio for Combination 3
    - 21.3%~43.29% average CCE saving ratio for Combination 4
  + Intel: The ratio of CCE saving is about 20~40%.
  + Vivo: joint-DCI scheduling brings more than
    - 33.09% CCE saving for combination 1,
    - 28.13% CCE saving for combination 2,
    - 32.59% CCE saving for combination 3,
    - 18.14% CCE saving for combination 4,
  + MediaTek: for Combination 1, saving rate is 21.3% for 84 bits DCI, 20.6% for 96 bits DCI.
  + CATT: for a DSS-DCI with payload size 60 bits – 108 bits,
    - 28% - 45% average CCE saving ratio for combination 1
    - 22.5%- 45% average CCE saving ratio for combination 2
    - 26.4% - 41.7% average CCE saving ratio for combination 3
    - 21.1% - 42.1% average CCE saving ratio for combination 4

On PDCCH blocking probability using a single DCI to schedule multiple PDSCHs on multiple carriers, simulation results are summarized below:

* 12 companies [OPPO, Huawei, HiSilicon, Intel, InterDigital, CATT, vivo, Nokia, NSB, Lenovo, Motorola Mobility, Qualcomm] observe decreased PDCCH blocking probability via simulation.
* 2 companies [ZTE, Ericsson] observed marginal performance gain in PDCCH blocking.
* 1 company [Samsung] observe higher PDCCH blocking compared to two DCIs scheduling two PDSCHs.

On PDSCH throughput, simulation results are summarized below:

* 4 companies [Huawei, HiSilicon, vivo, MediaTek] observe non-negligible PDSCH throughput gain via simulation.
  + Huawei, HiSilicon: 8~10% throughput gain for 108bits DCI or 96bits DCI.
  + Vivo: 2.32~3.12% throughput gain for 96bits DCI or 108bits DCI for combination 1/2/3, 1.42% throughput gain for combination4, but if the number of UE increases to 15 or 20, using single DCI to schedule multiple PDSCH may bring 0.2%~0.31% throughput loss for combination4 as the loss caused by increased scheduling granularity cannot be compensated by throughput gain brought by the saved PDCCH resources.
  + MediaTek: For 96bits DCI, 16.7%/32.7% mean/cell-edge UE throughput gain for 2GHz and 29~34%/63~100% mean/cell-edge UE throughput gain for 700MHz. In the 1st table, the average/cell-edge UE throughput gain is 8.2/22.4% for FTP 3 traffic with packet size of 20Kbytes & 10 packets/s per UE.
    - There are two tables for 2GHz: 1st table assumes 2-symbol CORESET and 2nd table assumes 3-symbol CORESET. The UE throughput gain Ericsson refers to is from the 2nd table.
* 1 company [Samsung] observe marginal throughput gain 1.07% for Combination 1 and 0.084% for Combination 2 for 108bits DCI via estimation.
* 1 company [ZTE] observe 13.4 or 8.7% loss for inter-band case and intra-band case for 84 bits DCI via simulation.

On UE blind detection reduction and power saving, companies’ simulation results and views are summarized below:

* 6 companies [Huawei, HiSilicon, Lenovo, Motorola Mobility, Nokia, NSB] observe UE power saving by using a single DCI to schedule multiple PDSCHs on multiple carriers.
  + Huawei, HiSilicon: save up to 6.67%~15% power consumption.

Regarding above observations, companies are encouraged to provide comments in the table below.

|  |  |
| --- | --- |
| **Company** | **View** |
| ZTE | Thank you for the proposal.  Firstly, as commented by many other companies online, the CCE consumption is not a desired metric to evaluate the performance of multi-cell scheduling via single DCI. Instead of using the intermediate parameter (CCE consumption), we would suggest to make some observations of PDCCH blocking rate only.  Secondly, since we are going to further discuss the throughput simulation assumptions in Proposal#2 below, we would suggest to delete the observations of the PDSCH throughput in Proposal#1.  Thirdly, regarding the power saving, we are not sure why we need to capture this aspect in the observation above considering that we never discuss how to simulate/calculate the power saving gain for Multi-cell scheduling. Even if we are going to capture it, we noticed that not all sources listed in the above observation have done power saving simulation/calculation, we may need to make it clearer. Furthermore, the potential power saving gain is probably achieved by reducing the BD/CCE budget. We may need to capture this assumption in the observations.  Fourthly, for the PDCCH blocking rate, from our perspective, the current observation is too general and unclear. For example, one may consider 1% gain as beneficial and the other may consider 30% as beneficial. We suggest to capture the detailed simulation results of PDCCH blocking rate and necessary simulation assumptions, similar as what we did for some study items. Maybe a table or template can be created for companies to collect each companies’ observations and necessary simulation assumptions.  Lastly, when collecting companies’ results of PDCCH blocking rate, the DCI size that is too small may not provide much value. Because in the practical deployment, it is not realistic to assume most of the DCI fields are shared between PCell and SCell. Thus, we suggest to capture the PDCCH blocking gain for each different DCI size individually.  Take our simulation results as an example. We would suggest the following formulation. Other simulation assumptions can also be added in the observations per companies’ request.  *Observation 1: One source observed that for inter-band CA case,*   * *In case of 700M and 4G, the average gain of PDCCH blocking rate for DCI size 72 bits, 84 bits 96 bits and 108 bits of the one-to-two scheduling DCI is about 5.7%, 4.0%, 1.4% and 0.6%, respectively.* * *In case of 700M and 2G, the average gain of PDCCH blocking rate for DCI size 72 bits, 84 bits 96 bits and 108 bits of the one-to-two scheduling DCI is about 11.1%, 9.3%, 6.1% and 4.8%, respectively.*   *Observation 3: One source observed that for intra-band (2GHz) CA case,*   * *The average gain of PDCCH blocking rate for DCI size 72 bits, 84 bits, 96 bits and 108 bits of the one-to-two scheduling DCI is about 9.5%, 7.5%, 5.6% and 4.6%, respectively.* |
| Moderator | @ZTE: Thanks for the good comments.  Firstly, I’d like to clarify that my intention for above proposal is to continue discussion on the simulation results provided by companies. Some companies may have concern on other companies’ results. So it is better to further check them. My intention is not to capture above CCE saving, PDCCH blocking rate, PDSCH throughput and UE power saving into conclusive observation. The proposal is to further discuss the results. So my proposal is to continue the discussion.  FL Proposal#1:   * Further discuss the below observations:   Secondly, regarding your comments, please kindly check my reply below:   1. If majority companies prefer not to add CCE saving gain, we can delete it from the final conclusive observation. 2. I think checking the throughput impact and the simulation assumptions can be proceeded parallel. During the procedure of checking simulation results, we can discuss whether new simulation assumptions need to be agreed for further evaluation. 3. As mentioned above, list of power saving above is for companies to check the results, which does not imply such result will be captured in observations. 4. Yes, I agree with you. So far, most companies just show the curves of PDCCH blocking performance and don’t give the detailed value. We can prepare a template for companies to provide their results. 5. The PDCCH blocking rate is related to DCI payload size. You can see all the companies’ curves include multiple DCI payload sizes which we agreed in previous meeting. When we collect the simulation results, of course, the associated DCI payload sizes should be given together. |
| vivo | Share the same view as ZTE that there is no need to capture CCE saving gain, CCE saving ratio proves nothing. |
| Huawei, HiSilicon | We agree to start from PDCCH blocking probability and PDSCH throughput. We are also OK with other templates if it helps and can be created in time. ZTE’s draft observation in our view is aligned and detailed version from FL proposal, which is a good direction.  Particularly, we try to make some modifications based on the current FL proposal, which can surely be modified based on companies comments (and can include what ZTE is proposing, in our view). One example can be found below. We will complete other cases later.  **On PDCCH blocking probability using a single DCI to schedule multiple PDSCHs on multiple carriers, compared to two separate DCIs of PDCCH payload of 60 bits for each, with PDCCH target BLER@1%, simulation results are summarized below:**   * **12 companies [OPPO, Huawei, HiSilicon, Intel, InterDigital, CATT, vivo, Nokia, NSB, Lenovo, Motorola Mobility, Qualcomm] observe decreased PDCCH blocking probability via simulation.**   + **For the case of scheduling carrier 2GHz, with same SCS as scheduled carrier, PDCCH payload 108 (*[/104] for some results?*) bits,**     - **[Huawei, HiSilicon, or other companies with similar assumptions/results], for UE number in the range of 10~20, PDCCH blocking rate is reduced by x%~y%**     - **[Company A…] For UE number in the range of 10~20 [with CA UE ratio of z%], [with/without CCE interleaving], [CORESET size of ?], the PDCCH blocking rate is reduced to x%~y%**   + **(*similarly for other combinations, PDCCH payloads*)** * **2 companies [ZTE, Ericsson] observed marginal performance gain in PDCCH blocking.**    + **For the case of scheduling carrier 700M, with different SCS from scheduled carrier 4Ghz, PDCCH payload 108 bits,**     - **[ZTE] observed PDCCH blocking is only reduced by 0.6%** * **1 company [Samsung] observe higher PDCCH blocking compared to two DCIs scheduling two PDSCHs.**   where x and y can be the lowest and highest value respectively, among all the companies in this category. In case only Huawei falls into this category, x=7 and y=18; in case 5% can be viewed obvious, then for the same SCS case, we think ZTE’s results can also be included in the first category with x=5% for example.  It may be up to companies to formulate their results, e.g. with respect to whether “**[with CA UE ratio of z%], [with/without CCE interleaving], [CORESET size of ?]**” or other factors that they have investigated.  In our view, the cases that ZTE show marginal performance gain, i.e. the second category, are limited to different SCS between carriers with PDCCH payloads of 96 and 108bits. |
| Samsung | CCE savings gains can be misleading as they don’t provide information for what matters – system throughout gain that is the motivation/metric for this study.  We also observe CCE savings in the order of 20%-30% but that is under ideal assumptions, purely based of the use of single-cell scheduling DCI vs. dual-cell scheduling DCI – without considering any other operating aspects.  Those gains never translate to more than 1% throughput gain under ideal assumptions that include (a) the saved CCEs are always possible to use, (b) scheduling is always on 2 cells (never on one cell), and (c) there is no additional overhead due to scheduling on one cell (even on the UL) while using the 2-cell scheduling DCI or due to additional padding to DCI formats in order to maintain the “3+1” DCI size budget.  None of the above ideal assumptions holds in reality. For example, if there is a 70/30 probability to schedule a UE on 2-cells/1-cell and the DCI used for scheduling on 1 cell is the 2-cell scheduling DCI, there may even be a throughput loss.  Regarding the blocking probability, most presented results are unrealistic as they assume scheduling of 10+ UEs with CA in a same slot on a 10 MHz carrier. Typically, 1-2 CA UEs are scheduled in such case and blocking is not an issue.  Further, the evaluations for the blocking probability are overly simplistic as none considered use of multiple CORESETs on the scheduling cell and, more importantly, that a UE can be scheduled on one cell (then, if the 2-cell scheduling DCI is used, the blocking will be worse).  We can further discuss assumptions to evaluate blocking, such as how often a UE is scheduled on 2 cells vs. 1 cell, or what DCI is used for scheduling on 1 cell, or how many CORESETs are used. However, that would be unnecessary given that blocking for scheduling on a ~10 MHz cell is not an issue because, practically always, no more than 2 CA UEs are scheduled in a slot. |
| CATT | Some companies argue that CCE saving ratio is not practical and prove nothing. We agree the PDCCH blocking is more practical than CCE saving ratio. However, it is depends on many things, e.g. the search space configuration, the periodicity, the AL distribution and so on. And sorry to say it is far from being practical as well. But it doesn’t mean all of them are very meaningless for the study as it can prove we do get benefits from different aspects. CCE saving ratio can provide purest proof of the benefits we can get (actually the fundamental one as all the other benefits comes from CCE saving). The saved CCEs can be converted into the PDCCH capacity increase. It is obvious that more available CCEs more UEs can be scheduled. If some companies do have concerns, we can add a note saying ‘Note: CCE saving ratio is an intermediate result and not directly reflected on the PDCCH blocking possibility’. Given that many companies provide the simulation results for CCE saving, it is fair enough to capture them in the observation.  Given we didn’t calibrate the simulation platform for now, it will cost lots of time. Hence we agree with ZTE and HW that we can collect the value range of performance gain. We can still get lots of guidance in this way. |
| MediaTek | We’re okay to focus on PDCCH blocking rate and PDSCH throughput in the discussion of observations though PDCCH blocking rate to me is also an intermediate result.  For moderator’s proposal, we would suggest to also capture which traffic type is assumed in the SLS or which method is used for PDSCH throughput gain. In addition, we propose the following modifications on MediaTek’s results in PDSCH throughput part.  On PDSCH throughput, simulation results are summarized below:   * 4 companies [Huawei, HiSilicon, vivo, MediaTek] observe non-negligible PDSCH throughput gain via simulation.   + Huawei, HiSilicon: 8~10% throughput gain for 108bits DCI or 96bits DCI.   + Vivo: 2.32~3.12% throughput gain for 96bits DCI or 108bits DCI for combination 1/2/3, 1.42% throughput gain for combination4, but if the number of UE increases to 15 or 20, using single DCI to schedule multiple PDSCH may bring 0.2%~0.31% throughput loss for combination4 as the loss caused by increased scheduling granularity cannot be compensated by throughput gain brought by the saved PDCCH resources.   + MediaTek: For 84/96bits DCI, 8.2%/22.4% mean/cell-edge UE throughput gain for Combination 1 and 27.3~29.0%/63.2~68.4% mean/cell-edge UE throughput gain for Combination 3.     - For Combination 1 results, FTP 3 traffic with packet size of 20Kbytes and 10 packets/s per UE is assumed     - For Combination 3 results, FTP 3 traffic with packet size of 10Kbytes and 12 packets/s per UE is assumed * 1 company [Samsung] observe marginal throughput gain 1.07% for Combination 1 and 0.084% for Combination 2 for 108bits DCI via estimation. * 1 company [ZTE] observe 13.4 or 8.7% loss for inter-band case and intra-band case for 84 bits DCI via simulation. |
| Nokia, NSB | We would agree with PDCCH blocking probability and PDSCH throughput, while don’t see the point in the CCE consumption.   * + The blocking probability text would benefit from values to be collected. e.g. as shown by ZTE and could perhaps be used as-is, or a data collection activity with a specific template can be done.   + The Huawei proposal for adding a sub-bullet per company would be a useful exercise for a TR, but maybe an overkill for this purpose where the summary is what matters in the coming RAN discussion when deciding whether or not to proceed with the work. A specific explanation would only be warranted for anomalous results, e.g. showing intuitively too large TP gains or increased blocking probability results. |
| OPPO | We agree with PDCCH blocking probability and PDSCH throughput. Meanwhile we think CCE saving ratio is a useful observation. CCE saving ratio is straightforward to present saving resource from two-cell scheduling. However, PDSCH throughput is impacted by many factors. Even simulation assumption is consistent, different simulators still lead significant difference in PDSCH throughput. It is difficult to define which result is more reasonable. So, we think CCE saving ratio needs to be considered, at least as an intermediate result. |
| Ericsson2 | Thank you vivo for the clarification in 2.2.5.  As commented earlier, we do not support “CCE savings” as capturing observations using such intermediate metric does not provide useful information without proper context.  For PDCCH blocking comparisons,   * Whether the blocking results are for agreed Combination 1 or for 2 should be explained * It is better to present the blocking results individually for each case than only show percentage differences (or even worse express the percentage differences as percentages) i.e.,   Gains from 1 DCI scheduling 2 PDSCHs (i.e., mc-DCI) are only available for Case 3 below. Whether below aspect has been considered or not in the evaluations should be clarified.  ***Observation 2***   * *For a CA scenario with e.g. two serving cells, the NW may choose to schedule any of following cases for a given UE based on available slots for NR scheduling on a given carrier, data in the buffer, channel conditions, NW loading and HARQ retransmission activity of each serving cell*    1. *PDSCH on cell 1 only*   2. *PDSCH on cell 2 only*   3. *PDSCH on cell 1 and cell 2*   4. *No PDSCH scheduled*   Also, below observations from our tdoc are not correctly reflected in FL Proposal#1    ***Observation 3***   * *For scenario 1 (i.e., 20MHz carrier at 2GHz used for scheduling PCell PDSCH/PUSCH on another low-band DSS carrier),*    + *in slots where PDSCH is scheduled on both cell1 and cell 2, mc-DCI can achieve similar blocking performance as baseline case with reduced CCE allocation. The amount of possible CCE reduction depends on loading, i.e., 8 CCEs for low load and smaller for higher loads. If CCE allocation is reduced any further, performance of mc-DCI is worse.*   + *Assuming 50% of slots have two-PDSCH scheduling with cell1 scheduling PDSCH on both cell1 and cell2 (optimistic assumption for scenario 1 if one of the scheduled carriers is shared with LTE), and 10 symbols available for data scheduling on scheduling cell (2 DMRS symbols), an overhead reduction of < 2.5% is expected with other optimistic assumptions that rate-matching of PDSCH around PDCCH can reclaim all the saved resources (which is unlikely when there are other DCIs in the Coreset), and that there is no performance loss due to lower flexibility when scheduling with mc-DCI. Under realistic assumptions, no gains are expected.*   ***Observation 4***   * *For scenario 2 (i.e., 100MHz mid-band 4GHz carrier used for scheduling PCell PDSCH/PUSCH on a low-band DSS carrier),*    + *using mc-DCI is not expected to provide performance gains as the blocking performance for scheduling up to 10 UEs is close to zero even for baseline case of two legacy DCIs.*   ***Observation 5***   * *Evaluations indicate that single DCI scheduling PDSCH on two cells (mc-DCI) provides marginal or no performance gains.* |
| Qualcomm | We don’t think its technically reasonable just to present the average CCE saving gain. Possible way of capturing CCE saving gain is to translate the amount of CCEs saved by the 2-cell DCI into either (1) the peak throughput improvement that is achievable by using the unused CCEs for PDSCH, or (2) the number of UEs or DCIs that can be accommodated by using the unused CCEs for PDCCH.  Regarding PDCCH blocking probability, we need to have common understandings on (1) what PDCCH blocking probability is the operational point, and (2) what number of UEs or DCIs should be accommodated in the same CORESET/PDCCH monitoring occasion are the target. Otherwise, showing gain in “the ratio of percentage” is pointless.  For the throughput gain, we don’t think vivo’s throughput gain is “non-negligible” gain. It should be captured outside from the bullet. |
| Huawei, HiSi-02 | CCE saving was used in previous study e.g. URLLC and is useful for understanding the potential. We agree that its translation to throughput or user/PDCCH capability is also useful, while in the real site it is actually one metric used for network configuration setup (; on the contrary, throughput or capacity is rarely a direct metric). However for the time being we are ok to start from PDCCH blocking rate and throughput.  We are fine to remove “non-negligible” from the bullet.  While we also request to revise Samsung results as ‘analysis-based’, rather than SLS results. |
| Moderator | @Huawei: Thanks for the good suggestions. Yes, we can give a value range for reduced PDCCH blocking rates as soon as majority companies provide their values.  @Samsung: Please kindly check below simulation assumptions which we have agreed in previous RAN1 meeting. Most companies provide PDCCH blocking rates in case of 20/100MHz carrier BW with 10/15/20 UEs per cell.  If only 1 or 2 UEs are assumed as CA UEs per cell, I am afraid that it would not be a reasonable assumption as the performance of any feature will disappear in SLS, e.g., SCell cross-carrier schedules PCell.   * Combination 1: 2 GHz, 15 kHz SCS, 2 Tx, 2 Rx, 20 MHz carrier BW, 2-symbol CORESET with 96RBs * Combination 2: 4 GHz, 30 kHz SCS, 4 Tx, 4 Rx, 100 MHz carrier BW, 1-symbol CORESET with 270RBs * [Combination 3: 700MHz, 15 kHz SCS, 2 Tx, 2 Rx, 10 MHz carrier BW, 3-symbol CORESET with 48RBs] * [Combination 4: 4GHz, 30 kHz SCS, 4 Tx, 4 Rx, 40 MHz carrier BW, 2-symbol CORESET with 96RBs]   @CATT, @Nokia: yes, we can collect the values in the template then capture the value range in conclusive observations.  @MediaTek: yes, the traffic model is added in the template for collecting PDSCH throughput. Please provide your results in the two templates then we can provide a value range for observations.  @OPPO @CATT: Since majority companies prefer no CCE saving in the conclusive observations, maybe we can firstly focus on PDCCH blocking reduction and PDSCH throughput.  @Ericsson: Sorry for missing your observations. I uploaded two templates for collecting the detailed results. If fine with you, please provide your simulation results.  @Qualcomm: I think we can focus on the reduced PDCCH blocking rates now and further discuss which operational point is reasonable for network implementation. Maybe different network vendors have different assumptions. I think the most important thing for us to collect the values in the template then capture the value range in conclusive observations.  BTW, I will not use the word of “non-negligible” or “marginal”. Let’s only capture the detailed value ranges in the observations. |
| Samsung 2 | @ Moderator: The scheduling cell can have multiple UEs scheduled per slot – both on the UL and the DL – both on a single cell and on multiple cells. The scheduling cell may also have CSS. The scheduling cell has multiple CORESETs.  None of the above were considered in evaluating blocking probability. However, that is not the point and doesn’t really matter. What matters is how many UEs the scheduling cell needs to schedule using a 2-cell DCI on a carrier with small BW (e.g. 10 MHz at 700 MHz frequency) per slot. That number is at most 1 in all field logs (in some slots, there can be single-cell scheduling) and the number of carriers an operator has below 1 GHz are very few. Multi-UE SLS results for such scenarios are still useful as throughout per cell can be determined based on the scheduler selecting a UE with favourable conditions in a slot (assuming no other restricting factors such as traffic type) but they are not relevant for the purposes of this study.  As previously mentioned, blocking evaluations also did not consider the fact that the single-cell scheduling DCI size will increase, either because the 2-cell scheduling DCI is used for that purpose or because the UL DCI will need to be padded. Arguing for blocking to justify a 2-cell scheduling DCI completely misses reality.  Further, to reiterate, whatever throughput gain each company reported for the 2-cell scheduling DCI did not consider that:   1. There would be no gain if another UE was scheduled PDSCH through the CORESET, or if any UL was scheduled through the CORESET, or if CSS exists in the CORESET 2. A 2-cell scheduling DCI won’t be used neither for all UEs on the cell nor all the time. 3. There is loss associated with padding the UL DCI to maintain the “3+1” DCI budget, or associated with using the 2-cell DCI also for single-cell scheduling.   It shouldn’t have to be argued that the above are self-evident. Nevertheless, even without considering the above, the throughput gain is 1% or less in all scenarios. If the above are also considered, it is likely that there is marginal loss when using the 2-cell scheduling DCI (due to padding the UL DCI or due to using the 2-cell DCI also for single-cell scheduling). |

FL Proposal#2:

* Take below simulation assumptions to further evaluate the impact on PDSCH throughput due to multiple carriers scheduled by a single DCI
* Companies are encouraged to report the simulation assumptions on how to use the saved CCEs for PDSCH transmission.

Table 2: System level simulation assumptions

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Performance metrics | Average UE throughput, 5%-tile UE throughput |
| Link adaptation | Separate MCS and time-frequency resources for each scheduled carrier |
| Deployment scenario | Inter-band: 700MHz + 2GHz  Intra-band: 2GHz + 2GHz |
| CORESET configuration | Follow agreed link level simulation assumptions.  Companies report the carrier where the CORESET is configured. |
| Percentage of UEs with CA capability per cell | 100% |

Regarding above proposal, companies are encouraged to provide comments in the table below.

|  |  |
| --- | --- |
| **Company** | **View** |
| ZTE | Overall, we are fine with the approach suggested by feature lead, i.e., to further align the simulation assumptions/methodologies. But we have some detailed comments below.  Two factors have big impact on the throughput simulation, i.e., (1) whether/how to use the saved CCEs for PDSCH transmission (2) whether the CORESET size is the same between the baseline and the Multi-cell scheduling scenario. The first one has been capture in the FL proposal, but the second one is not. We would suggest the following updates.  FL Proposal#2:   * Take below simulation assumptions to further evaluate the impact on PDSCH throughput due to multiple carriers scheduled by a single DCI * Companies are encouraged to report the simulation assumptions on how to use the saved CCEs for PDSCH transmission. * Companies are encouraged to report the CORESET configuration of the baseline and the Multi-cell scheduling scenario.   Regarding the performance, it seems that most companies use average cell throughput instead of average UE throughput. We would suggest to use average cell throughput.  Regarding the link adaptation, we suggest to let companies to report the assumption of DCI fields, i.e., whether MCS/TDRA/FDRA is shared or not. Without the reporting, it is not clear why/how the gain/loss is achieved.  Regarding the deployment scenario, we would suggest to add Inter-band: 700MHz + 4GHz as an optional scenario. |
| Vivo | Regarding the scenario, we would like to add 4 GHz+2GHz as this is a typical deployment in NR.  Regarding the link adaption, I am not pretty sure about the intention of ‘Separate time-frequency resources for each scheduled carrier’, the two PDSCHs are transmitted on two carriers, so they must be allocated with separate T/F resources. Do you mean that the joint-DCI should have separate TDRA/FDRA fields for the two cells? |
| Huawei, HiSilicon | We don’t agree to abandon the submitted simulation results. We support to start from the below FL summary with modifications. Actually, for companies who report SLS results, most of the parameters in the table in FL proposal#2 should/can be reported within this meeting, including the adding that ZTE proposed. What else needs to be clarified, we can clarify.  One example as below. We will complete the observations later with other cases we have simulated, e.g. considering DSS overhead.  **On PDSCH throughput, simulation results are summarized below:**   * **4 companies [Huawei, HiSilicon, vivo, MediaTek] observe non-negligible PDSCH throughput gain via simulation.**   + **Huawei, HiSilicon: 8~11~~0~~% throughput gain for 108bits DCI or 96bits DCI, based on the following assumptions**     - **Same SCS between two carriers, with 2Ghz or 700Mhz as scheduling carrier,**     - **The PDCCH blocking probability reduction is implemented**     - **Separate MCS/RV fields, separate resource allocation (RA) fields, both DCI-level and CORESET-level PDSCH rate-matching with CORESET size the same as baseline**   + **Vivo: 2.32~3.12% throughput gain for 96bits DCI or 108bits DCI for combination 1/2/3, 1.42% throughput gain for combination4, but if the number of UE increases to 15 or 20, using single DCI to schedule multiple PDSCH may bring 0.2%~0.31% throughput loss for combination4 as the loss caused by increased scheduling granularity cannot be compensated by throughput gain brought by the saved PDCCH resources.**   + **MediaTek: For 96bits DCI, 16.7%/32.7% mean/cell-edge UE throughput gain for 2GHz and 29~34%/63~100% mean/cell-edge UE throughput gain for 700MHz. In the 1st table, the average/cell-edge UE throughput gain is 8.2/22.4% for FTP 3 traffic with packet size of 20Kbytes & 10 packets/s per UE.**     - **There are two tables for 2GHz: 1st table assumes 2-symbol CORESET and 2nd table assumes 3-symbol CORESET. The UE throughput gain Ericsson refers to is from the 2nd table.** * **1 company [Samsung] observe marginal throughput gain 1.07% for Combination 1 and 0.084% for Combination 2 for 108bits DCI via estimation.** * **1 company [ZTE] observe 13.4 or 8.7% loss for inter-band case and intra-band case for 84 bits DCI via simulation.** |
| Samsung | OK to provide the SLS results but it is questionable what additional insight will be obtained given that this is purely about PDCCH resources and any overhead decrease/increase obtained from LLS can be directly translated to spectral efficiency/throughput gains/losses based on fundamental theory.  If SLS according to the suggested setup is to be performed, the assumption that all UEs both support and are configured for CA is unrealistic. OK to keep that assumption for an upper bound, but the realistic case that ~20% of UEs operate with CA should be baseline. The 50% case may also be considered to provide a mid-point for reference. |
| CATT | Our feeling is that even the same parameters listed above are used across companies, the simulation results are still diverse as SLS depends on far more assumptions compared to the ones in the table. We agree with HW, the submitted SLS simulation results should be respected. The parameters, scenarios and metric can be further reported by companies for the submitted SLS simulation results.  Regarding to the FL’s proposal, we are OK with it for the additional simulations if necessary. |
| MediaTek | We prefer to conclude whether to support multi-cell scheduling via a single DCI in Rel-17 based on the LLS/SLS results submitted this meeting. At least, some observations based on the submitted results can be made this meeting. However, we understand some companies’ concerns and open to study further with more clear evaluation assumptions but we prefer to have a deadline for decision making if any further study agreed. Study forever is not a good option.  For performance metrics, we prefer average/cell-edge UE throughput, instead of average cell throughput, at least for FTP traffic model and companies should report which traffic model is assumed.  Based on my understanding, it’s commonly assumed that all UEs support a new feature for the performance evaluation in RAN1. Not sure why we need to change such assumption specifically for this feature. |
| Nokia, NSB | The task for RAN1#104 is to produce data for RAN#91 to take a decision, so in that sense discussion of further evaluation assumptions doesn’t seem to be fruitful, but observations need to be taken based on results submitted to this meeting. |
| OPPO | The intention to further provide SLS simulation result is not clear for us. Current simulation results based on aligned simulation assumption last meeting are diverse but SLS results from most companies still have shown non-negligible gain. Although the total number of companies providing SLS result is not large, but current SLS has identify the benefit from two-cell scheduling. What do we expect from more SLS results? |

## Proposals for 3rd GTW session

FL proposals:

For multi-cell scheduling via a single DCI, capture the following observations as conclusions:

Observations:

On PDCCH blocking probability using a single DCI to schedule two PDSCHs on two carriers,

* 10 sources ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Nokia, NSB, [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)], [ZTE, R1-2101789]) reported PDCCH blocking probability via simulation.
  + 10 sources ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Nokia, NSB, [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)], [ZTE, R1-2101789]) reported reduced PDCCH blocking probability, compared to using two separate DCIs with each having 60 bits payload.
    - For the case of Combination 1: [2 GHz, 15 kHz SCS, 2 Tx, 2 Rx, 20 MHz carrier BW, 2-symbol CORESET with 96RBs],
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 6.9%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 9.48% and 23.94%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip)]) show the gain of PDCCH blocking rate reduction is 83.5%, for 5 UEs per cell with 80% CA UEs.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 9.03%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 11.02% and 28.74%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip)]) show the gain of PDCCH blocking rate reduction is 83.6%, for 5 UEs per cell with 80% CA UEs.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 12.1%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 13.15% and 35.34%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip)]) show the gain of PDCCH blocking rate reduction is 83.4%, for 5 UEs per cell with 80% CA UEs.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 19.8%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 15.15% and 41.11%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip)]) show the gain of PDCCH blocking rate reduction is 76.5%, for 5 UEs per cell with 80% CA UEs.
    - For the case of Combination 2: [4 GHz, 30 kHz SCS, 4 Tx, 4 Rx, 100 MHz carrier BW, 1-symbol CORESET with 270RBs],
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)], [Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)]) show the gain of PDCCH blocking rate reduction is 18.73%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 26.78% and 57.86%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)], [Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)]) show the gain of PDCCH blocking rate reduction is 24.92%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 28.92% and 62.25%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
        + One source ([Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)]) show the gain of PDCCH blocking rate reduction is 28% ~ 59.1%, for 5~20 UEs per cell with 50% CA UEs.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)], [Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)]) show the gain of PDCCH blocking rate reduction is 36.32%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 34.25% and 72.17%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 8 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [Lenovo, Motorola Mobility, [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)], [Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)]) show the gain of PDCCH blocking rate reduction is 42.62%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 36.03% and 77.28%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
        + One source ([Qualcomm, [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip)]) show the gain of PDCCH blocking rate reduction is 51.6% ~ 70.6%, for 5~20 UEs per cell with 50% CA UEs.
    - For the case of Combination 3: [700MHz, 15 kHz SCS, 2 Tx, 2 Rx, 10 MHz carrier BW, 3-symbol CORESET with 48RBs]
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 0.06%~70.5%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 10.29% and 24.01%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 0.75%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 11.4% and 27.14%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 3.25%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 13.9% and 35.45%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Intel, [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip)], [ZTE, R1-2101789], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 4.78%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 15.49% and 40.25%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
    - For the case of Combination 4: [4GHz, 30 kHz SCS, 4 Tx, 4 Rx, 40 MHz carrier BW, 2-symbol CORESET with 96RBs]
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 5 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 8.06%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 24.33% and 52%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 5 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 18.76%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 26.57% and 56.67%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 5 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 31.56%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 32.35% and 70.2%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 5 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [CATT, [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip)], [Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) show the gain of PDCCH blocking rate reduction is 37.99%~100%, for per cell UE number in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip)]) show the gain of PDCCH blocking rate reduction is 35.54% and 75.56%, for 10 UEs per cell with 10%, 50% CA UEs, respectively.
* More detailed results and assumptions are listed in the attached excel tables.

Regarding above observations on PDCCH blocking probability reduction, companies are encouraged to provide comments in the table below including the additional simulation assumptions and metrics.

|  |  |
| --- | --- |
| **Company** | **View** |
| ZTE | As indicated by some companies during the GTW session, we would also like to propose (b-a) as the performance metric. Based on our reading, if we use (b-a), the simulation results of PDCCH blocking rate may be more converging. Otherwise, the results may seem diverging. |
| Huawei, HiSi | To Xingguang, Ravi, Fred  Regarding whether ‘/b’ is useful, as explained, this was used for URLLC and it should be well-understood that whenever a particular range of values are interested then one should look into the numbers of absolute *a* and *b* values to check. And precluding some small values from the template can make the output incomplete. So at a minimum all results should be fairly captured in our view. A simple example would be ideal channel estimate - it can never be realistic but it is useful. We think CCE saving ratio is actually useful - a network vendor can check with your product. In a real network which product will use PDSCH throughput or PDCCH blocking rate as a metric for network maintenance? But they are useful tools for understanding the potential of a feature and are widely used in 3GPP.  Honestly, with current template including both a, b and ‘/b’, everything is clear. One can always drive (b-a) as they want. We don’t prefer to re-do that but if majority companies do not mind to update the results with (b-a), we could be ok as well.  Note in this case, the values in the above observation will also need update. |
| Samsung | Agree with the comment by ZTE. Dividing % by % can always lead to weird outcomes and have little/no meaning and do not indicate what matters for the system operation.  The following for the simulation assumptions need to be captured. A ‘Yes’/‘No’ answer suffices.   1. Was a number of CORESETs larger than one considered? 2. Was presence of PDCCH for any of (a) CSS, (b) scheduling single-PDSCH, (c) scheduling UL transmissions, considered? 3. Was blocking on single-PDSCH scheduling or on PUSCH scheduling considered?   We note that the core question of whether blocking probability is relevant at all when scheduling CA UEs on few ~10 MHz carriers (i.e. very small number of scheduled UEs with PDSCH on exactly 2 cells) remains. The evaluations assumed highly unrealistic large numbers of UEs. |
| Nokia, NSB | Agree with the point that the %-gain in blocking probability is misleading. The very low blocking probabilities are of little interest when drawing conclusion even if a very large gain percentage may be seen. It also looked to us that the gain percentages were calculated by a few companies (including Nokia as we copied the formula from some other companiy who reported their values before us) was calculating the gain as (a+b)/a, where a was blocking for one DCI scheduling two cells, and b was blocking two DCI scheduling two cells, but the DCI for a and b was of the same size, when b should be always two 60-bit DCIs. b-a would seem to make more sense, but here it should be clear that b is two DCIs of 60 bits in all results. |
| Ericsson3 | For the observations, results for agreed combinations 1 and 2 should be separated out from other combinations (e.g. it should be captured that only combination 1 and 2 are per agreed in evaluation methodology. Other combinations are additional results provided by companies).  For PDCCH blocking, reporting b-a for a given a is OK from our perspective. |

On PDSCH throughput using a single DCI to schedule two PDSCHs on two carriers, based on the summary of submitted results and detailed simulation assumptions in [R1-21xxx]

* 3 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)], [ZTE, R1-2101789]), reported PDSCH throughput via system level simulation and 2 sources ([Samsung, [R1-2101238](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101238.zip)], [Ericsson, [R1-2101562](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) reported PDSCH throughput via theoretical analysis, compared to using two separate DCIs with each having 60 bits payload.
  + For 108 bits DCI payload of two-cell scheduling DCI,
    - 1 source ([Huawei, HiSilicon, [R1-2100194](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100194.zip)]) show the gain of PDSCH throughput is 6.69 ~8.93%, for per cell UE number in range of 10~20 with 100% DL CA UE only, full buffer, no common message scheduling, and with assumptions of PDCCH blocking probability reduction implemented for PDCCH and PDSCH multiplexing (i.e. SU/MU-MIMO) implemented for PDSCH reception.
    - 1 source ([vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)]) show the gain of PDSCH throughput is 0.74% ~1.42% for combination4, 3.02 ~3.12% for combination3, 1.27% ~1.56% for combination2, 1.80% ~2.23% for combination1,for per cell UE number in range of 10~20 with 100% CA UE and full buffer traffic model, with assumptions of utilizing saved CORESET RBs for PDSCH transmission.
    - 1 source ([ZTE, R1-2101789]) show the gain of PDSCH throughput is <1%, for 10 UEs per cell UE with 100% CA UE and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission.
  + For 96 bits DCI payload of two-cell scheduling DCI,
    - 1 source ([Huawei, HiSilicon, [R1-2100194](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100194.zip)]) show the gain of PDSCH throughput is -7.89%~10.92% with similar assumptions as provided for PDCCH payload of 108 bits.
    - 1 source (vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)]) show the gain of PDSCH throughput is -0.31%~0.94% for combination4, 3.02%~3.11% for combination3, 1.90%~2.32% for combination2, 2.31%~2.44% for combination1, for per cell UE number in range of 10~20 with 100% CA UE and full buffer traffic model, with assumptions of utilizing saved CORESET RBs for PDSCH transmission
  + For 84 bits DCI payload of two-cell scheduling DCI,
    - One source([[ZTE, R1-2101789]]) shows the gain of PDSCH throughput is -13.4%~-8.7%, for 10 UEs per cell 100% CA UEs and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission and shared FDRA/TDRA for two scheduled PDSCHs.
  + One source ([Samsung, [R1-2101238](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101238.zip)]) shows there is no gain for 20MHz BW and only PDSCH scheduling on 2 cells all the time (no single-cells scheduling, no UL, no CSS) and no loss due to UL DCI padding, with assumption of 84 or 132 bits of the two-cell scheduling DCI by applying the Shannon capacity formula to the CCE savings and normalizing by the total number of time-frequency resources per slot for the indicated BW of the scheduling cell.
  + One source ([Ericsson, [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)]) shows there is <2.5% gain for Combination 1 and no gain for Combination 2, with idealistic assumption that all saved PDCCH CCE resources can be reused for PDSCH, no scheduling flexibility is lost due to two-cell DCI, and assumption that 50% slots can benefit from using two-cell scheduling DCI.96 bits payload size for the two-cell scheduling DCI is assumed.
* More detailed results and assumptions are listed in the attached excel tables.

Regarding above observations on PDSCH throughput, companies are encouraged to provide comments in the table below including the additional simulation assumptions and metrics.

|  |  |
| --- | --- |
| **Company** | **View** |
| ZTE | **Comment#1**: One of the description about our simulation seems not in line with our assumptions. Thus, updated it in the above observation (also copied below).   * + For 84 bits DCI payload of two-cell scheduling DCI,     - One source([[ZTE, R1-2101789]]) shows the gain of PDSCH throughput is -13.4%~-8.7%, for 10 UEs per cell 100% CA UEs and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission and shared FDRA/TDRA for two scheduled PDSCHs.   **Comment#2**: Currently, vivo’s and Huawei’s simulation results are captured together. However, since the simulation results diverges a lot, we would suggest to separate vivo’s and Huawei’s simulation results of PDSCH throughput. Take the following as an example, one result is “-0.31%” and another result is “10.88%”, it may be clearer to separate them into two bullets.   * + For 96 bits DCI payload of two-cell scheduling DCI,     - 2 sources ([Huawei, HiSilicon, [R1-2100194](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100194.zip)], [vivo, [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip)]) show the gain of PDSCH throughput is -0.31%~10.88%, for per cell UE number in range of 10~20 with 100% CA UE and full buffer traffic model. |
| Huawei, HiSi | Please see our further modifications above with change mark and comments below.   * + Assuming there will be some detailed assumptions that are not suitable to be all captured in the above texts, we modified the main bullet   + SLS and analysis-based approaches are separately given   + Some more assumptions for our results added per the email exchanges   + Ok to separate our results from vivo in the above case (commented by ZTE).   Siqi,  Could you then update the corresponding values in the above, if you are fine with such formulation.  Xingguang,  Could you double check your results that you have uploaded in the template? As the number values are even different from that in your updated contribution in R1-2101789 (where the baseline throughput and that for joint scheduling DCI is exactly the same at fourth decimal place).  Aris, Ravi  Please check if my modifications are proper, and what you want to additionally clarify for our results. I put square bracket in ‘ideal’ for Ericsson results – better to be specific. |
| Samsung | The following for the simulation assumptions need to be captured. A ‘Yes’/‘No’ answer suffices.   1. Were all UEs assumed to be scheduled PDSCHs on 2 cells all the time? 2. Was there ever any PDCCH associated with CSS or UL scheduling? 3. Was there any consideration on PDCCH overhead from one of: (a) scheduling single-cell PDSCH by the 2-cell scheduling DCI, or (b) increasing/padding the UL DCI size to maintain the “3+1” DCI size budget.   We also note that:   1. throughput gains using CORESET-based rate matching for PDSCH do not exist as (a) blocking is not an issue or (b) a CORESET cannot be dimensioned only for scheduling UEs capable/configured for CA on 2 cells. 2. Throughput gains using CCE-based rate matching for PDSCH can exist only if (a) the UE is the only one scheduled with only PDSCH in the CORESET and (b) an appropriate FDRA includes the CORESET. |
| vivo | Yi, Xingguang  We have updated the numbers above accordingly. |
| ZTE | Thank you Yi and Siqi for the updates.  @ Yi, thank you for the careful check. We double checked internally, it is a copy-past error in our contribution forCase B (DCI size=108bits) when preparing the figures. The results we submitted in the templated are the correct one. Sorry for the confusion. |
| Ericsson3 | For the observations, results for agreed combinations 1 and 2 should be separated out from other combinations (e.g. it should be captured that only combination 1 and 2 are per agreed in evaluation methodology. Other combinations are additional results provided by companies).  Updated the description for Ericsson results for clarity.  Editorial: when capturing observations better to say ‘8% loss’ than ‘-8% gain’. |
| Vivo2 | I corrected some of the copy-paste errors in our values above, and I also separated out the results of the different combinations. |

## Updated proposals for 3rd GTW session

FL proposals:

For multi-cell scheduling via a single DCI, capture the following observations as conclusions:

Observations:

On PDCCH blocking probability using a single DCI to schedule two PDSCHs on two carriers,

* 11 sources ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [Huawei, [3](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100194.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Nokia, [8](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100720.zip)], [Lenovo, [9](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100771.zip)], [Qualcomm, [15](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101491.zip)], [Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)], [ZTE, 19], [Samsung, 12]) reported PDCCH blocking probability via simulation.
  + 10 sources ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [Huawei, [3](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100194.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Nokia, [8](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100720.zip)], [Lenovo, [9](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100771.zip)], [Qualcomm, [15](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101491.zip)], [Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)], [ZTE, 19]) reported reduced PDCCH blocking probability, compared to using two separate DCIs with each having 60 bits payload.
    - For the case of Combination 1 (agreed in RAN1#103-e): [2 GHz, 15 kHz SCS, 2 Tx, 2 Rx, 20 MHz carrier BW, 2-symbol CORESET with 96RBs],
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 4%~17.8%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 2.4% and 9.6%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [8](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100720.zip)]) show the reduced PDCCH blocking probability is 53.9%, for 5 scheduled UEs per slot per cell with 80% CA UEs.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 3.7% and 8.8% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 5.1%~24%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 2.7% and 11.5%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [8](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100720.zip)]) show the reduced PDCCH blocking probability is 53.9%, for 5 scheduled UEs per slot per cell with 80% CA UEs.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 4.2% and 10% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 7.2%~29%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 3.3% and 14.2%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [8](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100720.zip)]) show the reduced PDCCH blocking probability is 61%, for 5 scheduled UEs per slot per cell with 80% CA UEs.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 4.5% and 13.9% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 8.6%~32%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 3.8% and 16.5%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Nokia, NSB, [8](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100720.zip)]) show the reduced PDCCH blocking probability is 62.6%, for 5 scheduled UEs per slot per cell with 80% CA UEs.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 4.8% and 15.7% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
    - For the case of Combination 2 (agreed in RAN1#103-e): [4 GHz, 30 kHz SCS, 4 Tx, 4 Rx, 100 MHz carrier BW, 1-symbol CORESET with 270RBs],
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 6 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)] show the reduced PDCCH blocking probability is 0.8%~21.3%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 0.2% and 1.6%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0% and 0.2% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Qualcomm, [15](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101491.zip)]) show the reduced PDCCH blocking probability is 0.8%~24.7%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 0.2% and 1.7%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Qualcomm, [15](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101491.zip)]) show the reduced PDCCH blocking probability is 0.1% ~ 8.1%, for 5~20 scheduled UEs per slot per cell with 50% CA UEs.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0% and 0.4% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 6 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)] show the reduced PDCCH blocking probability is 0.8%~37.5%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 0.3% and 2.0%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0% and 0.4% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 7 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [Lenovo, 9], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Qualcomm, [15](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101491.zip)]) show the reduced PDCCH blocking probability is 0.8%~43.5%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 0.3% and 2.1%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Qualcomm, [15](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101491.zip)]) show the reduced PDCCH blocking probability is 0.1% ~ 21.9%, for 5~20 scheduled UEs per slot per cell with 50% CA UEs.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0% and 0.4% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
    - For the case of Combination 3(optional for companies): [700MHz, 15 kHz SCS, 2 Tx, 2 Rx, 10 MHz carrier BW, 3-symbol CORESET with 48RBs]
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 6 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 3.6%~24%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 3.0% and 10.8%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([ZTE, 19]) show the reduced PDCCH blocking probability is 0.1%~1.1% when the SCS is different between scheduling cell and scheduled cell, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 8.6% and 9.5% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 6 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 4.7%~34%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 3.3% and 12.2%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([ZTE, 19]) show the reduced PDCCH blocking probability is 0.6%~2.2% when the SCS is different between scheduling cell and scheduled cell, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 9.5% and 11.3% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 6 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 7.6%~34%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 4.0% and 16.0%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([ZTE, 19]) show the reduced PDCCH blocking probability is 2.8%~5.3% when the SCS is different between scheduling cell and scheduled cell, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 11.5% and 16.3% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 6 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)], [Intel, [7](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100678.zip)], [ZTE, 19]) show the reduced PDCCH blocking probability is 9.8%~34%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 4.5% and 18.2%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([ZTE, 19]) show the reduced PDCCH blocking probability is 4.1%~7.5% when the SCS is different between scheduling cell and scheduled cell, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 12.8% and 18.8% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
    - For the case of Combination 4(optional for companies): [4GHz, 30 kHz SCS, 4 Tx, 4 Rx, 40 MHz carrier BW, 2-symbol CORESET with 96RBs]
      * For 108 bits DCI payload of two-cell scheduling DCI,
        + 4 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)][16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)) show the reduced PDCCH blocking probability is 2.4%~16%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 0.9% and 5.9%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0.4% and 2.5% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 96 bits DCI payload of two-cell scheduling DCI,
        + 4 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)]) show the reduced PDCCH blocking probability is 2.7%~16.2%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 1.0% and 6.4%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0.4% and 2.6% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 84 bits DCI payload of two-cell scheduling DCI,
        + 4 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)]) show the reduced PDCCH blocking probability is 2.8%~28%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 1.2% and 8.0%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0.6% and 4.9% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
      * For 72 bits DCI payload of two-cell scheduling DCI,
        + 4 sources ([Huawei, 3], [OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [CATT, [4](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100359.zip)]) show the reduced PDCCH blocking probability is 2.9%~40.7%, for number of scheduled UEs per cell per slot in range of 5~20 with 100% CA UE.
        + One source ([OPPO, [2](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100187.zip)]) show the reduced PDCCH blocking probability is 1.3% and 8.6%, for 10 scheduled UEs per slot per cell with 10%, 50% CA UEs, respectively.
        + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) show the reduced PDCCH blocking probability is 0.6% and 5.0% for 5 and 10 scheduled UEs per slot per cell with 100% CA UEs, with assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot.
  + 1 source (Samsung) reported increased PDCCH blocking probability, compared to using two separate DCIs with each having 60 bits payload.
    - For the case of Combination 1 (agreed in RAN1#103-e): [2 GHz, 15 kHz SCS, 2 Tx, 2 Rx, 20 MHz carrier BW, 2-symbol CORESET with 96RBs],
      * For 108 bits DCI payload of two-cell scheduling DCI
* More detailed results and assumptions are listed in the attached excel tables.

Regarding above observations on PDCCH blocking probability reduction, companies are encouraged to provide comments in the table below including the additional simulation assumptions and metrics.

|  |  |
| --- | --- |
| **Company** | **View** |
| Moderator | @ZTE @Samsung @Nokia @Ericsson @Huawei: (b-a) is reflected in above observations.  @Ericsson: To address your concern, I added “optional for companies” for Combination 3 and 4, and “(agreed in RAN1#103-e)” for Combination 1 and 2.  @Samsung: Regarding the three assumptions as you mentioned above, we have not discussed them in previous RAN1 meeting. I think majority companies may not simulate them. I leave them for companies to add in the template. |
| Huawei | @FL  We are fine with taking some as ‘optional’ as previously agreed.  @Xingguang,  One place seems to be  “and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission and with shared FDRA/TDRA for two scheduled PDSCHs”  We also separated some cases of different SCS between carriers from the cases of same SCS, is it fine with you?  @Aris  We’ve captured the assumptions in the template with   * + DL CA UE only, thus no UL   + No common message scheduling – a bit different from CSS as UE specific can also be scheduling on CSS. Anyway, again, CSS is rare and not on sScell when scheduling Pcell, thus will not change much.   + Full buffer, i.e. no slot restriction   + Not capturing any about DCI size budget for now. That can be clarified separately then the thought about possibility of no change of DCI size budget should also be captured, since it depend on design.   We don't agree with the gain does not exist for CORESET/CCE-based based rate matching, because we are looking into benefits and CORESET can be configured for 2-cell scheduling. CCE-based rate matching must be useful as it was specified at the time, and would be up to network configuration.  I don’t expect to change your views on how some results could be useful or not – it is even questionable to use analysis based approach which can of course be useful for guiding some research on high level but won't be able to be used for indicate x~xx% difference. Otherwise no simulation needed later on. There are agreed assumptions and amount of results showing something, especially for the parameters that fully are under network control – operators may have better feeling on those numbers.  @Ravi, Ajit  We have some clarification questions:   * + On PDCCH blocking, better to capture the assumption about 50% chance per UE used for UL scheduling somewhere. Is it fine?   + We noticed that there is obvious difference for UE geometry/AL distribution in your results from others, e.g. the ratio of AL=1 for Comb-1@60bits is 93% while all others report less than 45%. This does not seem to be common as geometry is not supposed to be such different.   + On PDSCH throughput, is the UL scheduling of 50% assumed in PDCCH blocking further applied on top of the 50% PDSCH slots for 2-cell scheduling? |
| Samsung | @All – The comments made in the previous round stand and are not repeated here.  @All – I updated the introductory text in 2.2.1 and 2.2.2 to reflect what was commonly assumed by all in the simulations. Please check and we can of course discuss if something needs to be revised.  @Yi – Thanks for the update.  Overall OK with the update – one thing to also clarify is that there is never any single-cell PDSCH scheduled (i.e. there are no UEs that are either non DL-CA capable or simply not configured for DL CA that are scheduled).  OK not capturing anything about the DCI format size in the template – that can be argued separately.  We will have to agree to disagree about whether there is any gain if you assume only CORESET-based rate matching (i.e. assume that the CORESET size can somehow be reduced as if the only PDCCHs that can be transmitted in any slot are the ones for scheduling PDSCH on two cells). As previously mentioned, we do not agree to such statement as it is not realistic. |
| Ericsson4 | For the observations on blocking – “*for per cell UE number in range of …”* , should be *for number of scheduled UEs per slot in range of …* as that is the driving factor for blocking and not the actual number of UEs in the cell. Also observation should be as --- *the blocking probability with scheduling based on legacy DCI is in the range of x1-y1%, and with two-cell DCI is in rage of x2-y2% showing blocking probability reduction of x3-y3%* . This would be aligned with ‘(b-a) for a given a’ approach that we discussed.  Then on comments from Yi – Thanks for the comments. OK to capture that we considered UL scheduling. Can add e.g. *Note1: One source [Ericsson, R1-2101562] also modelled UL grants with assumption that there is a 50 % chance per UE that a DCI carrying an UL grant with 60 bit DCI size is sent.* On SINR distribution, our evaluations included beamforming when estimating the SINR distribution. |
| Qualcomm | In the observation, some corrections on reference to our paper have been corrected.  Agree with Ericsson4 that the description of observations had better to reflect ‘(b-a) for a given a’ approach. |
| Moderator | @Samsung: minor revisions in 2.2.1 and 2.2.2. Please check whether it is OK to you.  @Ericsson: (1) I made some additions as you suggested. Should be better “*number of scheduled UEs per cell per slot”.* (2) I agree with you that your suggestion is good. When I made update, I find the observations will be too long. So it is better not to add more. Furthermore, the template for PDCCH blocking rates is also attached with the FL summary. Hence the blocking probability with scheduling via legacy DCI and with two-cell scheduling can be easily checked by companies. Hope this clarifies your concern. |
| OPPO | We are fine with FL proposal. |
| ZTE | @Yi, we are ok with your updates on our simulation results. |
| Huawei03 | Some modifications to the texts on 2.2.1 and 2.2.2 tagged with Huawei03.  @Xingguang  Thanks for confirmation.  @Aris  Thanks for the response and check.  Ok, I will additionally capture the below to the template:   * + The CORESET is assumed to be used for either single-cell scheduling only for baseline, or for two-cell scheduling only for the joint scheduling PDCCH.   I don’t know how I can be even clearer, as said for CORESET level rate matching, we DONOT reduce the CORESET size since all PDSCH are rate-matched around the semi-statically configure CORESET. The gain comes from more PDCCHs and also more PDSCHs that can be multiplexed on the same resources. Additionally, we ALSO have results for CCE-level rate matching which is as specified in R15. Separately there is reported result from other companies assuming the CORESET size can reduced with keeping PDCCH blocking rate unchanged, which in our view is also quite natural and valid as an implementation result of single-DCI joint scheduling - up to network control.  @Ajit  Thanks for the response. Yes, a note is fine, either in the text for observation or in the template isok with us.  Could you also clarify the below (which was asked in the last round),   * + On PDSCH throughput, is the UL scheduling of 50% assumed in PDCCH blocking further applied on top of the 50% PDSCH slots restriction for 2-cell scheduling in your throughput analysis? |
| Ericsson5 | Thanks, Haipeng for capturing “*number of scheduled UEs per cell per slot”.* On capturing ‘(b-a) for given a’, we still think that provides clearer picture but would not insist if we are only company. On observations being too long – perhaps using reference numbers for identifying tdocs can compress them.  Yi – Yes as also explained in the tdoc. The Note can be as follows -- *Note: UL grants are also modelled for all the simulated cases in [Ericsson,* [*R1-2101562*](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip)*], i.e., For each UE, one PDSCH for each cell in slots where two-cell PDSCHs are scheduled, and 1PUSCH with 50% chance per slot, are assumed.* |
| vivo | Thanks to FL for summarizing the observations, we are fine with FL proposal.  Regarding Samsung’s comments on the simulation based on reduced CORESET BW. I don't think such an assumption is unrealistic in any case, how to configure CORESET size can be decided by gNB, and it is natural to assess how much gain can be expected assuming that all the saved RBs are utilized.  I have already added the assumptions (utilizing saved CORESET RBs for PDSCH transmission) to the observation of throughput and the assumptions (no UL DCI, no single-cell scheduling, no CSS) to the template of PDCCH blocking rate as Samsung suggested. |
| Moderator | @Ericsson: Thanks for the good suggestions. The reference numbers have been used to replace the tdoc numbers in the observations. |
| Huawei04 | @all  For Huawei results, corrected one value from -7.89% to 7.89%.  We’ve also added one more assumption to the template as per the discussion with Aris.  We also added one sentence of below to section 3.3, given some companies may have interest. For information.  “Although not in the scope, we also have results for the scenarios of more than 2 CCs, as in [3].”  @Xingguang  Thanks for confirmation.  Also, for throughput, 108bits, for 10 UEs per cell UE with 100% CA UE and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission. Is it also with the assumption that saved CCE resources are not used for PDCCH transmission? (sorry if you’ve clarified somewhere).  @Ajit  Thanks. |
| Moderator | @Ericsson @all: As clarified by Ajit, Ericsson used different simulation assumptions with other companies, i.e., 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot. So I listed Ericsson’s results separately and added above assumptions. Please Ajit or Ravi double check that. |

On PDSCH throughput using a single DCI to schedule two PDSCHs on two carriers, based on the summary of submitted results and detailed simulation assumptions in [R1-21xxx]

* 4 sources ([Huawei, 3], [vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)], [ZTE, 19], [MediaTek, [6](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_104-e/Docs/R1-2100611.zip)]), reported PDSCH throughput via system level simulation and 2 sources ([Samsung, [12](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101238.zip)], [Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) reported PDSCH throughput via theoretical analysis, compared to using two separate DCIs with each having 60 bits payload.
  + For 108 bits DCI payload of two-cell scheduling DCI,
    - 1 source ([Huawei, 3]) show the gain of PDSCH throughput is 6.69 ~8.93%, for per cell UE number in range of 10~20 with 100% DL CA UE only, full buffer, no common message scheduling, and with assumptions of PDCCH blocking probability reduction implemented for PDCCH and PDSCH multiplexing (i.e. SU/MU-MIMO) implemented for PDSCH reception.
    - 1 source ([vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)]) show the gain of PDSCH throughput is 0.74% ~1.42% for combination4, 3.02 ~3.12% for combination3, 1.27% ~1.56% for combination2, 1.80% ~2.23% for combination1,for per cell UE number in range of 10~20 with 100% CA UE (no UL DCI, no single-cell scheduling, no CSS) and full buffer traffic model, with assumptions of utilizing saved CORESET RBs for PDSCH transmission.
    - 1 source ([ZTE, 19]) show the gain of PDSCH throughput is <1%, for 10 UEs per cell UE with 100% CA UE and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission.
  + For 96 bits DCI payload of two-cell scheduling DCI,
    - 1 source ([Huawei, 3]) show the gain of PDSCH throughput is 7.89%~10.92% with similar assumptions as provided for PDCCH payload of 108 bits.
    - 1 source (vivo, [5](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100474.zip)]) show the gain of PDSCH throughput is -0.31%~0.94% for combination4, 3.02%~3.11% for combination3, 1.90%~2.32% for combination2, 2.31%~2.44% for combination1, for per cell UE number in range of 10~20 with 100% CA UE (no UL DCI, no single-cell scheduling, no CSS) and full buffer traffic model, with assumptions of utilizing saved CORESET RBs for PDSCH transmission
    - 1 source ([MediaTek, 6]) shows the gain of PDSCH throughput is 3.0%~8.1% for combination1 for per cell UE number of 10 with 100% CA UEs and full buffer traffic model, with assumptions of utilizing saved CORESET RBs for PDSCH transmission
    - 1 source ([MediaTek, 6]) shows the gain of PDSCH throughput is 8.2%~22.4% for combination1, 27.3%~63.2% for combination3 for per cell UE number of 10 with 100% CA UEs and FTP 3 traffic model with packet size = 20Kbytes (combination1) and 12Kbytes (combination3), with assumptions of utilizing saved CORESET RBs for PDSCH transmission
  + For 84 bits DCI payload of two-cell scheduling DCI,
    - One source([[ZTE, 19]]) shows the gain of PDSCH throughput is -13.4%~-8.7%, for 10 UEs per cell 100% CA UEs and full buffer traffic model without assumptions of utilizing saved CCE resources for PDSCH transmission and with shared FDRA/TDRA for two scheduled PDSCHs.
    - 1 source ([MediaTek, 6]) shows the gain of PDSCH throughput is 3.0%~8.1% for combination1 for per cell UE number of 10 with 100% CA UEs and full buffer traffic model, with assumptions of utilizing saved CORESET RBs for PDSCH transmission
    - 1 source ([MediaTek, 6]) shows the gain of PDSCH throughput is 8.2%~22.4% for combination1, 29.0%~68.4% for combination3 for per cell UE number of 10 with 100% CA UEs and FTP 3 traffic model with packet size = 20Kbytes (combination1) and 12Kbytes (combination3), with assumptions of utilizing saved CORESET RBs for PDSCH transmission
  + One source ([Samsung, [12](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101238.zip)]) shows there is no gain for 20MHz BW even for only PDSCH scheduling on 2 cells all the time (no single-cells scheduling, no UL, no CSS) and no loss due to UL DCI padding, with assumption of 84 or 132 bits of the two-cell scheduling DCI by applying the Shannon capacity formula to the CCE savings and normalizing by the total number of time-frequency resources per slot for the indicated BW of the scheduling cell.
  + One source ([Ericsson, [16](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2101562.zip)]) shows there is <2.5% gain for Combination 1 and no gain for Combination 2, with assumption that all saved PDCCH CCE resources can be reused for PDSCH, no scheduling flexibility is lost due to two-cell DCI, and assumption that 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI modelled per slot on top.96 bits payload size for the two-cell scheduling DCI is assumed.
* More detailed results and assumptions are listed in the attached excel tables.
* Combination 1 and Combination 2 in simulation assumptions are agreed in RAN1#103-e, and Combination 3 and Combination 4 are optional.

Regarding above observations on PDSCH throughput, companies are encouraged to provide comments in the table below including the additional simulation assumptions and metrics.

|  |  |
| --- | --- |
| **Company** | **View** |
| Moderator | @all: Companies please further check. |
| OPPO | We are fine with FL proposal. |
| Ericsson5 | For the observations on PDSCH throughput – results for agreed combinations 1 and 2 should be separated out from other combinations e.g. it should be captured that only combination 1 and 2 are agreed in evaluation methodology, other combinations are additional results provided by companies (as we also commented earlier). |
| MediaTek | Add our results in the above based on Moderator’s format.  We also add our results in the excel file. |
| Moderator | @Ericsson: One bullet is added above to show agreed combinations 1 and 2 and optional combination 3 and 4. Furthermore, in the excel table of PDSCH throughput, companies also reported the band combinations and CORESET configurations. Hope this is fine with you. |
| Moderator2 | @Ericsson @all: As clarified by Ajit, Ericsson used different simulation assumptions with other companies, i.e., 50% slots can benefit from using two-cell scheduling DCI and 50% UL DCI is modelled per slot. So I added above assumptions to Ericsson’s results. Please Ajit or Ravi double check that. |

# Standard impact

## DCI format design

If scheduling multiple PDSCHs on multiple carriers via a single DCI is supported, one important thing is to design the DCI format. Based on the simulation results, for reducing PDCCH blocking probability, the DCI payload should be further compressed. So many fields in the DCI need to be shared for the PDSCHs scheduled on two carriers. However, this scheduling inflexibility may lead to throughput loss for inter-band CA case. Due to the large frequency separation between the scheduled carriers in inter-band CA, the channel conditions are less correlated. It is difficult to assume same link adaptation property on the scheduled carriers and use single fields for indicating same MCS, frequency domain resource allocation as well as time domain resource allocation. For full flexibility scheduling two PDSCHs on two carriers by a single DCI, almost all the related fields in the scheduling DCI need to be doubled except DAI, HARQ timing, PRI, TPC and 24-bit CRC. However, the larger the DCI payload size, the lower the transmission reliability and less coverage. As a result, further overhead reduction is required for the two-carrier scheduling DCI at the cost of potential reduction in scheduling flexibility.

In addition, in order not to increase UE’s PDCCH blind decoding budget as one target of Rel-17 DSS, another open issues is whether the multi-carrier scheduling DCI needs to schedule not only a single PDSCH but also two PDSCHs on two carriers when the UE is configured with such feature.

Regarding DCI format design, companies’ views are summarized as below:

|  |  |
| --- | --- |
| Company | Key Proposals/Observations |
| ZTE | Observation 5: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to discuss whether to adopt shared indication or separate indication for each DCI field.  Observation 6: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to further study how to handle the Rel-16 newly introduced DCI fields in DCI format 1\_1.  Observation 7: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to further study whether to reuse DCI format 1\_1/1\_2 or introduce a new DCI format for one-to-two scheduling.  Observation 8: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to further study how to indicate the two scheduled carriers.  Observation 9: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to further study how to guarantee the current BD/CCE budget. |
| Huawei, HiSilicon | Observation 7: For the DCI scheduling multi-carrier scheduling, some DCI fields can be predefined to be independent for separate PDSCHs, some fields can be predefined to be common for 2 PDSCHs, and the other fields can be configurable to be independent or common based on network decisions.  Observation 8: Even with the simplest DCI design of sharing some fields according to network configuration, significant bits can be saved, e.g. to 84 bits for the presented evaluation combinations and corresponding gains. The flexibility is still under network control.  Observation 9: Scheduling PDSCH(s) on multiple cells with a single PDCCH can be specified without impact on the current PDCCH blind decoding budget. |
| CATT | Proposal 3: The DCI content for multi-cell PDSCH scheduling and HARQ feedback procedure need to be further studied. |
| vivo | Proposal 2. Field type (i.e., shared or cell-specific) of each information field in joint-DCI needs to be investigated.  Observation 7. To support multi-cell scheduling, the following issues need to be resolved - DCI field design - Any restrictions on the scheduled cells to be paired for multi-cell scheduling - Framework of multi-cell scheduling - Whether to introduce a new DCI format  - PDCCH BD budget maintenance if multi-cell scheduling is enabled - HARQ-ACK codebook determination if multi-cell scheduling is enabled |
| Intel | Observation 3: Potential specification impacts include but not limited to   * The RRC configuration * Separate design for each DCI field * UE complexity on PDCCH detection. * HARQ-ACK transmission. |
| Nokia, NSB | Observation 3: The baseline design would be to determine DCI format fields based on primary of the two-cells and interpret the fields for the secondary of the two-cells as in case of BWP switching R15. Some fields could be further optimized or doubled in the DCI format which is FFS. |
| Lenovo, Motorola Mobility | Proposal 2: Further study payload size reduction for the two-cell scheduling DCI.  Proposal 3: The two-cell scheduling DCI can schedule one PDSCH on one cell or two PDSCHs on two cells. |
| LG | Proposal #2: At least following issues would need to be addressed, and relevant specification impacts (and standardization workload for them) are expected, if the single DCI based multi-cell PDSCH scheduling is introduced.   * How to indicate the multiple cells with PDSCH transmission by single scheduling DCI * How to compose (and signal) the DCI fields in the multi-cell PDSCH scheduling DCI * How to construct PDCCH search space for the multi-cell scheduling DCI transmission * How to allocate (and handle) PDCCH BD candidates for the multi-cell scheduling DCI |
| ETRI | Observation 1: Multi-cell scheduling via a single DCI should be generally applicable for any valid CA scenario.  Observation 2: Multi-cell scheduling via a single DCI should allow a sufficiently wide range of scheduling flexibility to support different scenarios.  Observation 3: For multi-cell joint scheduling, the principle that one PDSCH is allocated within a cell needs to be kept the same to minimize the specification workload.  Observation 5: Need of dynamic switching between single-cell DCI and multi-cell DCI can be discussed together with the design of the multi-cell DCI contents. |
| ASUSTeK | Proposal 2-1: At least DCI fields about the feedback information of the multiple PDSCHs can be shared between the multiple PDSCHs, e.g. TPC command for scheduled PUCCH, PUCCH resource indicator, PDSCH-to-HARQ feedback timing indicator, downlink assignment index  Proposal 2-2: At least DCI fields about the resource assignment or the transmission parameter of the respective PDSCHs cannot be shared between the multiple PDSCHs, e.g. TDRA field, FDRA field, TB information, HARQ process number, TCI field.  Proposal 3: Constrain one of the two scheduled cell to be the scheduling cell to reduce the number of bits that are induced to the DCI formats for supporting the multi-cell PDSCH scheduling via a single DCI. |
| Intel | Observation 1: To support 2-cell scheduling by a single DCI, at least the following bit fields are likely to be duplicated: FDRA, MCS/NDI/RV and Antenna ports/TCI. TDRA field may be duplicated too. |
| InterDigital | Support a single DCI to schedule two PDSCH in different cells. |
| DOCOMO | Observation 1:   * PDCCH of P(S)Cell/SCell scheduling PDSCH on multiple cells using a single DCI can improve PDCCH resource efficiency.   Observation 2:   * In the assumed scenario (e.g. Inter-band CA with PCell (DSS carrier) and an SCell), CRC field attached to DCI (i.e. 24-bit) can be shared between the scheduled multiple cells.   Observation 3:   * In the assumed scenario (e.g. Inter-band CA with PCell (DSS carrier) and an SCell), 3-bit CIF may be reasonable assumption for single DCI scheduling PDSCH on multiple cells.   Observation 4:   * In the assumed scenario (e.g. Inter-band CA with PCell (DSS carrier) and an SCell), at least the case where the number of PDSCH TBs on multiple cells scheduled by single DCI is two can be considered.   Observation 5:   * In the assumed scenario (e.g. Inter-band CA with PCell (DSS carrier) and an SCell), it may be better to separate Time domain resource assignment field for each scheduled cell.   Observation 6:   * In the assumed scenario (e.g. Inter-band CA with PCell (DSS carrier) and an SCell), it may be better to separate Frequency domain resource assignment field for each scheduled cell.   Observation 7:   * Whether/how to support some indications in DCI for multiple scheduled cells can be considered.   + e.g. rate matching indicator, BWP indicator, CSI request and SRS request   Observation 8:   * How to determine the size of DCI scheduling PDSCH on multiple cells can be considered.   Observation 9:   * How to indicate the scheduled cells by using a single DCI to the UE can be considered. * Whether/how to support dynamic switching between scheduling a single cell and scheduling multiple cells can be considered.   Observation 10:   * Whether the same TB and/or different TBs is/are scheduled on multiple cells can be considered. |

FL suggestions:

The issues about DCI format design can be discussed after RAN1 agree to support the multi-cell scheduling DCI.

## HARQ-ACK codebook design

Regarding HARQ-ACK codebook design, there is no issue for Type 1 HARQ-ACK codebook due to the semi-static codebook size. However, for Type 2 HARQ-ACK codebook, since each non-fallback DCI can schedule one or two PDSCHs, when the DCI is missed by UE, there may be misunderstanding between gNB and UE on the number of scheduled PDSCHs. In that sense, HARQ-ACK codebook ambiguity may happen. As a result, how to construct the Type 2 HARQ-ACK codebook needs to be considered in order to synchronize the same understanding between gNB and UE.

**Company views:**

|  |  |
| --- | --- |
| **Company** | **Key Proposals/Observations** |
| ZTE | Observation 10: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to further study how to perform the corresponding HARQ-ACK feedback. |
| CATT | The HARQ-ACK feedback procedure may also need to be further studied accordingly, e.g. the SCS and scheduling/feedback timing may be different for the different scheduled cells. We also provide some tentative insights below from our side:   * For type1 HARQ-ACK codebook, current mechanism can be directly reused if two separate PDSCHs are scheduled on different cells respectively. * Design of C-DAI and T-DAI in one DCI for counting multiple PDSCHs scheduled by one DCI should be considered. * HARQ-ACK timing needs to be further considered as the scheduling timing and feedback timing may be both different on the two scheduled cells. |
| Intel | Observation 3: Potential specification impacts include but not limited to   * The RRC configuration * Separate design for each DCI field * UE complexity on PDCCH detection. * HARQ-ACK transmission. |
| ZTE | Observation 8: If single DCI scheduling two PDSCHs on two carriers is supported, RAN1 needs to further study how to perform the corresponding HARQ-ACK feedback. |
| Lenovo, Motorola Mobility | Observation 7: HARQ-ACK feedback for the two PDSCHs scheduled by a single DCI is included in same HARQ-ACK codebook.  Proposal 4: Further study Type-2 HARQ-ACK codebook determination. |
| Samsung | More important for now is to identify bit savings from fields that have no impact on scheduling (e.g. C-RNTI, TPC, …) and determine the total number of bits.  If companies want to re-use FDRA/MCS/… on two cells, additional requirements are then needed such as evaluation of throughout loss through system simulations, description of solutions for operation with different SCS on different cells, … |

FL suggestions:

The below issues can be discussed after RAN1 agree to support the multi-cell scheduling DCI.

* HARQ-ACK codebook determination
* DAI design

## Other issues

Regarding other issues not mentioned above, companies are encouraged to provide comments in the table below.

|  |  |
| --- | --- |
| **Company** | **View** |
| Huawei | Although not in the scope, we also have results for the scenarios of more than 2 CCs, as in [3]. |
|  |  |

## Proposals for 1st GTW session

FL Proposal#2:

For the two-cell scheduling DCI, if supported, study below options for payload reduction:

* All the fields of the DCI can be divided into three types:
  + First type field: common to the two PDSCHs
  + Second type field: separate to the two PDSCHs
  + Third type field: common or separate to the two PDSCHs dependent on RRC configuration
* Other solutions are not precluded, e.g., using 2-stage DCI to schedule two PDSCHs on two carriers.

Regarding proposals above, companies are encouraged to provide comments in the table below.

|  |  |
| --- | --- |
| **Company** | **View** |
| Intel | Not sure if 2-stage DCI is in the scope. If not, prefer to not list it as example to minimize potential standardization efforts. |
| CATT | From our understanding, this proposal makes sense only if the two-cell scheduling DCI is supported. We don’t need ‘if supported’ in the main bullet. |
| Samsung | Need to first conclude whether or not 2-cell scheduling DCI is supported - no point for any other discussion. |
| Huawei | OK with FL proposal |
| OPPO | Agree with moderator’s proposal |
| MediaTek | Agree with moderator’s proposal. |
| Lenovo, Motorola Mobility | Agree with moderator’s proposal. |
| LG | Same view with Samsung.  Whether or not to support 2-cell scheduling by single DCI should be concluded first as per WID before proceeding discussions on any details. |
| Nokia, NSB | Probably no time to address these issues in the 1st GTW session, but would be good to have some outline of what the design principles are as an output of this meeting. Tend to think 2-stage DCI is not in scope. |

# References

1. [R1-2100111](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100111.zip) Discussion on Multi-cell PDSCH Scheduling via a Single DCI ZTE
2. [R1-2100187](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100187.zip) Discussion on multi-cell PDSCH scheduling via a single DCI OPPO

1. [R1-2100194](file:///D:\\RAN1\\RAN1%23104-e\\tdocs\\R1-2100194.zip) Discussion on multi-carrier scheduling using single PDCCH Huawei, HiSilicon
2. [R1-2100359](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100359.zip) Discussion on multi-cell PDSCH scheduling via a single DCI CATT
3. [R1-2100474](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100474.zip) Discussion on joint scheduling vivo
4. [R1-2100611](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100611.zip) On Multi-cell PDSCH Scheduling via Single DCI MediaTek Inc.
5. [R1-2100678](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100678.zip) On 2-cell scheduling via single DCI Intel Corporation
6. [R1-2100720](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100720.zip) On support of Single DCI scheduling two cells Nokia, Nokia Shanghai Bell
7. [R1-2100771](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100771.zip) Discussion on multi-cell PDSCH scheduling via a single DCI Lenovo, Motorola Mobility
8. [R1-2100886](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2100886.zip) Discussion on multi-cell PDSCH scheduling via a single DCI LG Electronics
9. [R1-2101089](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101089.zip) Discussion on multi-cell PDSCH scheduling via a single DCI ETRI
10. [R1-2101238](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101238.zip) Considerations for scheduling on two cells using a single DCI format Samsung
11. [R1-2101293](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101293.zip) On the support of single DCI scheduling multi-cell InterDigital, Inc.
12. [R1-2101363](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101363.zip) Views on Rel-17 DSS Multi-cell PDSCH scheduling via a single DCI Apple
13. [R1-2101491](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101491.zip) Multi-cell PDSCH scheduling via a single DCI Qualcomm Incorporated
14. [R1-2101562](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101562.zip) Study on single DCI scheduling PDSCH on multiple cells Ericsson
15. [R1-2101633](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101633.zip) Discussion on multi-cell PDSCH scheduling via a single DCI for NR DSS NTT DOCOMO, INC.
16. [R1-2101657](file:///D:\RAN1\RAN1%23104-e\tdocs\R1-2101657.zip) Discussion on multi-cell PDSCH scheduling via a single DCI ASUSTeK
17. R1-2101789 Discussion on Multi-cell PDSCH Scheduling via a Single DCI ZTE

# List of agreements:

## Agreements made in RAN1#103-e

Agreements:

Further study with below simulation assumptions:

Simulation scenarios:

* For two-cell scheduling via a single DCI, PDCCH transmitted on a first cell schedules one PDSCH on the first cell and another PDSCH on a second cell.
* For single-cell scheduling (baseline), one PDCCH transmitted on a first cell schedules one PDSCH on the first cell via self-scheduling and another PDCCH transmitted on the first cell schedules another PDSCH on a second cell via cross-carrier scheduling.
  + Companies can optionally compare to the case of PDCCH transmitted on each of the two cells via self-scheduling. In this case, company should provide details on how to calculate the PDCCH blocking rate.

Simulation assumptions on carrier frequency, SCS, antenna configuration, carrier bandwidth as well as CORESET configuration

* Combination 1: 2 GHz, 15 kHz SCS, 2 Tx, 2 Rx, 20 MHz carrier BW, 2-symbol CORESET with 96RBs
* Combination 2: 4 GHz, 30 kHz SCS, 4 Tx, 4 Rx, 100 MHz carrier BW, 1-symbol CORESET with 270RBs
* [Combination 3: 700MHz, 15 kHz SCS, 2 Tx, 2 Rx, 10 MHz carrier BW, 3-symbol CORESET with 48RBs]
* [Combination 4: 4GHz, 30 kHz SCS, 4 Tx, 4 Rx, 40 MHz carrier BW, 2-symbol CORESET with 96RBs]

Payload size of two-cell scheduling DCI (excluding CRC):

* 60 for single-cell scheduling DCI (baseline).
* 72/84/96/108 for two-cell scheduling DCI.
* Companies are encouraged to report how the values are obtained, e.g., via separate or shared fields in DCI format.

Target BLER for two-cell scheduling DCI: 1% (baseline), 0.5%(optional)

* ~~Option 1: 1%.~~
* ~~Supported by OPPO, vivo, Nokia, Qualcomm, CATT, Ericsson, Huawei, Lenovo, Intel, MediaTek~~
* ~~Option 2: 0.5%.~~
* ~~Supported by Samsung, LG~~

Regarding the CCE-to-REG mapping, based on the agreed interleaved CCE-to-REG mapping, whether to adopt non-interleaved CCE-to-REG mapping is up to the proponent.

Agreements:

* Further study with below simulation assumptions:

                     Table 2: System level simulation assumptions

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Carrier frequency | For scheduling cell, follow agreed link level simulation assumptions  For scheduled cell, consider 700MHz/2GHz with 10/20MHz BW (LTE overhead on DSS carrier can be optionally provided, up to proponent) |
| SCS |
| Simulation bandwidth |
| BS antenna height | 25 m |
| UE height | 1.5m |
| TRP transmit power | 46 dBm for 10MHz |
| Scenario | Urban Macro |
| ISD | 500m |
| TRP antenna configuration | (M,N,P,Mg,Ng;Mp,Np)= (1,2,2,1,1;1,1) for 700MHz  (M,N,P,Mg,Ng;Mp,Np)= (2,8,2,1,1;1,1) for 2GHz  (M,N,P,Mg,Ng;Mp,Np)= (8,4,2,1,1;1,1) for 4GHz |
| UE antenna configuration | (M,N,P,Mg,Ng;Mp,Np)= (1,1,2,1,1;1,1) for 700MHz/2GHz  (M,N,P,Mg,Ng;Mp,Np)= (1,2,2,1,1;1,1) for 4GHz |
| Device deployment | 80% indoor, 20% outdoor |
| UE speeds of interest | Indoor users: 3km/h |
| Outdoor users (in-car): 30 km/h |
| BS noise figure | 5 dB |
| BS antenna element gain | 8 dBi |
| UE noise figure | 9 dB |
| Thermal noise level | -174 dBm/Hz |
| Traffic | Full Buffer(baseline), FTP model 1 or 3 up to company |
| Macro sites | 19 |
| Number of UEs per cell | 10/15/20 UEs |
| Downtilt | 102° |
| Minimum BS to UE distance | 35m |

Agreements:

Further study multi-cell PDSCH scheduling via a single DCI with below simulation assumptions:

                                     Table 1: Link level simulation assumptions

|  |  |
| --- | --- |
| **Parameters** | **Values** |
| Carrier frequency | Option 1:  Inter-band CA (700MHz + 4GHz)  Intra-band CA (2GHz)    Option 2:  Only 4GHz is considered |
| SCS | 15 kHz for 700MHz/2GHz  30 kHz for 4GHz |
| Bandwidth | Option 1:  Baseline: PCell 10MHz + SCell 10/40MHz  Optional: PCell 20MHz + SCell 20/40/100MHz    Option 2:  Baseline: Scheduling cell 100 MHz  Optional: Scheduling cell 20 MHz |
| Channel model | TDL-C |
| Delay spread | 300 ns |
| Number of symbols for CORESET | [1], 2 or 3 |
| CORESET BW (contiguous PRB allocation) | 24/48/96 RBs depending on the bandwidth |
| CCE-to-REG mapping | Interleaved, [non-interleaved] |
| REG bundle size | 6 |
| Interleaver size | 2 |
| DCI payload size (excluding CRC) | Single PDSCH scheduling: 60 bits as baseline payload size  Multi-cell PDSCH scheduling: 72/84/96/104 bits |
| BLER target for multi-cell scheduling DCI | Option 1: 1%  Option 2: 0.5% |
| Number of BS antennas | 2 Tx for 700MHz/2GHz carrier frequency  4 Tx for 4GHz |
| Number of UE antennas | 2 Rx for 700MHz/2GHz carrier frequency  4 Rx for 4GHz carrier frequency |
| Modulation | QPSK |
| Channel coding | Polar code |
| UE speed | 3km/h |
| Aggregation level | 1/2/4/8/16 |
| Tx Diversity | One port precoder cycling |

Note 1: For two-cell scheduling via a single DCI, PDCCH transmitted on SCell schedules one PDSCH on the SCell and another PDSCH on PCell.

Note 2: For comparison, for single-cell scheduling, one PDCCH transmitted on SCell schedules one PDSCH on the SCell via self-scheduling and another PDCCH transmitted on the SCell schedules another PDSCH on PCell via cross-carrier scheduling.

Further discussion which rows are applicable to the scheduling cell/the scheduled cell for PDCCH

## Agreements made in RAN1#102-e

Agreements:

* Following scheduling combinations are allowed/not allowed when cross-carrier scheduling from an SCell to PCell/PSCell is configured
  1. self-scheduling on PCell/PSCell is allowed
  2. cross-carrier scheduling from PCell/PSCell to another SCell is not allowed
  3. self-scheduling on the ‘SCell used for scheduling PCell/PSCell’ is allowed
  4. cross-carrier scheduling from the ‘SCell used for scheduling PCell/PSCell’ to another serving cell is allowed
  5. cross-carrier scheduling from another serving cell to the ‘SCell used for scheduling PCell/PSCell’ is not allowed
* FFS: Search space and DCI format handling for the allowed cases above

Agreements:

* Configuring 2 or more Scells to schedule the PCell/PSCell is not allowed

Agreements:

* For the study on single DCI scheduling PDSCH on two cells
  + Consider the following scenarios as baseline for evaluation
    - UE configured with Inter-band CA with PCell and an SCell
      * PCell for the UE is operated on a DSS carrier (i.e., same carrier is also used for serving LTE users)
      * Case 1: Different SCS for PCell and SCell
      * Case 2: Same SCS for PCell and Scell
  + Additional scenarios can also be evaluated, e.g. as below
    - Intra-band CA case with multiple serving cells having same SCS (all cells operated on non DSS carriers)
    - Inter-band CA case with PCell and more than one SCell (at least the SCells are operated on non DSS carriers)
    - Note: other combinations not precluded
* Note: Further details of evaluation framework (including carrier BW, slot format etc.) to be discussed in next stage

# Miscellaneous (Low priority)

Regarding some low priority issues, companies’ views are summarized as below:

|  |  |
| --- | --- |
| Company | Key Proposals/Observations |
| Huawei, HiSilicon | Observation 12: Using single DCI scheduling multi-carriers has large potential to be deployed with the deployment scenario with 3 carriers and UL scheduling. |
| CATT | Proposal 2: Two TBs should be scheduled separately on different serving cells for multi-cell PDSCH scheduling via a single DCI. |
| vivo | Proposal 3. Clarify whether PUSCH multi-cell scheduling should be studied. |
| ZTE | Proposal 2: If TU permits, RAN1 considers one DCI scheduling two PDSCHs on the same carrier instead of one DCI scheduling two PDSCHs on two carriers. |
| MediaTek | Proposal 2: Continue to work on detailed design of multi-cell PDSCH scheduling via single DCI with the following design considerations.   * PDCCH blind decoding complexity is not worse than Rel-16 * Scalable DCI size based on the number of scheduled cells * Switch of same/different TDRA/FDRA across the scheduled cells * Forward compatibility to CA with more than 2 cells |
| ETRI | Observation 4: For multi-cell joint scheduling, scheduling more than two cells using a single DCI can be considered. |
| Nokia, Nokia Shanghai Bell | Proposal 1: Support multi-cell DCI in R17, focus on multiple SCell (2 or more) with the same/similar carrier size and SCS first. Strive to keep DCI format 1\_1 payload <106bits (including CRC). |

FL suggestions:

The below issues can be discussed after RAN1 agree to support the multi-cell scheduling DCI.

* Using two-stage DCI for scheduling multiple PDSCHs on multiple carriers
* Using a single DCI for scheduling multiple PUSCHs on multiple carriers
* Using a single DCI for scheduling multiple PDSCHs on same carrier
* Using a single DCI for scheduling more than 2 carriers