**[101-e--NR-5G\_V2X\_NRSL-SYNC-01]**

**Email discussion/approval regarding PSBCH content/TDD configuration indication**

* **Issue 1: Indication of TDD configuration**
* **Issue 2: SL-TDD-Config determination**
* **Issue 4: PSBCH contents and payload size (WAs confirmation)**

**By 5/29, with potential TP till 6/4 – Teng (CATT)**

**Issue 1 Indication of TDD configuration**

***FL Proposal:***

***Proposal 1: For indication of TDD configuration, the pattern(s) indication (X) and periodicity indication (Y) follows the two tables below:***

**Table 1. Periodicity indication Y with single TDD pattern (X=0)**

|  |  |  |
| --- | --- | --- |
| Periodicity indication Y | P (ms) | Single pattern |
|
| 0 | 0.5 | 0.5 |
| 1 | 0.625 | 0.625 |
| 2 | 1 | 1 |
| 3 | 1.25 | 1.25 |
| 4 | 2 | 2 |
| 5 | 2.5 | 2.5 |
| 6 | 4 | 4 |
| 7 | 5 | 5 |
| 8 | 10 | 10 |
| 9-15 | Reserved | |

**Table 2. Periodicity indication Y with two TDD patterns (X=1)**

|  |  |  |  |
| --- | --- | --- | --- |
| Periodicity indication Y | P+P2 (ms) | Two patterns | |
| P | P2 |
| 0 | 1 | 0.5 | 0.5 |
| 1 | 1.25 | 0.625 | 0.625 |
| 2 | 2 | 1 | 1 |
| 3 | 2.5 | 0.5 | 2 |
| 4 | 2.5 | 1.25 | 1.25 |
| 5 | 2.5 | 2 | 0.5 |
| 6 | 4 | 1 | 3 |
| 7 | 4 | 2 | 2 |
| 8 | 4 | 3 | 1 |
| 9 | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | 5 | 5 |
| 15 | 20 | 10 | 10 |

***Proposal 2: For indication of the granularity of UL resources,***

* ***If single pattern is configured, the granularity of the number of UL resources indicated by SL-TDD-Config is 1 slot.***
* ***If two patterns are configured, the granularity of the number of UL resources indicated by SL-TDD-Config follows the table below.***

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Periodicity indication Y | P+P2 (ms) | Two patterns | | **Granularity in slots with different SCS** | | | |
| P | P2 | 15kHz | 30 kHz | 60 kHz | 120 kHz |
| 0 | 1 | 0.5 | 0.5 | 1 | | | |
| 1 | 1.25 | 0.625 | 0.625 |
| 2 | 2 | 1 | 1 |
| 3 | 2.5 | 0.5 | 2 |
| 4 | 2.5 | 1.25 | 1.25 |
| 5 | 2.5 | 2 | 0.5 |
| 6 | 4 | 1 | 3 | 1 | | | 2 |
| 7 | 4 | 2 | 2 |
| 8 | 4 | 3 | 1 |
| 9 | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | 5 | 5 | 1 | | 2 | 4 |
| 15 | 20 | 10 | 10 | 1 | 2 | 4 | 8 |

***Proposal 3: For indication of the UL slots by Z,***

* ***If single patter is configured, Z bits indicate the UL slots;***
* ***If two patterns are configured, Z bits indicate the state index derived by the UL slots.***

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| --- | --- |
| **Company** | **Views** |
| Huawei, HiSilicon | We agree with Proposal 1 and 3, but have concern on Proposal 2 towards the scaled granularity. Our suggestions for Proposal 2 are below:  ***Proposal 2: For indication of UL resources,***   * ***Both the slot and number of symbols within a slot should be indicated by the sidelink reference SCS.*** * ***If single pattern is configured, the sidelink reference SCS is 120 kHz.*** * ***If two patterns are configured, the sidelink reference SCS is derived according to the table below:***  |  |  |  |  |  | | --- | --- | --- | --- | --- | | Periodicity indication Y | P+P2 (ms) | Two patterns | | SL reference SCS  (kHz) | | P | P2 | | 0 | 1 | 0.5 | 0.5 | 120 | | 1 | 1.25 | 0.625 | 0.625 | 120 | | 2 | 2 | 1 | 1 | 120 | | 3 | 2.5 | 0.5 | 2 | 120 | | 4 | 2.5 | 1.25 | 1.25 | 120 | | 5 | 2.5 | 2 | 0.5 | 120 | | 6 | 4 | 1 | 3 | 60 | | 7 | 4 | 2 | 2 | 60 | | 8 | 4 | 3 | 1 | 60 | | 9 | 5 | 1 | 4 | 60 | | 10 | 5 | 2 | 3 | 60 | | 11 | 5 | 2.5 | 2.5 | 60 | | 12 | 5 | 3 | 2 | 60 | | 13 | 5 | 4 | 1 | 60 | | 14 | 10 | 5 | 5 | 30 | | 15 | 20 | 10 | 10 | 15 |   From our understanding, we think both the slot and number of symbols should be indicated by the sidelink reference SCS. According to 38.213 specification, an UL slot is defined as a slot that includes only uplink symbols. These partial UL slots as UL slots also will be used for sidelink. For the rows indexed by Y=0 and Y=2~8 in single-pattern case and the rows indexed by Y=0~14 in two-pattern case, our proposal can give better indication granularity than the FL proposal. Indication of UL symbols potentially gives more accurate TDD configuration and provides more potential SL slots and symbols. One example is shown in below. |
| CMCC | Agree with proposal 1 and proposal 3.  For proposal 2, fine with the direction that different periodicity combinations using different indication granularity. In our view, using scaled granularity achieves better forward compatibility than different reference SCS considering more periodicity combinations may be introduced and the indication granularity may be some value like 3-slot, 5-slot…  However, as explained by HW, both full UL slot and partial UL slot/flexible slot should be considered as potential SL slots if partial slot satisfies the condition required by BWP configuration with sl-StartSymbol and sl-LengthSymbols. Therefore, to give better indication granularity, we suggest to use 60kHz as reference SCS for FR1 and 120kHz as reference SCS for FR2 regardless of SL SCS and proposal 2 can be modified as following:  ***Proposal 2: For indication of the granularity of UL resources,***   * ***60kHz is used as reference SCS for FR1 and 120kHz is used as reference SCS for FR2.*** * ***If single pattern is configured, the granularity of the number of UL resources indicated by SL-TDD-Config is 1 slot.*** * ***If two patterns are configured, the granularity of the number of UL resources indicated by SL-TDD-Config is as follows:***   + ***For FR1:***     - ***For periodicity combinations other than 5ms+5ms and 10ms+10ms, one-slot granularity is used;***     - ***For 5ms+5ms periodicity, two-slot granularity is used;***     - ***For 10ms+10ms periodicity, four-slot granularity is used.***   + ***For FR2:***     - ***For 0.5+0.5ms, 0.625+0.625ms, 1+1ms, 0.5+2ms, 2+0.5ms and 1.25+1.25ms periodicity combinations, one-slot granularity is used;***     - ***For 1+3ms, 3+1ms, 2+2ms, 1+4ms, 4+1ms, 2+3ms, 3+2ms and 2.5+2.5ms combinations, two-slot granularity is used;***     - ***For 5ms+5ms periodicity, four-slot granularity is used;***     - ***For 10ms+10ms periodicity, eight-slot granularity is used.*** |
| Intel | OK with proposals from FL |
| MediaTek | Agree with FL’s proposals |
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|  |  |

**Issue 2 SL-TDD-Config determination**

***FL Proposal: SL-TDD-Config in PSBCH is set to the same values in SIB provided by gNB***

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| --- | --- |
| **Company** | **Views** |
| Huawei, HiSilicon | It is preferable at this stage not to define new signaling at this stage if we can rely on proper network configuration instead, due to the overhead of transmitting the signaling and the standardization effort of designing it. If the flexibility of NW configuration is considered too extremely restrictive by operators, we would be interested to discuss how we can achieve better flexibility. |
| CMCC | Agree with FL’s proposal to flexibly accommodate diverse TDD configurations, i.e. sometimes DL-dominant configurations and sometimes UL-dominant configurations to adapt the changes of traffic load. |
| Intel | Agree with FL |
| MediaTek | Agree with FL’s proposal |
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|  |  |

**Issue 4 PSBCH contents and payload size**

RAN1#99 meeting

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Working assumption:   * PSBCH payload size is 56 bits including 24 bits of CRC.   Agreements:   * Note: “green” already earlier; “blue” new agreements, “brown” working assumption, “change marks” for updates  |  |  |  | | --- | --- | --- | | **PSBCH contents** | **Number of bits** | **Notes** | | DFN | 10 |  | | Indication of TDD configuration | 12 | System-wide information, e.g. TDD-UL-DL common configuration and/or potential SL slots | | Slot index | 7 | ~~Note: Up to 3 bits can be carried in DM-RS or in PBCH payload.~~ | | In-coverage indicator | 1 |  | | Reserve bits |  |  | | CRC | 24 |  | | Total bits | 56 |  | |

***FL Proposal: Confirm the working assumptions in RAN1#99 for the PSBCH contents for NR SL Rel-16, and reserve bits are 2***

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| --- | --- |
| **Company** | **Views** |
| Huawei, HiSilicon | Agree with the FL proposal. |
| CMCC | Agree with the FL proposal. |
| Intel | Propose to have configurable number of reserved bits and configurable values. |
| MediaTek | Agree with FL’s proposal |
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|  |  |