**[101-e--NR-5G\_V2X\_NRSL-SYNC-01]**

**Email discussion/approval regarding PSBCH content/TDD configuration indication**

* **Issue 1: Indication of TDD configuration**
* **Issue 2: SL-TDD-Config determination**
* **Issue 4: PSBCH contents and payload size (WAs confirmation)**

**By 5/29, with potential TP till 6/4 – Teng (CATT)**

**Issue 1 Indication of TDD configuration**

From the email responses 5/25-5/27, the feedbacks can be summarized as follows:

* For Proposal 1, all companies agree with the FL proposal.
* For Proposal 2, the FL proposal is to apply different slot granularity when two patterns are applied, which is only consider the slots with all UL symbols. Different views from 3 companies proposed to also consider the partial UL slots for potential SL transmission and applying reference SCS 60kHz and 120kHz for FR1 and FR2 respectively. There is also a suggestion to use equation instead of chart to demonstrate the various granularities. 2 companies proposed to pre-configure the certain number of TDD configuration when two patterns are used.
* For proposal 3, the principle is supported by majority companies, and the second bullet on how to use Z to indicate two patterns should be clarified with more details. On the other hand, 3 companies proposed to use (pre-)configured set and index to indicate different states when two patterns are applied. By consuming another 1 bit of Z (7 bits) to indicate lower granularity UL slots seems not quite worthy.

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| **Proposal 1** | **Companies** |
| Support | [Huawei, HiSilicon] [CMCC] [Intel] [MediaTek] [ZTE, Sanechips] [OPPO] [vivo] [Ericsson] [Nokia] [Qualcomm] [LGE] [Samsung] [NTT DOCOMO] [Apple] |
| NOT support |  |

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| **Proposal 2** | **Companies** |
| Support | [Intel] [MediaTek] [ZTE, Sanechips] [vivo] [Nokia] [Samsung] [NTT DOCOMO] [Apple] |
| NOT support | [OPPO] |
| Partial slot | [Huawei, HiSilicon] [CMCC] [LGE] |
| Pre-configuration | [Ericsson] [Qualcomm] |

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| **Proposal 3** | **Companies** |
| Support | [Huawei, HiSilicon] [CMCC] [Intel] [MediaTek] [OPPO] [Samsung] [NTT DOCOMO] [Apple] |
| NOT support | [ZTE, Sanechips] |
| Pre-configuration | [Ericsson] [Nokia] [Qualcomm] |

* For proposal 1, I would like to take the FL proposal as potential consensus.
* For proposal 2, there are three alternatives now. From my understanding, Alt 1 as in my previous proposal is considered.
* **Alt 1**: Indicate slots which all the symbols in the slot are UL symbols. The partial UL slots are not included in the TDD indication of PSBCH.
* **Alt 2**: Considering and indicating both UL slots and partial UL slots in the TDD indication of PSBCH. Different SL reference SCSs are used for one pattern and two patterns separately.
* **Alt 3**: Pre-configure the certain number of TDD configuration when two patterns are used
* For proposal 3, the details on Z of two patterns are further proposed.

***Potential Consensus:***

***Proposal 1: For indication of TDD configuration, the pattern(s) indication (X) and periodicity indication (Y) follows the two tables below:***

**Table 1. Periodicity indication Y with single TDD pattern (X=0)**

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| Periodicity indication Y | P (ms) | Single pattern |
|
| 0 | 0.5 | 0.5 |
| 1 | 0.625 | 0.625 |
| 2 | 1 | 1 |
| 3 | 1.25 | 1.25 |
| 4 | 2 | 2 |
| 5 | 2.5 | 2.5 |
| 6 | 4 | 4 |
| 7 | 5 | 5 |
| 8 | 10 | 10 |
| 9-15 | Reserved | |

**Table 2. Periodicity indication Y with two TDD patterns (X=1)**

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| --- | --- | --- | --- |
| Periodicity indication Y | P+P2 (ms) | Two patterns | |
| P | P2 |
| 0 | 1 | 0.5 | 0.5 |
| 1 | 1.25 | 0.625 | 0.625 |
| 2 | 2 | 1 | 1 |
| 3 | 2.5 | 0.5 | 2 |
| 4 | 2.5 | 1.25 | 1.25 |
| 5 | 2.5 | 2 | 0.5 |
| 6 | 4 | 1 | 3 |
| 7 | 4 | 2 | 2 |
| 8 | 4 | 3 | 1 |
| 9 | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | 5 | 5 |
| 15 | 20 | 10 | 10 |

***FL proposal:***

***Proposal 2: For indication of the granularity of UL resources,***

* ***If single pattern is configured, the granularity of the number of UL resources indicated by SL-TDD-Config is 1 slot.***
* ***If two patterns are configured, the granularity of the number of UL resources indicated by SL-TDD-Config follows the table below.***

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| Periodicity indication Y | P+P2 (ms) | Two patterns | | **Granularity in slots with different SCS** | | | |
| P | P2 | 15kHz | 30 kHz | 60 kHz | 120 kHz |
| 0 | 1 | 0.5 | 0.5 | 1 | | | |
| 1 | 1.25 | 0.625 | 0.625 |
| 2 | 2 | 1 | 1 |
| 3 | 2.5 | 0.5 | 2 |
| 4 | 2.5 | 1.25 | 1.25 |
| 5 | 2.5 | 2 | 0.5 |
| 6 | 4 | 1 | 3 | 1 | | | 2 |
| 7 | 4 | 2 | 2 |
| 8 | 4 | 3 | 1 |
| 9 | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | 5 | 5 | 1 | | 2 | 4 |
| 15 | 20 | 10 | 10 | 1 | 2 | 4 | 8 |

***FL proposal:***

***Proposal 3: For indication of the UL slots by Z,***

* ***If single patter is configured, Z bits indicate the UL slots;***
* ***UL slot number in the pattern=***
* ***If two patterns are configured, Z bits indicate the state index derived by the UL slots.***
* ***UL slot number in the first pattern=***
* ***UL slot number in the second pattern=***

***Where is the periodicity in units of ms of the second pattern, w is the granularity of resource indication and u=0/1/2/3 corresponds to the 15/30/60/120 kHz SCS for SL respectively.***

**Comments 5/28-5/29**

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| **Company** | **Views** |
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**Email responses 5/25-5/27**

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| **Company** | **Views** |
| Huawei, HiSilicon | We agree with Proposal 1 and 3, but have concern on Proposal 2 towards the scaled granularity. Our suggestions for Proposal 2 are below:  ***Proposal 2: For indication of UL resources,***   * ***Both the slot and number of symbols within a slot should be indicated by the sidelink reference SCS.*** * ***If single pattern is configured, the sidelink reference SCS is 120 kHz.*** * ***If two patterns are configured, the sidelink reference SCS is derived according to the table below:***  |  |  |  |  |  | | --- | --- | --- | --- | --- | | Periodicity indication Y | P+P2 (ms) | Two patterns | | SL reference SCS  (kHz) | | P | P2 | | 0 | 1 | 0.5 | 0.5 | 120 | | 1 | 1.25 | 0.625 | 0.625 | 120 | | 2 | 2 | 1 | 1 | 120 | | 3 | 2.5 | 0.5 | 2 | 120 | | 4 | 2.5 | 1.25 | 1.25 | 120 | | 5 | 2.5 | 2 | 0.5 | 120 | | 6 | 4 | 1 | 3 | 60 | | 7 | 4 | 2 | 2 | 60 | | 8 | 4 | 3 | 1 | 60 | | 9 | 5 | 1 | 4 | 60 | | 10 | 5 | 2 | 3 | 60 | | 11 | 5 | 2.5 | 2.5 | 60 | | 12 | 5 | 3 | 2 | 60 | | 13 | 5 | 4 | 1 | 60 | | 14 | 10 | 5 | 5 | 30 | | 15 | 20 | 10 | 10 | 15 |   From our understanding, we think both the slot and number of symbols should be indicated by the sidelink reference SCS. According to 38.213 specification, an UL slot is defined as a slot that includes only uplink symbols. These partial UL slots as UL slots also will be used for sidelink. For the rows indexed by Y=0 and Y=2~8 in single-pattern case and the rows indexed by Y=0~14 in two-pattern case, our proposal can give better indication granularity than the FL proposal. Indication of UL symbols potentially gives more accurate TDD configuration and provides more potential SL slots and symbols. One example is shown in below. |
| Huawei, HiSilicon | **Based on companies’ views, we would like to give some further clarifications**  We share the same view of CMCC and LGE that the partial UL slot should be considered to provide more potential SL resources. Under this assumption, the reference SCS can give better indication resolution. If the “scaled granularity” is the only concept to be used, then there will be no UL slots to be indicated in our exemplary figure. To address this issue especially in small period cases, we believe the “SL reference SCS” should be additionally utilized.  Considering this discussion still goes to some type complex situation. We think the proposal from CMCC e.g. “SL reference SCS” plus “scaled granularity” manner give some compromise way to move forward in principle. A relatively large SL reference SCS can be provided first, then the “scaled granularity” method is applied based on one slot corresponding to the “SL reference SCS”.  Some clarification from our figures in the below:  For companies’ better understanding, and indicate the number of UL slots based on SL reference SCS. The superscripts “SL” are used to differentiate from the Uu RRC parameters and . Since the SL reference SCS is 120kHz in the figure, indicating these UL slots does not contradict the agreement that Z=7 bits indicate the UL slots. |
| CMCC | Agree with proposal 1 and proposal 3.  For proposal 2, fine with the direction that different periodicity combinations using different indication granularity. In our view, using scaled granularity achieves better forward compatibility than different reference SCS considering more periodicity combinations may be introduced and the indication granularity may be some value like 3-slot, 5-slot…  However, as explained by HW, both full UL slot and partial UL slot/flexible slot should be considered as potential SL slots if partial slot satisfies the condition required by BWP configuration with sl-StartSymbol and sl-LengthSymbols. Therefore, to give better indication granularity, we suggest to use 60kHz as reference SCS for FR1 and 120kHz as reference SCS for FR2 regardless of SL SCS and proposal 2 can be modified as following:  ***Proposal 2: For indication of the granularity of UL resources,***   * ***60kHz is used as reference SCS for FR1 and 120kHz is used as reference SCS for FR2.*** * ***If single pattern is configured, the granularity of the number of UL resources indicated by SL-TDD-Config is 1 slot.*** * ***If two patterns are configured, the granularity of the number of UL resources indicated by SL-TDD-Config is as follows:***   + ***For FR1:***     - ***For periodicity combinations other than 5ms+5ms and 10ms+10ms, one-slot granularity is used;***     - ***For 5ms+5ms periodicity, two-slot granularity is used;***     - ***For 10ms+10ms periodicity, four-slot granularity is used.***   + ***For FR2:***     - ***For 0.5+0.5ms, 0.625+0.625ms, 1+1ms, 0.5+2ms, 2+0.5ms and 1.25+1.25ms periodicity combinations, one-slot granularity is used;***     - ***For 1+3ms, 3+1ms, 2+2ms, 1+4ms, 4+1ms, 2+3ms, 3+2ms and 2.5+2.5ms combinations, two-slot granularity is used;***     - ***For 5ms+5ms periodicity, four-slot granularity is used;***     - ***For 10ms+10ms periodicity, eight-slot granularity is used.***   [CMCC-2]  Based on companies’ views, we would like companies to further check whether partial UL slot can be considered as potential SL resources if SL BWP configuration condition is met with regard to the start and number of SL symbols. In our view, we do not see a reason to exclude the partial UL slot and regarding to ZTE’s comments towards the wording “UL slot” in the agreement of last meeting, we understand it’s something like “virtual UL slot” which is used to derive available SL resources, so indicating partial UL slot with the restriction of SL start symbol and length as “virtual UL slot” does not contradict the agreement (please correct me if I understand it incorrectly).  As to how partial UL slot can be indicated as “virtual UL slot”, we are open to discuss any of the following alternatives:   1. Based on gNB’s implementation if FL proposal in Issue 2 is agreed; 2. “SL reference SCS” plus “scaled granularity” manner as proposed by HW |
| Intel | OK with proposals from FL |
| MediaTek | Agree with FL’s proposals |
| ZTE/Sanechips | *Proposal 1*: Agreed  *Proposal2*: We agree with the FL proposal 2 on the slot number granularity measured by the SCS of SL BWP or, alternatively put, 'equivalent slot' measured by a scaled reference SCS for indication purpose as elaborated in HW/HiSi/CMCC proposals. This granularity in slots measured by the SCS of SL BWP in FL proposal is reasonably derived from the indication capability of 7 bits and aligned with that in R1-2003574. However, as additionally pointed out in R1-2003574, there are 5 cases, i.e. pattern periodicities (P, P2) being one of {(1,3),(1,4),(2,2),(3,1),(4,1)} (corresponding to row 6,7,8,9,13 in the table in FL proposal) with SCS of SL BWP equal to 120kHz that 1 remainder bit could be leveraged to further indicate the slot number less than the granularity, we believe this remainder slot should be put into use to further cover 64 more slot patterns under the corresponding 5 cases. We put our thinking on how to leverage the remainder bit in our feedback to proposal 3.  **To HW/HiSi, CMCC**  Agreements:   * *For indication of TDD configuration:* * *X=1 bit indicates the number of patterns*   + *Value 0 indicates one pattern is used.*   + *Value 1 indicates two patterns are used.* * *Y=4 bits indicate the periodicity information*   + *When one pattern is used, Y indicates the periodicity of the pattern.*   + *When two patterns are used, Y jointly indicates the periodicities of the two patterns.* * *Z=7 bits indicate the UL slots*   + *UL slots are jointly indicated by 7 bits when two patterns are configured.*   + *FFS other details.*   During the last meeting, ZTE/Sanechips was the only proponent of using 'potential SL slots' to replace 'UL slots' as the wording in the agreement above. We believe the 'potential SL slots' is an accurate term and does not preclude the symbol level indication as shown in HW/HiSi's illustrative figure (hopefully you don't mind my copying below to better deliver our idea). Clearly the (10,5) UL symbols in the UL slot measured by the 15kHz SCS of UL BWP within both patterns could be transformed into (5,2) potential SL slots measured by the 120kHz reference SCS for indication purpose. Presumably the first 5 potential SL slots could be put into use if the required symbol length for sidelink transmission is less than 10 within a slot measured by the SCS of SL BWP(If we further assume the SCS of SL BWP equals to UL BWP). But the agreement was made and we don't think your proposals are still within the scope of the agreement for the following reasons.    The fundamental difference between the FL proposal and your proposals is that if we transform the slot number granularity in FL proposal into the reference SCS for indication as in your proposals, the reference SCS (and its corresponding numerology) should not be larger than the reference SCS of the SL BWP. This ensures the 'UL slots' is indicated as the agreement requires.  *Proposal 3*: As clarified in our feedback to proposal 2. We believe the remainder bit should/could be used for further indication of slot number less than the granularity.  ***For indication of the UL slots by Z,***   * ***If single patter is configured, Z bits indicate the UL slots;*** * ***If two patterns are configured, Z bits indicate the state index derived by the UL slots.***   ***- 1 bit should be used to indicate UL slots less than the granularity under the cases where pattern periodicities (P, P2) are one of {(1,3),(1,4),(2,2),(3,1),(4,1)} and SCS of SL BWP is 120kHz.***  [ZTE/Sanechips - 02]  **Just to clarify, we do not the object to indicating partial slot.** In fact, our preference to proposal 3 is to use the 7 bits to indicate remainder slots which could include the partial slot and we believe this is good from resource utilization/indication capability perspetive. **We just don’t see the need to use a reference SCS for indication purpose that is larger than the SCS of SL BWP for the purpose of indicating partial slot or symbol level indication as mentioned in some companies’ replies/contributions**, e.g. using 120kHz as the reference for indication when the SCS for SL BWP is 60kHz. **We believe it’s violating the agreement given the UL slots are agreed to be indicated, not the symbol level information within a UL slot nor an equivalent potential SL slot meausred by a reference SCS larger than the SCS of SL BWP.** |
| OPPO | Agree with proposal 1and 3.  For proposal 2, we propose to use 15kHz and 60kHz as referenceSubcarrierSpacing to determine the UL slot boundary which is indicated by PSBCH in FR1 and FR2 respectively.  In that case, only two cases cannot be indicated within Z=7 bits for 2 patterns, they are 10ms and 20ms periodicity case (highlight part in the table below). In these two special cases, 30kHz SCS and 15kHz SCS are used as referenceSubcarrierSpacing respectively. |
| Vivo | Proposal1: agree  Proposal2: agree.  Firstly, in Uu, there can be multiple SCSs configured in the same frequency, the activated SCS may change over time. To accommodate to the switched BWP/SCS, \ reference SCS is defined for Uu. However, in NR SL, there is no such motivation given that there is only 1 SL BWP on a carrier and the SCS is fixed.  Secondly, introducing SL reference SCS seems to be redundant if the indication granularity is defined. Using SL reference SCS as well as coarse granularity is equivalent to use a fine-grained resource indication. Moreover, always having candidate SL resources(UL resources) defined in SL reference SCS such as 60kHz and 120kHz have an impact on SL resource pool (pre-)configuration. It will force the SL resource bitmap to be (pre)configured in SL reference SCS instead of SL SCS, which will unnecessarily increase the signaling overhead especially when the SL SCS is small.  Thirdly, the agreement clearly said the SL-TDD-Config indicates the number of UL slot, so partial UL slots should be precluded.  Proposal3: agree    [vivo-2]  Given the SL SCS in the Huawei’s figure is 15kHz, I suppose it is for FR1, then I am confused why the SL reference SCS is set to 120kHz which is not allowed in FR2. It would be more reasonable to assume the SL BWP SCS is 60kHz or 120kHz and then the benefits of using 120kHz diminish or even disappear as up to one additional slot in 120kHz can be indicated.  Moreover, even if 120kHz could be used as reference SCS in FR1, and 5 UL slots+2 UL slots in 120kHz are indicated by the PSBCH when SL SCS is 15kHz. UE still needs to convert them into 15kHz (as shown in step2 in figure below) to derive the resource pool as each bit in the pool bitmap correspond to a SL slot. In this case, the merit of indicating additional resources in 120kHz disappear. If the SL BWP is configured with startsymbol=1, then it is impossible to utilize the blue part for SL pool although PSBCH indicates them. So the reference SCS only introduce additional complexity but cannot improve the resource utilization.    Or, as we commented in the first round, do you assume the bitmap should be more precise in this case, e.g., each bit should correspond to a slot in SL reference SL? Structure didn't discuss the possibility either. Worse still, it also means the bitmap overhead will be 8 times of that in SL SCS and the bitmap contains a large amount of redundant ‘1’ and ‘0’ due to SCS scaling. |
| Ericsson | Proposal 1: Agree.  Proposal 2: we believe that it is essential that the gNB has a way of configuring any pattern of its choice because we do not know at this point the type of patterns selected for real deployments. Therefore, we propose to pre-configure a certain number of TDD-UL-DL configurations in the case of two patterns.  Proposal 3: we are fine with the first bullet. For the second bullet, the terminology state index is not clear for us. We believe that for the case of two patterns, Z bits may sometimes indicate pre-configured pattern(s). |
| Nokia | Proposal 1: Agree  Proposal 2: Agree  Proposal 3: Like noted by Ericsson, maybe we should clarify bit how shall we determine the state index. E.g. the use of the arimethic shift operation used to dynamically allocate the bit for each pattern. |
| Qualcomm | We agree with proposal 1.  For proposal 2, we share the view that pre-configuring a set of patterns and indexing into it is simple and provides flexibility for the network.  For proposal 3, we think that indexing into a pre-configured set should be used at least for the two pattern case. For the single-pattern case, we’re ok with number of slots or with an index into a set.  In our view, indication should cover as many patterns as possible and with as fine granularity as possible for each SCS. We don’t think that using a reference SCS would achieve both goals. |
| LGE | Proposal 1 is supported.  As for proposal 2, I agree with Huawei/HiSilicon and CMCC that the partial UL slot needs to be used as SL slot if SL BWP configuration condition is met with regard to the start and number of SL symbols.  A slot that contains at least *Y*-th, (*Y*+1)-th, ..., (*Y*+*X*-1)-th UL symbols, where *X* and *Y* are *sl-LengthSymbols* and *sl-StartSymbol* respectively, is indicated as UL slot by SL-TDD-Config in PSBCH.  If the above condition is met, there is no granularity issue with FL proposal on signaling the number of SL slots.  As for the proposal 3, we need to finalize the details in this meeting. The proposal 3 is supported with the following Z values for the two patterns case.   |  |  |  | | --- | --- | --- | | *Z value* | *#UL slots in P1* | *#UL slots P 2* | | *0, …, NP2-1* | *0* | *1,…, NP2* | | *NP2, …, 2\* NP2* | *1* | *0,…, NP2* | | *2\* NP2+1, …, 3\* NP2+1* | *2* | *0,…, NP2* | | *…* | *…* | *…* | | *k\* NP2+k-1, …, (k+1)\* NP2+k-1* | *k* | *0,…, NP2* | | *…* | *…* | *…* | | *NP1\* NP2+ NP1-1, …, ( NP1+1)\* NP2+ NP1-1* | *NP1* | *0,…, NP2* |   Where *NP1 and NP2 are the maximum number of UL slots in pattern 1 and 2 respectively for given X and Y values.* |
| Samsung | Agree with FL’s proposals, generally. As other company mentioned, reference subcarrier spacing does not provide any further benefits rather than ‘granularity’ concept in view of forward compability and flexibility. Furthermore, agreement does not say other than slot indication literally. Actually, proposal 2 could be generalized as a ‘simple’ equation to include all possible cases for potential periodicity and combiniation for future release. |
| NTT DOCOMO | We support the FL’s proposal. Regarding reference SCS, it seems to be optimization and unnecessary since symbol-level indication is impossible for the reference SCS itself. |
| Apple | We support proposals 1 and 2. For proposal 3, we are fine with the first bullet, and think the second bullet needs clarification on “state index”. |

**Issue 2 SL-TDD-Config determination**

From the email responses 5/25-5/26, the FL proposal is understood in different ways. I would like to have more clarification. *TDD-UL-DL-ConfigCommon* is configured to UE by network, and it indicates symbol level resources to UE. SL TDD Configuration (X/Y/Z) is carried in PSBCH, and only 12 bits can be used for limited indication on the slot level UL resources that can be used for SL. On which side SL TDD Configuration can be derived from *TDD-UL-DL-ConfigCommon*, UE side or network side?

* Option 1:SL TDD Configuration is derived from *TDD-UL-DL-ConfigCommon* on **UE side**.
* **Pros**: No new RRC signaling is introduced.
* **Cons**: Additional derivation rules are needed; significant physical spec effort/change is needed; high complexity for UE implementation; rules are various according to different TDD configurations.
* Option 2: SL TDD Configuration is derived from *TDD-UL-DL-ConfigCommon* on **Network side**.
* **Pros**: The derivation/conversion from *TDD-UL-DL-ConfigCommon* to SL TDD Configuration is done at network side; low implementation cost at UE side; no specs impact; good forward compatibility.
* **Cons**: New parameter in SIB is needed.

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| **Option** | **Companies** |
| Option 1 | [Huawei, HiSilicon] [ZTE, Sanechips] [OPPO] [Nokia] |
| Option 2 | [CMCC] [Intel] [MediaTek] [vivo] [Ericsson] [CATT] [Qualcomm] [LGE] [Samsung] [Sharp] [NTT DOCOMO] |

My suggestion is to leave the complexity and derivation at NW side. A new SIB parameter is introduced, e.g. *SL-TDD-Config*, which is directly indicating the X/Y/Z. NW indicates both *TDD-UL-DL-ConfigCommon* and *SL-TDD-Config* to SL UE by SIB, and UE set the TDD configuration field (12 bits) in PSBCH by simply copy it from *SL-TDD-Config*.

***FL proposal:***

* ***A new SIB parameter, e.g. SL-TDD-Config, is introduced to indicate the “indication of TDD configuration” in PSBCH.***

**Comments 5/28-5/29**

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| **Company** | **Views** |
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**Email responses 5/25-5/27**

*FL Proposal: SL-TDD-Config in PSBCH is set to the same values in SIB provided by gNB*

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| **Company** | **Views** |
| Huawei, HiSilicon | It is preferable at this stage not to define new signaling at this stage if we can rely on proper network configuration instead, due to the overhead of transmitting the signaling and the standardization effort of designing it. If the flexibility of NW configuration is considered too extremely restrictive by operators, we would be interested to discuss how we can achieve better flexibility. |
| CMCC | Agree with FL’s proposal to flexibly accommodate diverse TDD configurations, i.e. sometimes DL-dominant configurations and sometimes UL-dominant configurations to adapt the changes of traffic load. |
| Intel | Agree with FL |
| MediaTek | Agree with FL’s proposal |
| ZTE/Sanechips | We don't think this signaling is necessary. This signaling, if introduced, would require a major update of the WA under phystructure.  To our understanding, the intention of the signaling is to indicate convey the slot information in PSBCH in case its contents on slot information differs from that in TDD-UL-DL-ConfigCommon. Thus this signaling may be useful under 13 cases as shown in table A in appendix of R1-2003574. We think the flexibility of NW is a serious issue if the UL slots conveyed in PSBCH could be arbitrarily different from those in TDD-UL-DL-ConfigCommon and the limited Rx RPs are supposed to contain the slot patterns in both PSBCH and TDD-UL-DL-ConfigCommon. But we would say the flexibility of NW is sufficient if 7 bits in PSBCH is utilized to the fullest extent as in our feedback to proposal 3 under issue 1 and the following is mandated.  The UL slot(s) derived by out of coverage UE from PSBCH should be aligned with that derived by in coverage UE from *TDD-UL-DL-ConfigCommon* |
| OPPO | Agree. There is no need to introduce additional RRC signaling. SL-TDD-config can be derived at UE side based on SIB from gNB. |
| vivo | Agree.  As discussed before, transformation from TDD configuration in SIB1 to SL-TDD-Config and vice versa may be required due to limited PBSCH payload size. However, if such transformations are done by UE, additional rules to derive SL-TDD-Config must be specified in the spec, which will introduce higher complexity of UE implementation as well as significant spec efforts. We prefer to leave the complexity to gNB and UE just set the SL-TDD-Config to the same value provided by SL SIB. |
| Ericsson | We agree with the principle behind the proposal. However, it may happen that the TDD-UL-DL-ConfigCommon from Uu indicates one of the patterns which is not supported as indicated in Issue 1 for PSBCH. To avoid this, we suggest to have pre-configurable patterns. |
| Nokia | We agree that there should not be need to introduce additional signaling. However there should not be need to restrict NR-Uu allocation to comply with SL-TDD-Config range. The slot value in SL-TDD-Config should simply be largest possible value (among the possible slot index space) that is smaller or equal to the value given in tdd-UL-DL-ConfigurationCommon. |
| CATT | FL proposal is agreed in principle.  This issue is also being discussed in Issue C of PHY structure Thread 02, and these two discussions should keep alignment.  When the translation between TDD-UL-DL-configComm and SL-UL-DL\_ConfigCommon is processed at UE side, extra specification effort is needed. When the translation is processed at gNB side, a new RRC parameter shuld be introduced, but it is same as that in PSBCH. In order to have less spec effort and less complexity on UE, it is preferred to use a new RRC parameter to indicate the SL-UL-DL\_ConfigCommon. |
| Qualcomm | If the proposal is that a dedicated parameter in SIB is used to set the value of the TDD indication in PSBCH, we support it.  The comments from companies seem to have conflicting interpretations of the proposal. |
| LGE | Further clarification is needed on what SIB means in the FL proposal text. We prefer to define a new parameter TDD-ConfigSL that is configured by the network to be carried as SL-TDD-Config in PSBCH. This parameter is inevitable for out-of-coverage UE operation. With this parameter, the network is able to have more flexibility in restricting UL slots possibly used for SL slot, compared to applying a resource pool bitmap over TDD-UDL-DL-ConfigCommon.  In addition, a slot that contains UL symbols and satisfies SL BWP configuration condition needs to be available for SL slot.  In this sense, the FL proposal can be further clarified as follows.  **FL proposal:**   * Introduced a new parameter for configuring SL-TDD-Config in PSBCH * A slot that contains at least *Y*-th, (*Y*+1)-th, ..., (*Y*+*X*-1)-th UL symbols, where *X* and *Y* are *sl-LengthSymbols* and *sl-StartSymbol* respectively, is indicated as UL slot by SL-TDD-Config in PSBCH. |
| Samsung | Agree with motivation from FL. But, we are not sure what “same value” means in the proposal. Actually, if the intention is just reusing Uu TDD information to determine SL-TDD-Config, it is better to say as following.  *- SL-TDD-Config in PSBCH is determined based on SIB provided by gNB* |
| Sharp | The proposal itself is ambiguious to us. Which SIB does it refer to, SIB1 or SIB12? If it refers to SIB1, we suppose it’s same with LTE V2X and we support the FL proposal. |
| NTT DOCOMO | The direction should be OK, but proposal 2 should be considered, shouldn’t it? For example, a part of possible values of SL-TDD-Config in PSBCH is 4 slots and 6 slots, and SIB indication is 5 slots, then 4 slots should be indicated. In that sense, ‘same’ is not proper term, we think. |

**Issue 4 PSBCH contents and payload size**

RAN1#99 meeting

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| Working assumption:   * PSBCH payload size is 56 bits including 24 bits of CRC.   Agreements:   * Note: “green” already earlier; “blue” new agreements, “brown” working assumption, “change marks” for updates  |  |  |  | | --- | --- | --- | | **PSBCH contents** | **Number of bits** | **Notes** | | DFN | 10 |  | | Indication of TDD configuration | 12 | System-wide information, e.g. TDD-UL-DL common configuration and/or potential SL slots | | Slot index | 7 | ~~Note: Up to 3 bits can be carried in DM-RS or in PBCH payload.~~ | | In-coverage indicator | 1 |  | | Reserve bits |  |  | | CRC | 24 |  | | Total bits | 56 |  | |

From the email responses 5/25-5/26, majority companies agree to confirm the working assumptions in the above agreements, while one company suggests having configurable number of reserved bits and configurable values. For me by this stage, I suggest to following majority views.

***FL Proposal***

* ***Confirm the working assumptions in RAN1#99 for the PSBCH contents for NR SL Rel-16, and reserve bits are 2.***

**Comments 5/28-5/29**

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| **Company** | **Views** |
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**Email responses 5/25-5/27**

*FL Proposal: Confirm the working assumptions in RAN1#99 for the PSBCH contents for NR SL Rel-16, and reserve bits are 2*

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| --- | --- |
| **Company** | **Views** |
| Huawei, HiSilicon | Agree with the FL proposal. |
| CMCC | Agree with the FL proposal. |
| Intel | Propose to have configurable number of reserved bits and configurable values. |
| MediaTek | Agree with FL’s proposal |
| ZTE/Sanechips | Agreed |
| OPPO | Agree |
| Vivo | agree |
| Ericsson | Agree with the proposal and confirm the WA. |
| Nokia | Agree |
| CATT | Agree with the FL proposal. |
| Qualcomm | Agree |
| LGE | Supported. |
| Samsung | Agree |
| Sharp | Agree. |
| NTT DOCOMO | Agree |
| Apple | Agree |