**[100b-e-NR-5G\_V2X\_NRSL-SYNC-01]**

**Email discussion/approval related to PSBCH contents - indication of TDD configuration**

[100b-e-NR-5G\_V2X\_NRSL-SYNC-01] Email discussion/approval related to PSBCH contents - Indication of TDD configuration

(a,k.a. issue 1-1) by 4/24, with potential TPs by 4/29 (CATT, Teng)

**Issue 1-1 Indication of TDD configuration**

**4/30**

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| Agreements:   * For indication of TDD configuration: * X=1 bit indicates the number of patterns   + Value 0 indicates one pattern is used.   + Value 1 indicates two patterns are used. * Y=4 bits indicate the periodicity information   + When one pattern is used, Y indicates the periodicity of the pattern.   + When two patterns are used, Y jointly indicates the periodicities of the two patterns. * Z=7 bits indicate the UL slots   + UL slots are jointly indicated by 7 bits when two patterns are configured.   + FFS other details. |

**4/20-4/23**

From the email responses 4/20-4/23, the preference on the TDD indication can be summarized as following table.

* For X and Y, two alternatives are discussed. X and Y indicate pattern and periodicity separately or jointly.
* For Z, now I see many companies think that 8 bits can provide much more flexibility on the indication of UL slots, while 7 bits cannot, especially for FR2 120kHz. Whether Z=7 or 8 bits is also related to the total TDD bits in PSBCH and how X and Y are used.
* Reserve bits, few companies expressed the concerns on taking one bit from the reserve bit is not applicable, since there is only 2 reserve bits in PSBCH.

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| **Alternatives** | **Overhead** | **Indication of Slot/symbol-level timing** | **Supporting companies** |
| Alt. 1 | 12 bits | 1bit (Pattern) + 4bits (Periodicity) + 7bits (UL slots) | [Huawei, HiSilicon] [ZTE] [Spreadtrum] [Ericsson] [LGE] [MediaTek] [Intel] [Fujitsu] [DOCOMO] |
| Alt. ~~2~~ 4 | 5bits (Pattern + Periodicity) + 7bits (UL slots) | [OPPO][Qualcomm] |
| Alt. 3 | 4bits (Pattern + Periodicity) + 8bits (UL slots) | [Samsung] |
| Alt. ~~4~~ 2 | 13 bits | 1bit (Pattern) + 4bits (Periodicity) + 8bits (UL slots) | [CMCC][Huawei, HiSilicon] [Spreadtrum] [Apple] [Nokia] |
| Alt. 5 | 5bits (Pattern + Periodicity) + 8bits (UL slots) | [vivo] |

I propose the following alternatives for further discussion and potential down-selection.

* For X and Y, how they can be used for indication is easy to wording in the proposal.
* For Z, a principle wording can be agreed first, and the details can be discussed during the TP stage.

**4/23-4/24**

Based on the three alternatives below, companies had detailed discussion, and the supported solutions are quite different. Besides the following three alternatives, there are still some companies prefer to have other indication combination as shown in above table.

The current situation can be summarized below, and there are 5 combinations that are supported by companies.

* For indication of TDD configuration:
* For X and Y
* Opt 1: X=1 bit, Y=4 bits
* Opt 2: X=0, Y=4 bits
* Opt 3: X=0, Y=5 bits
* For Z
* Opt 1: Z=7 bits
* Opt 2: Z=8 bits

**FL comments:**

* No matter 7 or 8 is used for Z, the granularity loss is high. I did the calculation work, and it is highlighted as follows. The granularity loss is the disadvantages in PSBCH TDD indication due to bit limit (12 bits). Based on my calculation, approximately 13327 states may not be fully indicated. Z=7 bits has a loss of 11663, and Z=8 bits has a loss of 10447. Under this dimension, the difference (11663-10447=1216) between 7 or 8 bits seems like not so large. Anyhow, there is always more than 10000 granularity loss which is inevitable.
* For jointly indication by combination of X and Y, there is forward compatibility when it is 5 bits. When X=0 and Y=4 bits, some periods cannot be fully indicated, i.e. period 4, 5 and 10 ms. By calculation, 68 granularity loss happens. This is because there is no indication on one pattern or two patterns are configured.
* If 1 reserve bit is taken for TDD indication, only 1 reserve bit left. The concern is that it is not good for future function extension. From my perspective, 1 bit or 2 bits of reservation does not have so much difference.
* My previous proposal on Z is FFS the details on how to indicate UL slots. I think jointly indication when two patterns are configured is a proper way, so I add it to the Alt 1 and 2.
* There is also another critical issue mentioned by one company: different interpretation of SL slots between InC UEs and OoC UEs. InC UEs will have the symbol-level resource indication from gNB, while OoC UEs can only get slot-level resource indication from PSBCH. As it was agreed that 7~14 symbols within one slot can be used for SL UE, PSBCH cannot indicate those slots with only partial symbols are UL. There will be a problem when InC UEs communicate with OoC UEs.
* **FL: It is quite difficult for me to determine which Alt can be taken for TDD indication in PSBCH, because each one has pros accompanied with cons that cannot be ignored. From my perspective, I would like to take Alt 1 as a working assumption.**

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| **Alt 1: 1+4+7** | |
| **Pros** | Following the WA of 12 bits.  For one pattern: Full indication of all periods |
| **Cons** | For 2 patterns: Granularity loss (approx. 11663) |

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| --- | --- |
| **Alt 2: 1+4+8** | |
| **Pros** | For one pattern: Full indication of all periods |
| **Cons** | Revert WA of 12 bits.  Consume 1 reserve bit.  For two patterns: Granularity loss (approx. 10447) |

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| **Alt 3: 0+4+8** | |
| **Pros** | Following the WA of 12 bits. |
| **Cons** | For one pattern: period 4/5/10 ms cannot be fully indicated.  For one patterns: Granularity loss (approx. 68)  For two patterns: Granularity loss (approx. 10447) |

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| **Alt 4: 0+5+7** | |
| **Pros** | Following the WA of 12 bits.  For one pattern: Full indication of all periods  Forward compatibility of 5 bits |
| **Cons** | For 2 patterns: Granularity loss (approx. 11663) |

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| **Alt 5: 0+5+8** | |
| **Pros** | For one pattern: Full indication of all periods  Forward compatibility of 5 bits |
| **Cons** | Revert WA of 12 bits.  Consume 1 reserve bit.  For two patterns: Granularity loss (approx. 10447) |

***FL proposals:***

***Alt 1:***

* ***For indication of TDD configuration:***
* ***X=1 bit indicates the number of patterns***
* ***Value 0 indicates one pattern is used.***
* ***Value 1 indicates two patterns are used.***
* ***Y=4 bits indicate the periodicity information***
* ***When one pattern is used, Y indicates the periodicity of the pattern.***
* ***When two patterns are used, Y jointly indicates the periodicities of the two patterns.***
* ***Z=7 bits indicate the UL slots***
* ***UL slots are jointly indicated by 7 bits when two patterns are configured.***
* ***FFS other details.***

***Alt 2:***

* ***For indication of TDD configuration:***
* ***X=1 bit indicates the number of patterns***
* ***Value 0 indicates one pattern is used.***
* ***Value 1 indicates two patterns are used.***
* ***Y=4 bits indicate the periodicity information***
* ***When one pattern is used, Y indicates the periodicity of the pattern.***
* ***When two patterns are used, Y jointly indicates the periodicities of the two patterns.***
* ***Z=8 bits indicate the UL slots***
* ***UL slots are jointly indicated by 8 bits when two patterns are configured.***
* ***FFS detail.***

***Alt. 3:***

* ***For indication of TDD configuration:***
* ***X=0 bit indicates the number of patterns***
* ***Two patterns are used.***
* ***Y=4 bits indicate the periodicity information***
* ***Y indicates the periodicities of the two patterns.***
* ***Z=8 bits indicate the UL slots***
* ***First 4 bits indicates the number of UL slots in the first pattern and second 4 bits indicates the number of UL slots in the second pattern.***

For Alt 3, I add the following table for further explanation on how to use 2 patterns to indicate 1 pattern of the period. Please correct me if my summary is wrong.

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| --- | --- | --- | --- | --- | --- |
| Index | 1 Pattern  (msec) | | 2 Pattern  (msec) | Slot configuration period of *pattern1*  (msec) | Slot configuration period of *pattern2*  (msec) |
| 0 | 0.5 | | 1 | 0.5 | 0.5 |
| 1 | 0.625 | | 1.25 | 0.625 | 0.625 |
| 2 | 1 | | 2 | 1 | 1 |
| 3 | 2.5 |  | 2.5 | 0.5 | 2 |
| 4 | 1.25 | 2.5 | 1.25 | 1.25 |
| 5 |  | 2.5 | 2 | 0.5 |
| 6 | 4 |  | 4 | 1 | 3 |
| 7 | 2 | 4 | 2 | 2 |
| 8 |  | 4 | 3 | 1 |
| 9 | 5 | | 5 | 1 | 4 |
| 10 | 5 | 2 | 3 |
| 11 | 5 | 2.5 | 2.5 |
| 12 | 5 | 3 | 2 |
| 13 | 5 | 4 | 1 |
| 14 | 10 | | 10 | 5 | 5 |
| 15 |  | | 20 | 10 | 10 |

**Email responses 4/20-4/23**

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| **Company** | **Views** |
| CMCC | **Not fully agree.**   1. ***X=1 bit indicates the number of patterns: Agree*** 2. ***Y=4 bits indicate the periodicity information: Agree*** 3. ***Z=7 bits indicate the UL slots: Not agree***   We think the number of bits of Z is highly related to the indication method, i.e. joint indication (option 1) or independent indication (option 2) of UL slot in two patterns, so it is preferred to be discuss the design details first. It can be observed from the table below that for FR2, ***only the first 6 periodicity combinations (highlighted in grey) can be indicated within Z=7 bits (joint indication) or Z=8 bits (independent indication) using one-120KHz-slot granularity.*** For the rest of the periodicities, the granularity should be larger which sacrifices the indication flexibility, i.e. for 10ms+10ms periodicity, six-slot granularity is used for independent indication with Z=8 bits and eight-slot granularity is used for joint indication with Z=7 bits.  ***We are considering an additional way to reduce the impact, that is, we omit the state that the full periodicity are all UL slot***, which lead to option 1’(joint indication) and option 2’(independent indication) in the following table. For example, when 2ms+2ms is configured, if we do not indicate the case with all 16 slots as UL, the number of states to indicate is only 16, resulting that only 8bits (either joint indication or independent indication) are needed compared with the original option 1/2 where 9bits/10bits are required. In this way, ***more periodicity combinations (11 combinations highlighted in grey) can be indicated within 8bits without sacrificing slot granularity.*** Regarding the resource waste, we consider it acceptable since sacrificing only one slot when the whole periodicity is configured as UL. Therefore, ***it is preferred to use Z=8bits independent indication for finer granularity for more periodicity combination. The number of UL slots is indicated using 120KHz as reference SCS with different granularities for different periodicity combinations as follow:***  *• For 0.5+0.5ms, 0.625+0.625ms, 1+1ms, 0.5+2ms, 2+0.5ms, 1.25+1.25ms, 1+3ms, 3+1ms, 2+2ms, 1+4ms and 4+1ms periodicity combinations,* ***one-slot granularity*** *is used;*  *• For 2+3ms, 3+2ms and 2.5+2.5ms combinations,* ***two-slot granularity*** *is used;*  *• For 5ms+5ms periodicity,* ***three-slot granularity*** *is used;*  *• For 10ms+10ms periodicity,* ***five-slot granularity*** *is used.*  **Table 1 Number of bits needed for indicating number of UL slot using 120Khz as reference SCS**   |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | Pattern 1 | Pattern 2 | Total number of 120KHz slots N\_1 | Total number of 120KHz slots N\_2 | Option 1:  Number of bits for ***joint indication*** | Option 2:  Number of bits for ***independent indication*** | Option 1‘:  Option 1 with no full UL slot indication | Option 2‘:  Option 2 with no full UL slot indication | | 0.5 | 0.5 | 4 | 4 | 5 | 6 | 4 | 4 | | 0.625 | 0.625 | 5 | 5 | 6 | 6 | 5 | 6 | | 1 | 1 | 8 | 8 | 7 | 8 | 6 | 6 | | 0.5 | 2 | 4 | 16 | 7 | 8 | 6 | 6 | | 2 | 0.5 | 16 | 4 | 7 | 8 | 6 | 6 | | 1.25 | 1.25 | 10 | 10 | 7 | 8 | 7 | 8 | | 1 | 3 | 8 | 24 | 8 | 9 | 8 | 8 | | 3 | 1 | 24 | 8 | 8 | 9 | 8 | 8 | | 2 | 2 | 16 | 16 | 9 | 10 | 8 | 8 | | 1 | 4 | 8 | 32 | 9 | 10 | 8 | 8 | | 4 | 1 | 32 | 8 | 9 | 10 | 8 | 8 | | 2 | 3 | 16 | 24 | 9 | 10 | 9 | 9 | | 3 | 2 | 24 | 16 | 9 | 10 | 9 | 9 | | 2.5 | 2.5 | 20 | 20 | 9 | 10 | 9 | 10 | | 5 | 5 | 40 | 40 | 11 | 12 | 11 | 12 | | 10 | 10 | 80 | 80 | 13 | 14 | 13 | 14 | |
| NTT DOCOMO | Firstly, how to use each part of X/Y/Z should be clarified. Otherwise, the same discussion in the last meeting would be repeated.  We agree with the direction of CMCC’s proposal, i.e. in some cases, UL slots are indicated with granularity of more than one slot. This direction should be discussed and agreed if possible. Then, the granularity level can be discussed with the size of Z.  Similarly, how to X/Y should be clarified. For example, “X = 1 bit with 0 indicates one pattern and 1 indicates two patterns. Y = 4 bits, where one value from {0.5, 0.625, 1, 1.25, 2, 2.5, 4, 5, 10} is indicated with 0000 = 0.5, 0001 = 0.625, etc. for one pattern, …” something like this. |
| Samsung | No support with following reasons.   * It is evident that Z=8 (assuming X=0, default dual pattern) can provide more candidate numbers of UL slots rather than Z=7 (assuming X=1). For Z=7, 80 ( = min(27,80) for single pattern) + 128 ( = 27 for dual pattern) = **208** candidates. For Z=8, 16 ( = 24 for single pattern) + 256 ( = 28 for dual pattern) = **272** candidates. * For Z=7, it is quite difficult to find a single solution since companies supporting (X,Y,Z)=(1,4,7) have different detailed solutions and furthermore Z=7 has an issue of how to determine the number of UL slots per pattern in case of dual pattern as it is odd number. * It is unnecessary to have X=1 as the set of period for single pattern are subset of periods for dual pattern. Instead of indicating patterns, it should be used for other purpose such as indicating UL slots. * We also agree with DCM, CMCC such that just deciding how (X,Y,Z) sizes are should be done with detailed of design since different company have different design principle although they have shown the preference of same size of (X,Y,Z). Also, we agree to have something like the concept of different granularity depending on period since it is evident that all bitmap information cannot indicate entire TDD configuration considering it has limited bitmap size. * Regarding the proposal such as X+Y+Z=13 bits, we have strong concern of reducing reserved bits for PSBCH since reserved bits should be used for future V2X services that have not been identified. That’s why 2 reserved bits should be kept as working assumption.   In this sense, we are supportive of (X,Y,Z) =(0,4,8) with dual pattern as default without reverting working assumption. There is no need to revert working assumption, and it can provide higher flexibility / much information than (1,4,7). |
| Huawei, HiSilicon | We agree CMCC and DOCOMO’s view to first more clearly define the usage of the parameters of X, Y and Z. And considering the number of bits limitation, also we need to agree UL slots are indicated with scaled granularity. Then our proposal as following:  ***Proposal 1: Among the 12 bits for indication of TDD configuration:***   * ***X=1 bit indicates the number of patterns.***   + ***Xv=0: indicates one TDD-UL-DL Pattern 1 is used***   + ***Xv=1: indicates both TDD-UL-DL Pattern 1 and Pattern 2 is used*** * ***Y=4 bits indicate the periodicity information.***   + ***If Xv equals to 0, Y is used to indicate a TDD-UL-DL Pattern 1 periodicity***   + ***If Xv equals to 1, Y is used to jointly indicate both the TDD-UL-DL Pattern 1 and Pattern 2 periodicity*** * ***Z bits indicate the UL slots with scaled granularity***   + ***the Z field can be decided once X and Y are clear*** |
| Nokia | We share the view with other companies that we need to clarify how the bits assigned to X/Y/Z are used to complete the discussion.  We also agree with CMCC and NTT DOCOMO that that we can use higher granularity in higher SCS to indicate the number of SL slots. This may result of course some restriction (mainly numSLslots<=numULslots) depending on the used configuration, but would be acceptable in our view.  We agree with Samsung that the number of reserved bits should not be reduced (from 2) to increase the size of bits used for TDD configuration. However as pointed out in our paper (R1-2001806) we could consider reduce the bits used for slot index, if we account the TDD configuration information reducing the candidate locations for SL slots. |
| vivo | **For X and Y, We prefer to jointly indicate the periodicity and number of patterns, and X+Y=5 bits**.  9 different periodicities are supported for a single pattern case, while up to 16 possibilities are allowed in two patterns case. Thereby 25 combinations of periodicity and number of patterns are supported, and **5 bits are sufficient for joint indication wherein codepoints#25-31 are left unused**.  From the perspective of the indication of the number of patterns and the periodicities, there is no significant difference between using separate indication and joint indication. However, joint indication does have some merits in the perspective of forward compatibility. For example, if some new periodicities are introduced in future releases, such a scheme may only require a few modifications to exploit the unused codepoints for an extension. By contrast, the independent indication scheme needs more bits for extension whenever some of these parameters change.  **For Z, We prefer Z=8.**  We share a similar concern as CMCC and Samsung on Z =7 bits that it can cause a considerable loss in granularity and resource indication, especially when SCS=120kHz. We would like to decide the value of Z first, and then the granularity of Z can be discussed.  Additionally, we think **some extreme cases can also be precluded** to avoid significant compression of resource indication. To be specific, the following cases can be ruled out when two patterns are configured:   * 1. Case1. One or both patterns have no UL slots: 0 slots in P1 and/or 0 slots in P2      1. If there are no UL slots in both patterns, it is impossible to operate NR SL.      2. gNB should configure a single TDD pattern with a UL portion instead of configuring two TDD patterns wherein one of them has no UL   2. Case2. One or both patterns have full UL slots: full UL for P1 and/or full UL for P2      1. This case has already been discussed in the last meeting, it is not reasonable to assume that a whole pattern is UL or the consecutive UL resources across patterns.   By excluding case1 and case2, 1-slot granularity can be used for resource indication in the following cases except for the ones highlighted in yellow.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Two patterns: P1+P2 | | 120kHz | | Number of combinations(exclude case1 case2) | | P1(ms) | P2(ms) | P1(slot) | P2(slot) | | 0.5 | 0.5 | 4 | 4 | 9 | | 0.625 | 0.625 | 5 | 5 | 16 | | 1 | 1 | 8 | 8 | 49 | | 1.25 | 1.25 | 10 | 10 | 81 | | 2 | 0.5 | 16 | 4 | 45 | | 0.5 | 2 | 4 | 16 | 45 | | 2 | 2 | 16 | 16 | 225 | | 3 | 1 | 24 | 8 | 161 | | 1 | 3 | 8 | 24 | 161 | | 4 | 1 | 32 | 8 | 217 | | 1 | 4 | 8 | 32 | 217 | | 2.5 | 2.5 | 20 | 20 | 361 | | 3 | 2 | 24 | 16 | 345 | | 2 | 3 | 16 | 24 | 345 | | 5 | 5 | 40 | 40 | 1521 | | 10 | 10 | 80 | 80 | 6241 |   For these cases, coarse granularity is needed. For 2.5+2.5, 2+3, or 3+2, either 1-slot granularity or 2-slot granularity is acceptable. However, for 5 ms +5 ms, 10 ms +10 ms, if only one codepoint is used (and therefore 256 combinations are allowed), the indication granularity will be increased to 5 slots which is imprecise for resource indication. **Note that there are some unused codepoints of the indication of pattern number and pattern periodicities. Some of them can be reused together with Z bits for resource indication.**  For example, for P1+P2=10ms+10 ms and SCS=120KHz, the granularity of resource indication can be kept as small as 2-slots if 4 codepoints are exploited for 10ms+10ms. For example, if the indicator of periodicity and the number of patterns =M~M+3, P1+P2=10 ms+10 ms, and both patterns contain SL resources, up to 2^10 combinations can be indicated by PSBCH. We assume that the number of slots available for SL indicated by PSBCH is somehow restricted by the S-SSB number (pre-)configured as the S-SSB should be either concentrated on a set of consecutive UL slots or a set of equally spaced UL slots. Configurations can be envisioned that the consecutive slots available for SL in a pattern is no larger than 64 slots in this case. Thereby 4 codepoints+Z bits are sufficient to cover all combinations for 10+10 ms with 2-slot granularity. Similarly, for 5 ms+5ms, 2 codepoints +Z bits are sufficient to cover all combinations for 5+5 ms with 2-slot granularity if the number of available slots in each pattern is assumed to be no larger than 32 slots. |
| ZTE, Sanechips | We agree to the proposal. Though we echo that the bit width for different fields is substantial, further details including considerations on granularity for UL slot indication need to be captured in the proposal or make up a separate proposal to deliver the whole picture of TDD configuration indication. As analyzed in R1-2001578, Z = 7 bits could indicate the slot numbers within 10ms and the other periodicity values under single pattern. For double patterns, our considerations on this UL slot indication granularity works based on a reference SCS as follows.  Firstly, a reference SCS: ***refSCS*** is derived implicitly through a formula, e.g. ***refSCS*** = min(***SL SCS***, maximal supportable SCS with at most 7 bits) for any given pattern and period combination.  Secondly, the remainder bit(s), if any, are used to indicate the remainder slots measured in SL SCS.  For step 1, our thinking is that the range of {1,2,...,Ns,1} and{0,2,...,Ns,2-1}slots needs to be indicated. The following are the rationale behind:  1. At least 1 downlink/flexible slot should be reserved for SSB transmission and we suppose this case, if configured, places the downlink/flexible slot in the second pattern.  2. 0 UL slot, if configured, always presents in pattern 2. Single pattern could be configured instead otherwise.  3.At least 1 uplink slot should be reserved for sidelink.  The following example together with Fig.1 is put forward to illustrate the above methodology.  Example: Double patterns with periodicity {1ms, 4ms}and SL SCS = 120kHz  The slot combinations to be indicated is 8\*32 =256. The maximal supportable SCS with at most 7 bits is 60kHz with which the combinations to be indicated is 4\*16 = 64.  The remainder bits account for 7-log2(64) = 1 bit  Some remainder slot could be indicated with this bit.    Figure. 1 |
| Spreadtrum | We support that X=1 bit indicates the number of patterns and Y=4 bits indicate the periodicity information.  For the value of Z, we think the indication mechanism for the UL slots in two patterns should be discussed first, i.e., whether scaled granularity is supported in some cases and in which cases it is supported. |
| OPPO | We prefer **joint indication of patterns and periodicities: X+Y = 5 bits**. The following table shows the possible combination of patterns and periodicities.  To indicate the number of UL slot, we propose a default SCS is used to determine the number of UL slots based on TDD-UL-DL-Configuration, for example, 15kHz for FR1, and 60kHz for FR2. In this case, Z= 7 bits can be used for UL slot indication.     |  |  |  |  | | --- | --- | --- | --- | | Index | Slot configuration period  (msec) | Slot configuration period of *pattern1*  (msec) | Slot configuration period of *pattern2*  (msec) | | 0 | 0.5 | 0.5 | 0 | | 1 | 0.625 | 0.625 | 0 | | 2 | 1 | 1 | 0 | | 3 | 1 | 0.5 | 0.5 | | 4 | 1.25 | 1.25 | 0 | | 5 | 1.25 | 0.625 | 0.625 | | 6 | 2 | 2 | 0 | | 7 | 2 | 1 | 1 | | 8 | 2.5 | 1.25 | 1.25 | | 9 | 2.5 | 2.5 | 0 | | 10 | 2.5 | 2 | 0.5 | | 11 | 2.5 | 0.5 | 2 | | 12 | 4 | 4 | 0 | | 13 | 4 | 1 | 3 | | 14 | 4 | 2 | 2 | | 15 | 4 | 3 | 1 | | 16 | 5 | 5 | 0 | | 17 | 5 | 1 | 4 | | 18 | 5 | 2 | 3 | | 19 | 5 | 2.5 | 2.5 | | 20 | 5 | 3 | 2 | | 21 | 5 | 4 | 1 | | 22 | 10 | 10 | 0 | | 23 | 10 | 5 | 5 | | 24 | 20 | 10 | 10 | |
| Ericsson | Agree with the proposal |
| Qualcomm | We agree with the proposal overall. However, as indicated by others, clarification on details of the 3 fields is still needed.  For X and Y, we prefer a joint encoding in 5 bits. For example, the table shown by OPPO.  For Z, we agree that for larger period values, 7 bits may not be sufficient to indicate all the combinations in all cases. The details can be discussed separately. |
| LGE | FL Proposal is supported.  Additionally we need to define the details of each value as follows.  X value;   |  |  | | --- | --- | | *X value* | *Number of patterns* | | *0* | *1* | | *1* | *2* |   Y value for X=0;   |  |  | | --- | --- | | *Y value (in decimal)* | *Periodicity* | | *0* | *0.5* | | *1* | *0.625* | | *2* | *1* | | *3* | *1.25* | | *4* | *2* | | *5* | *2.5* | | *6* | *4* | | *7* | *5* | | *8* | *10* |   Y value for X=1;   |  |  |  | | --- | --- | --- | | *Y value (in decimal)* | *Periodicity of pattern 1* | *Periodicity of pattern 2* | | *0* | *0.5* | *0.5* | | *1* | *0.625* | *0.625* | | *2* | *1* | *1* | | *3* | *0.5* | *2* | | *4* | *2* | *0.5* | | *5* | *1.25* | *1.25* | | *6* | *1* | *3* | | *7* | *3* | *1* | | *8* | *2* | *2* | | *9* | *1* | *4* | | *10* | *4* | *1* | | *11* | *2* | *3* | | *12* | *3* | *2* | | *13* | *2.5* | *2.5* | | *14* | *5* | *5* | | *15* | *10* | *10* |   Z value for given X and Y;   |  |  |  | | --- | --- | --- | | *Z value (in decimal)* | *#UL slots in pattern 1* | *#UL slots in pattern 2* | | *0, …, NP2-1* | *0* | *1,…, NP2* | | *NP2, …, 2\* NP2* | *1* | *0,…, NP2* | | *2\* NP2+1, …, 3\* NP2+1* | *2* | *0,…, NP2* | | *…* | *…* | *…* | | *k\* NP2+k-1, …, (k+1)\* NP2+k-1* | *k* | *0,…, NP2* | | *…* | *…* | *…* | | *NP1\* NP2+ NP1-1, …, ( NP1+1)\* NP2+ NP1-1* | *NP1* | *0,…, NP2* |   where *NP1* and *NP2* are the maximum number of UL slots in pattern 1 and 2 respectively.  Regarding the reference SCS, the default value is the actual SL SCS unless Z cannot represent all the cases of the number of UL slots. If the possible number of UL slots exceeds the Z value range for a combination of SCS and the periodicity for two patterns, the reference SCS can be adjusted as follows. For a single pattern, the actual SL SCS is always used as the reference SCS.   |  |  |  |  | | --- | --- | --- | --- | | *SL SCS* | *Pattern 1 periodicity* | *Pattern 2 periodicity* | *Ref. SCS* | | *120 kHz* | *1* | *3* | *60 kHz* | | *3* | *1* | | *2* | *2* | | *1* | *4* | | *4* | *1* | | *2* | *3* | | *3* | *2* | | *2.5* | *2.5* | | *5* | *5* | *30 kHz* | | *10* | *10* | *15 kHz* | | *60 kHz* | *5* | *5* | *30 kHz* | | *10* | *10* | *15 kHz* | | *30 kHz* | *10* | *10* | *15 kHz* | | *All other cases* | | | *SL SCS* |   The reference SCS is (pre-)configured by a higher layer signaling rather than determined by an implicit rule. The UL slot counted in Z bits includes the slot that contains at least Y-th, (Y+1)-th, ..., (Y+X-1)-th UL symbols, where X and Y are sl-LengthSymbols and sl-StartSymbol respectively. The ‘virtual’ UL slots counted based on the reference SCS should include only the ‘actual’ UL slots based on the SL SCS. That is, if e.g. DL slots are included as part of the virtual UL slot, this virtual UL slot is discarded from UL slot indication in PSBCH. |
| Apple | We agree that X=1 to indicate the number of patterns and Y=4 to indicate periodicity.  We do not support Z=7. Instead, we think Z is 8 bits. Even with 8 bits, we are unable to exactly indicate the number of SL slots for two TDD patterns at high SCS. As mentioned by CMCC and other companies, we can allow higher granularity for the high SCS cases for two TDD patterns. Also, we prefer separate indication of two TDD patterns, and 4 bits are used to indicate the number of SL slots in each TDD pattern. |
| MediaTek | Agree with the proposal with the need of more consideration on the usage of Z bits. For the bits consuming patterns such as {2ms,2ms},{2.5ms,2.5ms},{5ms,5ms}, a reference pattern such as {2ms,2ms} with only total 6 bits (at SCS 60khz) can be used to indicate the UL slots. That is, the signaling based on 6 bits of the reference pattern {2ms,2ms} can be used to derive the UL slots of the other patterns by scaling with a granularity. For example, the signaling indicates 6 UL slots based on the reference pattern {2ms,2ms}, then the UL slots for the actual pattern {5ms,5ms} = 6 / RefPeriod \* ActualPeriod = 6/2\*5=15 UL slots. |
| Intel | We agree with proposal. Looking forward for further proposal on encoding details. |
| Fujitsu | Agree with the proposal. The details of X,Y,Z need to be further discussed as indicated by other companies. | The proposal can be agreed but the details of X,Y,Z need to be further discussed as indicated by other companies. |

**Email responses in 4/23-4/24**

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| --- | --- |
| **Company** | **Views** |
| Nokia | (Note: corrected Nokia position above table. Also just noting that we also considered option with Y=3 enabled by preconfiguration but as it is in minority it can be left out from the table).  Our preference would be Alt.2  On compressing the patterns (P, P+P2) to Y=4 bits, we proposed excluding cases where P2>P (And alignment rule that every 20/P or 20/(P+P2) patterns, first symbol of the pattern(s) is a first symbol of an even frame) to make the number of P+P2 cases to be 12.  For compressing the UL slots, like noted earlier, we think that larger granularity is acceptable (e.g. based on SCS and/or pattern). However, it would seem difficult to restrict the number of bits below 8 (4+4) while maintaining sufficient flexibility. Hence we would support increasing the size of the TDD configuration indication with one bit. If 1 reserved bit is not sufficient, we can reduce the size of tehslot index (based on the TDD pattern as the used slot has to be within the SL slots). |
| Huawei, HiSilicon | We think both Alt. 1 and Alt. 2 are agreeable. |
| LGE | Alt. 1 is supported.  Using Z=8 bits sacrifices the reserved bits from 2 bits to 1 bit, which is too small for future extension. Guaranteeing future extension is more beneficial than reducing a few cases of granularity loss. |
| Samsung | Based on I commented in email body, I rephrased my wording as below.  It seems common understanding that 11~13 bits are not clearly enough to indicate full UL slots for one or two patterns for Uu.  We have strong concern on having 1 bit of pattern indication based on our analysis. It does not bring significant benefits, and wasteful bit. This is not optional signaling design, PSBCH content that should be broadcasted everywhere and everytime. So, it should be carefully designed with a certain principle.  In this sense, alt.1 and alt. 2 are not necessary since there is no strong justification why 1 bit of pattern indication is necessary.  We support alt. 3. |
| ZTE, Sanechips | Alte 1 (Z = 7 bits). It is not sensible to reduce 1 bit out of the 2 bits reserved in PSBCH for enhancement in future release.  Our position is that it's of critical importance to ensure the same interpretation of the SL slots for InC and OoC UEs. The current working assumption under structure agenda indicates the SL slot for InC UEs are determined from ***TDD-UL-DL-ConfigCommon.*** Given the PSBCH indication would surely suffer from granularity loss irrespective of any altes taken and we are concerned on the potential slot misalignment issues caused due to the limited slot indication capability in PSBCH. We would like to propose the following under the proposal.  ***note: The UL slot(s) derived by out of coverage UE from PSBCH should be aligned with that derived by in coverage UE from TDD-UL-DL-ConfigCommon.*** |
| Qualcomm | (Note: corrected Qualcomm’s position in the table, our earlier comment was about the details of compressing/subsampling the content)  We still think that joint (X+Y) would be a good solution.  Of the alternatives on the table, we are ok with Alt 1 or Alt 3. We can be ok with Alt 2 depending on where the extra bit comes from. |
| OPPO | We agree with QC that joint (X+Y) indication of pattern/periodicity is OK. In this case X+Y=5. Based on our analysis, up to 25 code-points are enough considering all combinations of pattern and periodicity. Rest 7 code-point can be saved and more suitable for forward compatibility.  We are OK to set Z=8 to indicate UL slot with finer granularity. |
| CMCC | We are Ok with Alt 2 or Alt 3.  As noted earlier, by omitting the state that the full periodicity are all UL slot, more periodicity combinations (11 combinations totally) can be indicated within 8bits without sacrificing slot granularity, and for 10ms+10ms combination, the granularity is reduced from eight-slots to five-slots. So Z=8 bits is more preferred.  As noted by Samsung, we share similar view that 4ms single pattern can be indicated by 1ms+3ms dual pattern case.  Therefore, Alt 2 or Alt 3 are both OK for us. |
| NTT DOCOMO | We support Alt 1. Alt 3 is OK as well. We do not support Alt 4 and Alt 5.  Advantage of Alt. 4/5 is not so much while one reserved bit is sacrificed. Considering future release, two reserved bits are preferable for us. In addition, the main motivation of Alt 4/5 is case of 10+10ms/120kHz for dual patterns.  For smaller SCS, the advantage is very limited. For example, in SCS=30kHz, the issue occurs only in 10+10ms of dual patterns (see R1-2002440 - table 1). Based on RAN4 discussion, FR1 seems to be the typical use case in Rel-16. The reserved bit reduction mainly for FR2 is not preferable in the current situation. Therefore, we suggest that X+Y+Z=12.  Note: also our position is corrected as the above table. We do not support 13 bits, as our contribution mentioned. (What we supported in table below is CMCC’s direction of the discussion. Not total number.) |
| Ericsson | We support Alt.1 |
| Fujitsu | Either Alt1 or Alt2 is agreeable |
| vivo | We support Alt.2 with Z=8 bits but for X and Y, we still prefer to indicate (Pattern + Periodicity) jointly with 5 bits.  Technically there is no significant difference between separate indication (Pattern=1 bits, Periodicity=4 bits) and joint indication(Pattern + Periodicity =5 bits). However, as we explained in the first round input, the joint indication of the number of patterns and periodicity with X+Y=5 bits is beneficial from the perspective of future extension. |

**Email responses in 4/24-4/30**

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| --- | --- |
| **Company** | **Views** |
| Samsung | It is noted that single pattern is subset of dual pattern except 4ms.  As you see in table 1-2 (slot configuration period when two patterns are configured), there are indexes having same period for pattern 1 and pattern 2.  Assuming that P1 is the period of pattern 1 and P2 is the period of pattern, period of single pattern can be provided by P1=P2.  For example, in figure below, considering that Uu is configured with having single period of P, sidelink can configureP1=P2=P with thesame UL slots for each pattern.  So, green marked index can also support single pattern. But, there is no (4ms, 4ms) in table 1-2, as pointed out by CMCC.  As I commented, (1,3) or (2,2) or (1,4) can indicate 4ms as right figure as below.    To sum up, 16 entries in table 1-2 can indicate both single and dual pattern, and single pattern can beimplicitly indicated if two periods aresame and the number of UL slots aresame per each period (except to 4ms).  说明: cid:image001.png@01D61A4C.5489EC10  Table 1-2: Slot configuration period when**two patterns** are configured   |  |  |  |  | | --- | --- | --- | --- | | Index  j | Slot configuration period  P+P2 (msec) | Slot configuration period ofpattern1  P (msec) | Slot configuration period ofpattern2  P2 (msec) | | 0 | 1 | 0.5 | 0.5 | | 1 | 1.25 | 0.625 | 0.625 | | 2 | 2 | 1 | 1 | | 3 | 2.5 | 0.5 | 2 | | 4 | 2.5 | 1.25 | 1.25 | | 5 | 2.5 | 2 | 0.5 | | 6 | 4 | 1 | 3 | | 7 | 4 | 2 | 2 | | 8 | 4 | 3 | 1 | | 9 | 5 | 1 | 4 | | 10 | 5 | 2 | 3 | | 11 | 5 | 2.5 | 2.5 | | 12 | 5 | 3 | 2 | | 13 | 5 | 4 | 1 | | 14 | 10 | 5 | 5 | | 15 | 20 | 10 | 10 |   [To LGE]  I do agree with your concern on proposal 3.  For single pattern, proposal 3 cannot give more information than proposal 1 since proposal 3 just use 4 bits, while proposal 1 use 7 bits.  On the other hand, for dual pattern proposal 3 give more information than proposal 1, as you said, since proposal 3 provides 8 bits, while proposal 1 provides 7 bits.    I think that it cannot be arguable that single pattern is more general/significant than dual patterns, since we don’t have any clue or real deployment scenario, further we don’t know how operator will use this really.  From specification point of view, we have to treat single pattern and dual patternequally, without having any bias.  That’s why I gave the following table showing calculation of number of cases for all proposals in case of single patterns and dual patterns.  I have one more comment on your table.  Actually, principle of proposal 3 implicitly provides single pattern using dual patterns.  I just realized that we don’t need to fix P=P1=P2, instead, we can also use P=P1+P2 in similar with how we make 4ms.  In this sense, green part could be resolved by proposal 3, as well. So, the number of cases would be larger than what I expected in case of single patterns.   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | 120kHz SCS | 60kHz | 30kHz | 15kHz | | P1 | NumStates | NumStates | NumStates | NumStates | | 0.5 | 5 | 3 | 2 |  | | 0.625 | 6 |  |  |  | | 1 | 9 | 5 | 3 | 2 | | 1.25 | 11 | 6 |  |  | | 2 (1+1) | 17 | 9 | 5 | 3 | | 2.5 (1.25 +1.25) | 21 | 11 | 6 |  | | 4 (2+2) | 33 | 17 | 9 | 5 | | 5 (4+1) | 41 | 21 | 11 | 6 | | 10 (5+5) | 81 | 41 | 21 | 11 |   [To LGE]  For my better understanding, are you assuming that proposal 3 provide the granularity of 1 UL slot (1 state), so it may limit when the number of UL slots (or states) is larger than 16 slots or 16 states in one period?  Actually, I didn’t say anything about granularity for proposal 3. We also think that larger granularity concept in proposal 3, as we said in the first round of email discussion. If I misunderstand your saying “granularity”, please correct me.  Going back to your table, could clarify a little bit more why proposal 3 cannot support red-box, while proposal 1 can support red-box?    Anyway, proposal also have 7 bits, whether joint coding or individual coding, maximum information size indicating the possible cases is limited.  For example, there are 100 UL slots to be indicated in a period, if we have 1 bit,‘0’ says 0 slot and‘1’ says 100 slots. While we have 2 bits,‘00’ says 0 slot, ‘01’ says 33 slots,‘10’ says 66 slots, and‘11’ says 100 slots.  It is the fact that more bits indicate larger number of states.  **[To all]**  I do agree with alt. 3 that cannot indicate when the number of states exceed 16 in a certain period.  And, I appreciate your efforts for explaining details of alt. 1 on how joint coding operates.  But, I’m not sure whether that is common understanding for the group supporting alt. 1. This is because alt.1 is described below.  o   ***Z=7 bits indicate the UL slots***  −        ***FFS detail.***    For the granularity issue, actually, alt. 3 provides maximum number of 32 cases for single pattern (due to 16+16), and provides maximum number of 256 cases for dual pattern (due to 16\*16) with a restriction that one of dual patterns has less number of 16, it will be reduce the possible cases.  So, for fair comparison, I would like to share how many cases alt. 1 or alt. 3 provides.    For single pattern, I agree that alt.3 cannot provide full granularity. So, I checked how much loss will be happened as follows. As you see, about **60** granularity loss happens in alt. 3 compared to alt. 1.  (FYI, I didn’t put any information for cases where there is no issue)  (To Chao, for 2.5ms, alt. 3 provides 1.25+1.25 combination, so there is no issue of granularity loss)   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Alt. 1 | | | | | |  | 120kHz SCS | 60kHz | 30kHz | 15kHz | | P1 | NumStates | NumStates | NumStates | NumStates | | 0.5 |  |  |  |  | | 0.625 |  |  |  |  | | 1 |  |  |  |  | | 1.25 |  |  |  |  | | 2 |  |  |  |  | | 2.5 |  |  |  |  | | 4 | 33 |  |  |  | | 5 | 41 |  |  |  | | 10 | 81 | 41 |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | | Alt. 3 | | | | | |  | 120kHz SCS | 60kHz | 30kHz | 15kHz | | P1 | NumStates | NumStates | NumStates | NumStates | | 0.5 |  |  |  |  | | 0.625 |  |  |  |  | | 1 |  |  |  |  | | 1.25 |  |  |  |  | | 2 |  |  |  |  | | 2.5 |  |  |  |  | | 4 | 32 |  |  |  | | 5 | 32 |  |  |  | | 10 | 32 | 32 |  |  | |
| LGE | Thanks for the explanation. I have one comment on the proposal 3.  Compared to the proposal 1 (using same 12 bits in total), proposal 3 sacrifices the granularity in UL slot number even for a single pattern case. All the grey combinations in the table below cannot be perfectly represented by proposal 3, while proposal 1 can perfectly represent them. For two patterns case, the number of granularity loss cases are larger in proposal 3 than in proposal 1.  If my understanding is correct, such a significant loss in UL slot number granularity even for a single pattern case is not desirable in my opinion.   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | 120kHz SCS | 60kHz | 30kHz | 15kHz | | P1 | NumStates | NumStates | NumStates | NumStates | | 0.5 | 5 | 3 | 2 |  | | 0.625 | 6 |  |  |  | | 1 | 9 | 5 | 3 | 2 | | 1.25 | 11 | 6 |  |  | | 2 | 17 | 9 | 5 | 3 | | 2.5 | 21 | 11 | 6 |  | | 4 | 33 | 17 | 9 | 5 | | 5 | 41 | 21 | 11 | 6 | | 10 | 81 | 41 | 21 | 11 |   [To Samsung]  I slightly modified my response as you have sent an another email ;-)  First of all, I didn’t say that the proposal 3 provides more information than the proposal 1 for the two patterns case.  What I said is that the proposal 3 sacrifices more cases than the proposal 1 in granularity for the two patterns case. For the single pattern case, only proposal 3 sacrifices the granularity. This is because each 4 bits are used for #UL slots of each pattern in the proposal 3, while a join representation is used in the proposal 1. The cases of the granularity loss are indicated as grey box in the table below, for two proposals.  Inherited from the single pattern constraint, every case where the number of cases exceeds 16 cannot be perfectly represented by the proposal 3. So, from the granularity loss perspective, the proposal 1 is always better than the proposal 3, even though the new email is taken into account.  Regarding the table you have shown in your email, I think the figure only describes the possible number of cases that can be represented by given bit combinations. Please note that the actual number of cases to be signaled is already fixed regardless of the bit combinations, and all the cases are already covered by every proposal. Then the only issue is how much the granularity is preserved.   |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **Proposal 3** | |  |  |  |  |  | |  |  |  | 120kHz SCS | 60kHz | 30kHz | 15kHz | | P1 | P2 | Total\_P | NumStates | NumStates | NumStates | NumStates | | 0.5 | X | 0.5 | 5 | 3 | 2 |  | | 0.625 | X | 0.625 | 6 |  |  |  | | 0.5 | 0.5 | 1 | 25 | 9 | 4 |  | | 0.625 | 0.625 | 1.25 | 36 |  |  |  | | 1 | 1 | 2 | 81 | 25 | 9 | 4 | | 0.5 | 2 | 2.5 | 85 | 27 | 10 |  | | 2 | 0.5 | 2.5 | 85 | 27 | 10 |  | | 1.25 | 1.25 | 2.5 | 121 | 36 |  |  | | 1 | 3 | 4 | 225 | 65 | 21 | 8 | | 3 | 1 | 4 | 225 | 65 | 21 | 8 | | 2 | 2 | 4 | 289 | 81 | 25 | 9 | | 1 | 4 | 5 | 297 | 85 | 27 | 10 | | 4 | 1 | 5 | 297 | 85 | 27 | 10 | | 2 | 3 | 5 | 425 | 117 | 35 | 12 | | 3 | 2 | 5 | 425 | 117 | 35 | 12 | | 2.5 | 2.5 | 5 | 441 | 121 | 36 |  | | 5 | 5 | 10 | 1681 | 441 | 121 | 36 | | 10 | 10 | 20 | 6561 | 1681 | 441 | 121 |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **Proposal 1** | |  |  |  |  |  | |  |  |  | 120kHz SCS | 60kHz | 30kHz | 15kHz | | P1 | P2 | Total\_P | NumStates | NumStates | NumStates | NumStates | | 0.5 | X | 0.5 | 5 | 3 | 2 |  | | 0.625 | X | 0.625 | 6 |  |  |  | | 0.5 | 0.5 | 1 | 25 | 9 | 4 |  | | 0.625 | 0.625 | 1.25 | 36 |  |  |  | | 1 | 1 | 2 | 81 | 25 | 9 | 4 | | 0.5 | 2 | 2.5 | 85 | 27 | 10 |  | | 2 | 0.5 | 2.5 | 85 | 27 | 10 |  | | 1.25 | 1.25 | 2.5 | 121 | 36 |  |  | | 1 | 3 | 4 | 225 | 65 | 21 | 8 | | 3 | 1 | 4 | 225 | 65 | 21 | 8 | | 2 | 2 | 4 | 289 | 81 | 25 | 9 | | 1 | 4 | 5 | 297 | 85 | 27 | 10 | | 4 | 1 | 5 | 297 | 85 | 27 | 10 | | 2 | 3 | 5 | 425 | 117 | 35 | 12 | | 3 | 2 | 5 | 425 | 117 | 35 | 12 | | 2.5 | 2.5 | 5 | 441 | 121 | 36 |  | | 5 | 5 | 10 | 1681 | 441 | 121 | 36 | | 10 | 10 | 20 | 6561 | 1681 | 441 | 121 |   [To Samsung]  ***Alt. 3:***          ***For indication of TDD configuration:***  o   ***X=0 bit indicates the number of patterns***  −        ***Two patterns are used.***  o   ***Y=4 bits indicate the periodicity information***  −        ***Y indicates the periodicities of the two patterns.***  o   ***Z=8 bits indicate the UL slots***  −        ***First 4 bits indicates the number of UL slots in the first pattern and second 4 bits indicates the number of UL slots in the second pattern.***    The main difference between the proposal 3 and other two proposals is the separate indication of UL slots or the joint indication of UL slots for two patterns case. This is why the proposal 3 has granularity loss than other two proposals in general.    Let me try to explain more with the case you questioned below: SCS=120kHz, P1=2, P2=0.5.  The number of states (=possible number of #UL slots) for pattern 1 and 2 are (16+1) and (4+1) respectively, which results in total 85 number of states as shown in the table. As first 4 bits indicate the number of states for pattern 1, the whole 17 cases cannot be indicated by 4 bits. So we need to scale down the reference SCS to reduce the number of states, where a group of UL slots is indicated. This is the situation that I mentioned as the granularity loss case, because the every odd number of UL slots cannot be perfectly indicated.    On the contrary, the proposal 1 uses joint indication with 7 bits, which can indicate a total 128 cases as you said. The number of states in this case is 85, and there is no problem in granularity for #UL slots.  [To Samsung/OPPO]  Thank Sungjin for detailed explanation and analysis. Now I had better understanding what you wanted to say.    Considering all the related discussions, the level of granularity loss depends on how the reference SCS is configured. If the reference SCS is configured per combination of SCS and periodicity, the proposal 1 is better than the proposal 3, as explained by several companies. If the reference SCS is configured per combination of SCS, periodicity and the number of UL slots, the proposal 3 is better than the proposal 1, as explained by Sungjin (I didn’t crosscheck it but seems so due to the number of bits). Our preference is the former as the signaling of the reference SCS is much simpler, something similar to the proposal by LGE or Huawei.    Thank Zhenshan for reminding the issue of future extension, which is an important feature to be considered. With the Zhenshan’s comment, 5 bits for X+Y (FFS details) seems to have another advantage of forward compatibility. The proposal 3 consumes full bit capacity of Y=4 bits, no forward compatibility is expected. Actually in the last meeting, I insisted the same proposal of the joint coding of X and Y, but the agreement was made to separate the 3 fields if I remember correctly.    In summary, our preference is still the proposal 1. |
| Huawei, HiSilicon | We have similar view as Woo-Suk. For the newly proposed Alt. 3, it is an interesting idea, but it will seriously impact the granularity.  First, it is true that 4ms single period can be described with (1ms, 3ms) or (2ms, 2ms) or (3ms, 1ms). However, assume that 120kHz is taken as the reference SCS, and as proposed, 4bits describe the UL slots in pattern1 and 4 bits describe the UL slots in pattern2, then we believe (2ms, 2ms) will be the better choice. On this basis, there are in total 17 states (0,1,2,…,16) to indicate with 4 bits, which is impossible. The only solution will be using a larger granularity. By contrast, if 4ms single period is regarded as an independent codepoint for X+Y, then at most 33 states (0,1,2,…,32) states need to be indicated. No granularity loss is observed. Furthermore, such separation also impacts other period combinations (please see red columns in the following table). In Alt. 1 and Alt. 2, single period cases do not suffer any ambiguity. However, by applying Alt. 3, 2.5ms, 4ms, 5ms, 10ms single period will be indicated with scaled granularity. We tend to believe that single-pattern configuration is more common than dual-pattern in practical scenarios. The dual-pattern cases need to be considered, but they are optimization issue. We may try our best to make the granularity loss as small as possible for dual-pattern case, but it is not preferred to let the scheme impact the granularity for single-pattern case.  Second, by applying Alt. 3, the TX UE will be confused when it needs to describe a 5ms single-pattern. According to Alt. 3, the spec should make the constraint that the TX UE can only use the 10ms row (index 14) with two 5ms periods that share the identical TDD configurations. However, it is much more reasonable if the TX UE can use (2ms, 3ms), (2.5ms, 2.5ms), or (3ms, 2ms) to indicate one 5ms period, for the sake of better granularity.   |  |  |  |  | | --- | --- | --- | --- | | Index  说明: cid:image003.png@01D61F38.F592DA40 | Slot configuration period  说明: cid:image004.png@01D61F38.F592DA40 (msec) | Slot configuration period ofpattern1  说明: cid:image005.png@01D61F38.F592DA40 (msec) | Slot configuration period ofpattern2  说明: cid:image006.png@01D61F38.F592DA40 (msec) | | 0 | 1 | 0.5 | 0.5 | | 1 | 1.25 | 0.625 | 0.625 | | 2 | 2 | 1 | 1 | | 3 | 2.5 | 0.5 | 2 | | 4 | 2.5 | 1.25 | 1.25 | | 5 | 2.5 | 2 | 0.5 | | 6 | 4 | 1 | 3 | | 7 | 4 | 2 | 2 | | 8 | 4 | 3 | 1 | | 9 | 5 | 1 | 4 | | 10 | 5 | 2 | 3 | | 11 | 5 | 2.5 | 2.5 | | 12 | 5 | 3 | 2 | | 13 | 5 | 4 | 1 | | 14 | 10 | 5 | 5 | | 15 | 20 | 10 | 10 | |
| MediaTek | Our preference is Alt.1 (X=1,Y=4,Z=7) and we would like to keep the total bits not larger than 12 bits as agreed working assumption due to the impact on PSBCH design.  For the solutions, maybe we can try to agree some high level principles at first, e.g.,  -       Whether to introduce some reference SCS to derive the UL slots? E.g., use the formats for 60khz patterns as the reference patterns to derive the UL slots for the corresponding 120khz patterns considering the different granularity.  -       Whether to introduce some reference patterns for a set of patterns? E.g., for the most bits consuming patterns with the same P1/P2 ratio such as {2.5,2.5} {5,5},{10,10}, use the format of the reference pattern (selected from one of them) to derive the others. |
| OPPO | Thanks for the discussion. I think we are reiterating the argument again and againL.  I think we can discuss these fields separately.  Firstly, for indication pattern/periodicity, there are two options:  -         Option 1: separate indication, X=1, Y=4;  -         Option 2: joint indication, X+Y=5:    Secondly, for indication of UL slots, Z=7 or 8 or 4+4 bits.  For the first issue, we prefer option 2. The total combination of pattern and periodicity is in the table below. The total combination is 25, and 5 bits for X+Y is enough. The reserved code-point can be used for forward compatibility. We cannot identify the additional benefit to indicate pattern and periodicity separately.    For the second issue, we have a WA that the total number of bits is 12. If we follow this, Z=7 is the only selection. If this WA is not confirmed, Z=8 can be considered since it can indicate more UL slots, or with finer granualarity. We are OK to both.   |  |  |  |  | | --- | --- | --- | --- | | Index  j | Slot configuration period  P+P2 (msec) | Slot configuration period of pattern1  P (msec) | Slot configuration period of pattern2  P2 (msec) | | 0 | 0.5 | 0.5 | 0 | | 1 | 0.625 | 0.625 | 0 | | 2 | 1 | 1 | 0 | | 3 | 1 | 0.5 | 0.5 | | 4 | 1.25 | 1.25 | 0 | | 5 | 1.25 | 0.625 | 0.625 | | 6 | 2 | 2 | 0 | | 7 | 2 | 1 | 1 | | 8 | 2.5 | 1.25 | 1.25 | | 9 | 2.5 | 2.5 | 0 | | 10 | 2.5 | 2 | 0.5 | | 11 | 2.5 | 0.5 | 2 | | 12 | 4 | 4 | 0 | | 13 | 4 | 1 | 3 | | 14 | 4 | 2 | 2 | | 15 | 4 | 3 | 1 | | 16 | 5 | 5 | 0 | | 17 | 5 | 1 | 4 | | 18 | 5 | 2 | 3 | | 19 | 5 | 2.5 | 2.5 | | 20 | 5 | 3 | 2 | | 21 | 5 | 4 | 1 | | 22 | 10 | 10 | 0 | | 23 | 10 | 5 | 5 | | 24 | 20 | 10 | 10 | |
| CMCC | I sent this again due to email collision with Woo-suk and Zhenshan.    Thanks for your great efforts on this email discussion. After explanation by LG and HW, I noticed that Alt 3 impact the granularity seriously for single pattern and sorry for correct CMCC’s position that Alt 3 is not OK for us.    The main difference between Alt 1 and Alt 2 is the number of bits for Z, i.e. Z=7 bits for Alt 1 and Z=8 bits for Alt 2, which results in total 12bits or 13bits for TDD configuration indication. As we previously noted, Z=8 bits would surely indicate more periodicity combinations without sacrificing slot granularity and more preferred, while companies argue that Z=8 bits sacrifices the reserved bits from 2 bits to 1 bit, which is too small for future extension. I want companies to further check if there indeed exists some significant problems if reducing reserved bits to 1 bit, which is the same design as NR PBCH.    Similar view with Samsung, current Alt 1 is not clear to me and I’m not sure whether that is common understanding for companies supporting alt. 1. It would be appreciated to further clarify the details of Alt 1, i.e. the reference SCS, joint indication or independent indication, to see if we can find a way to move forward. |
| ZTE | While we acknowledge Teng's assessment that slot structure misaligment including the partial slot interpretation divergence for InC and OoC UEs, we feel it would be good to put this as a note under the FL proposal given should this be common understanding. Again, we invite other companies to share your views on this.  ***FL proposals:***  ***note: The UL slot(s) derived by out of coverage UE from PSBCH should be aligned with that derived by in coverage UE from TDD-UL-DL-ConfigCommon.***  [To all]  Our understanding is that this note is essential to this proposal and the following is the reason. Currently we have Z = 7 bits in the FL proposal to indicate the UL slots, but we have not agreed to how to use these 7 bits and to us the discussions till now is to ensure  Z=7 bits with different levels of granularity loss to indicate any given slot pattern in TDD-Config-Common. Thus it makes sense to capture in the proposal this note reflecting what we've done for nearly a week :)  LGE and HW mentioned that this alignment could be done up to network configuration, which, to our understanding, leads to restrictions on TDD-Config-Common for sure given the granularity loss acknowledged previously based on FL's nice calculations. In the meantime, CMCC thinks it is not acceptable. But to us this note with the current wording essentially captures both sides' views. We agree with Sharp that 'or pre-configuration' could be considered, which is why this is preferred to be handled under this thread given the current working assumption in [structure-03] is about derivation from TDD-Config-Common only.  Notes: The UL slot(s) derived by out of coverage UE from PSBCH  or pre-configuration should be aligned with that derived by in coverage UE from TDD-UL-DL-ConfigCommon  [To all]  Thanks for further discussions and I have to say I feel sympathetic of this situation. Though we are fine not to block in the way of the FL recommendation, we anticipate that this divergence observed in my previous email will have to be resolved by May meeting.  We have the following edtorial changes proposed and hopefully they will be considered.  ·         ***For indication of TDD configuration:***  o    ***X=1 bit indicates the number of patterns***  −           ***Value 0 indicates one pattern is used.***  −           ***Value 1 indicates two patterns are used.***  o    ***Y=4 bits indicate the periodicity information***  −           ***When one pattern is used, Y indicates the periodicity of the pattern.***  −           ***When two patterns are used, Y jointly indicates the periodicities of the two patterns.***  o    ***Z=7 bits indicate the ~~UL slots~~ SL slots***  −           ***~~UL slots~~ SL slots are jointly indicated by 7 bits when two patterns are configured.***  −           ***FFS other details.***    We acknowledge the agreement from RAN1 #100e that the wording 'UL slots' have been used but it's as inaccurate as put here. The indicated slots in PSBCH is effectively measured with the SCS of SL BWP in lieu of***refSCS***as indicated in  TDD-UL-DL-ConfigCommon. UL slots here, to our understanding, will lead to undesired confusion.  [FL]  Based on the discussion by now and current situation, changing “UL slots” to “SL slots” is**NOT**acceptable by all of other companies.  1. Indicating SL slots instead of UL slots will introduce uncertainty to TDD indication in S-SSB.  2. Indicating SL slots also has higher complexity than indicating UL slots, which will make 7 bits much more insufficient.  3. By taking my FL proposal as working assumption, there is no critical issue observed by now. However, we have to re-start our discussion by changing UL slots to SL slots, because other companies are not ready to agree with the change.  4. If you do observe any critical issue in SL SYNC by indicating UL slots, you may provide analysis that can prove the current WA cannot work. Then we can discuss more on it.  [ZTE]  Thanks for the reply. However I actually don't undertand your following 2 comments and I would appreciate if you could use the example followed or another example to clarify the uncertainty/complexity claimed:  Ø  Indicating SL slots instead of UL slots will introduce uncertainty to TDD indication in S-SSB.  Ø  Indicating SL slots also has higher complexity than indicating UL slots, which will make 7 bits much more insufficient.  To respond to your 4th comment, I am taking the example of partial coverage where a UE is configured byTDD-UL-DL-ConfigCommon the 'UL slots' @SCS = 120kHz and dual pattern with 10ms + 10ms periodicty. Then 7 bits(128 combinations available) will need to indicate the SL slots at a granularity of  e.g. 8 'UL slots' to cover the up to 100 possibilities. To us, the outcome of the indication is effectively 'SL slot' taking into consideration the following agreement from RAN1 #99 meeting.  [vivo]  In our understanding, the PSBCH indicates the slots that can be used for SL, but this does not mean these slots are all SL slot. Whether the indicated slots are used for SL depends on the resource pool bitmap and S-SSB configuration. E.g. if the corresponding bit in the bitmap is set to 1, then slot is used for SL communication, if it is set to 0, then the slot is not for SL. So we think the original proposal is more accurate.  For the cases where a coarse granularity is used(SCS = 120kHz and dual pattern with 10ms + 10ms periodicity, granularity=8 slots), Z-bit resource indication=1 which implies that 8 UL slots are potential SL slots, bitmap=00001111, then only 4 SL slots exist.  [ZTE]  Considering Siqi and Tao's input, we slightly prefer option 1 from Tao given it's more concise. With 'potential' added, the concern from Siqi seems addressed also :)  ***Z=7 bits indicate the UL slots potentialSL slots***  −           ***UL slots potentialSL slots are jointly indicated by 7 bits when two patterns are configured.***  [FL]  **“UL slots” follows the agreements in RAN1#100-e.**  1.     The agreements in RAN1#100-e is “UL slots” but not “SL slots”, and please refer to this latest agreements. Besides, this agreement also followed as well as aligned with the agreements in RAN1#99 that you copied: “System-wide information, e.g. TDD-UL-DL common configurationand/or potential SL slots”. The highlighted part “and/or” means the system-wide information can or cannot be potential SL slots.  2.     Please check the email discussion in last meeting, and you can find out why “SL slots” was changed to “UL slots” and finally agreed by all companies. We had long discussion in last meeting with details, and besides technical reasons, there was also another reason that it was agreed as a compromised agreement. I think everyone does not want to re-open the gate to discuss it.  3.     @ Siqi, thank you for further explanation on “UL slots”. Because of 12 bits, both UL slots and SL slots are all losing efficient indication of granularity as I calculated it in my previous summary email.  [ZTE]  In an earlier email,  I already commented that  "The indicated slots in PSBCH is effectively measured with the SCS of SL BWP in lieu of***refSCS***as indicated in  TDD-UL-DL-ConfigCommon. UL slots here, to our understanding, will lead to undesired confusion."  and till now I received no feedback. We are providing an illustration as below for the comment. Could anyone in the group kindly clarify, according to the agreement in RAN1 #100 and the working assumption in the current FL proposal, how to indicate the 2.5 'UL' slots with Z bits in the figure if the intention is to indicate 5 potential SL slots? We checked the email discussions from last meeting as suggested by FL but we didn't find anything addressing this issue.  说明: cid:image002.png@01D61F38.F592DA40  [LGE]  I think we have agreed that the SL BWP and UL BWP have the same numerology in the shared carrier case. So the figure below is not feasible scenario. Regarding the refSCS for TDD configuration indicator in PSBCH, it could be same as or different from the SL SCS, depending on the number of UL slots to be signaled. The refSCS for bitmap is an issue of discussion in SL resource pool. In summary, I see no problem in the current FL proposal.  [ZTE]  We ackowledge it's not expected that SL BWP and UL BWP is configured different numerology on shared carrier. But I don't agree this situation is not feasible. From our understanding, this situation happens under either of the following two scenarios:  1. The reference SCS is the one indicated in TDD-UL-DL-Config common is not necessarily the one for UL BWP, thus not the same as SL BWP. This is our reading of the RAN1#99 agreement in the table.  2. Even if LGE's understanding to 1 is different from that of ours, in case the SL UEs are operating in a different carrier without the Uu, its preconfigured SCS is not necessarily the same as that of UL BWP under Uu.    Again, to us, we don't see any issue with the revision to 'potential SL slots' while the current 'UL' slots are confusing at least under the above two scenarios and we would like to fix it.  [ZTE]  I am sorry we still find the proposal is problematic.  "I think the current discussion and corresponding issue can be clearly explained the by the following figure: **Slot 1 can be used by InC UE, but slot 1 cannot be indicated in PSBCH, and slot 1 cannot be used by OoC UE for SL. Because the UL symbols in slot 1 is non-full slot (7 < UL symbols < 14). e.g. When InC UE transmits PSCCH on slot 1, OoC UE will not expect to receive anything on slot 1."**  This issue is under discussion in PHYstructure thus we are not sure whether the above is common understanding.  My reading of HiSi's email is  that they are considering the 'UL' slots may be measured by either the refSCS of the TDD-Config-Common or UL BWP and my reading of LGE's email is that the refSCS of PSBCH could also be used to interpret the 'UL' slots indicated. To us the issue is about the refSCS of the slot. Thus we think this should be reflected in your FFS.  **FL proposal:**    **For indication of TDD configuration:**  o    **X=1 bit indicates the number of patterns**  −           **Value 0 indicates one pattern is used.**  −           **Value 1 indicates two patterns are used.**  o    **Y=4 bits indicate the periodicity information**  −           **When one pattern is used, Y indicates the periodicity of the pattern.**  −           **When two patterns are used, Y jointly indicates the periodicities of the two patterns.**  o    **Z=7 bits indicate the ~~UL~~slots**  −           **UL slots are jointly indicated by 7 bits when two patterns are configured.**  −           **FFS other details. including the refSCS of the slots**    @Woo-Suk, I am not convinced on your comment that this it ITS band given I am talking about the following captured in 36.331 5.7.10.4  1> else if out of coverage on the frequency used for V2X sidelink communication as defined in TS 36.304 [4], clause 11.4; and the concerned frequency is included inv2x-InterFreqInfoList in RRCConnectionReconfiguration or in v2x-InterFreqInfoList within SystemInformationBlockType21 or SystemInformationBlockType26 of the serving cell/ PCell:  2> set inCoverage to TRUE;  2> set sl-Bandwidth to the value of the corresponding field included in v2x-InterFreqInfoList;  2> set subframeAssignmentSL and reserved to the value of the corresponding field included in the preconfigured sidelink parameters (i.e. v2x-CommPreconfigGeneral in SL-V2X-Preconfiguration defined in 9.3); |
| Sharp | Sorry for jumping into the discussion so late. We have one comment targeting the alignment with the decision to be made in sidelink structure section, i.e. for out of coverage UE, it derives UL slots via pre-configuration besides PSBCH fromSyncRef UE. Hence, we suppose it’s better to further clarify the note as“Notes: The UL slot(s) derived by out of coverage UE from PSBCH  or pre-configurationshould be aligned with that derived by in coverage UE fromTDD-UL-DL-ConfigCommon”. |
| LGE | Thank Teng for your effort in managing the thread. I’m ok with your proposal of making Alt.1 as a working assumption. But I’m not sure whether the note is necessary. As mentioned several times in the offline meetings, the coincidence issues between (pre-)configured parameters of the INC UEs and OOC UEs are always there, same as in many other cases. It seems just up to network and gNB how to manage those (pre-)configuration parameters. |
| CMCC | Thanks Teng for your great effort for on coordinating the difficult discussion. We have one comment on the note that“Notes: The UL slot(s) derived by out of coverage UE from PSBCH should be aligned with that derived by in coverage UE fromTDD-UL-DL-ConfigCommon.”    The note is unclear to me and from the discussion under structure section, it seems different companies have different understanding, i.e.  1.      the note leads to restrictions on TDD-UL-DL-Config Common in order to achieve the alignment between in-coverage and out-of-coverage UEs  2.      More specification work is needed on the rules for SL slot derivation    If the note is intended for 1), we cannot accept it, if intended for 2), we are open to discuss it. However, since this issue has been widely discussed under structure section, we suggest to remove the note here and have further discussion and decision under email thread [100b-e-NR-5G\_V2X\_NRSL-PHYstructure-03]. |
| Huawei, HiSilicon | We agree with Yi and Woo-Suk’s view. We also think the notes is not necessary as well. Actually, it make more confuse here. There are many RRC related parameters, I think RAN1 has common understanding on it, i.e. the InC configurations should be aligned with those for OoC. No need to capture a dedicated notes here. |
| vivo | One comment for clarification for the note.According to the previous discussion, a coarse granularity will inevitably be used for resource indication in some cases (e.g., 10+10 ms and SCS=120kHz), so the number of UL resources indicated by PSBCH can be different from that of TDD-UL-DL-Configcommon. I am not sure about the intention of‘aligned ’ here….Does it mean the indicated resources can be a subset of the TDD-UL-DL-Configcommon, or should be exactly the same as TDD-UL-DL-Configcommon?And I think this alignment restriction is only for operations/transmissions in the same carrier. For IC UE and OOC UE on different carriers, no need to guarantee the alignment. |
| FL | It seems like the“Note” make the proposal quite controversial now.  As many companies have strong concerns on the note which is not so clear on the intention, I would like to delete the note to make progress.  Ø This issue can discussed in another sub-agenda PHY structure that is ongoing.  Ø Another view also think that the current RRC parameters can guarantee the alignment between InC UEs and OoC UEs.    **FL comment:**  By referring to my previous email of the FL proposal (Alt 1), the Note is deleted. |
| Ericsson | After deleting the note in the FL proposal, we are supportive of Alt. 1 as a working assumption. |
| MediaTek | I tend to agree with ZTE that “SL” is more accurate than “UL” since eventually SL UE just cares “SL” but not “UL” slots.  As agreed earlier, the field in S-SSB can be used to indicate potential SL slots. So the changes are not colliding with the early agreements by adding “potential” ahead of “SL slots”, as below:  -       Indication of TDD configuration is“System-wide information, e.g. TDD-UL-DL common configuration and/or potential SL slots”  So there can be two options:  **Option 1**:***Z=7 bits indicate the ~~UL slots~~ potentialSL slots***  −           ***~~UL slots~~ potentialSL slots are jointly indicated by 7 bits when two patterns are configured.***  **Option 2**:***Z=7 bits indicate the UL slots***  −           ***UL slots are jointly indicated by 7 bits when two patterns are configured.***   ***All UL slots are also the potential SL slots***  Either way is fine for us.  Then what about taking Option 2 by adding one sentence marked in red below, i.e.,  **Option 2**:***Z=7 bits indicate the UL slots***  −           ***UL slots are jointly indicated by 7 bits when two patterns are configured.***   ***All UL slots are also the potential SL slots***    We want to exclude the case that the indicated UL slots can’t be the potential SL slots. Otherwise, we have to further discuss which UL slots can be the potential UL slots. |
| FL | @Woo-Suk, Siqi  Thanks for your further explanation on the current issue.    @Yuzhou,  As Woo-Suk pointed out based on the agreement: UE on SL BWP is not expected to have different numerology from that on UL BWP. However, I understand you concerns that some slots (UL symbol < 14) cannot used for potential SL UE. InC UE and OoC UE will have different understanding on the UL slots that potentially can be used for SL transmissions. Based on the current agreements, how to indicate non-full UL slots in PSBCH is still un-known, and this issue is also discussed in PHY structure. That is what you want to clarify. This is why I put **FFS details** in the FL proposal. We already have the FFS details, and all of potential indication solutions can be determined by next meeting. If my following explanation and figure is your concerns, there is no necessary to add any notes to the current proposal.  Besides, for different carrier, there is no such issue need to worry about, because this issue does not exist.    @Tao,  Regarding the wording proposed by MediaTek, “**All UL slots are also the potential SL slots**”, I think it is common understanding that on the shared carrier, SL slots resource is a subset of UL slots resource. Whether the UL slots can be used as SL depending on its bitmap setting. The FFS part will also include how the UL slots are indicated to be potentially used by SL. We do not need to add more restrictions on the FFS part.    **@all,**    We have only 12 bits (1 pattern + 4 period + 7 UL slots). Due to lack of bits, we can only indicate part of the whole UL slots in PSBCH. This is a compromised result agreed by all of the companies.    I think the current discussion and corresponding issue can be clearly explained the by the following figure: **Slot 1 can be used by InC UE, but slot 1 cannot be indicated in PSBCH, and slot 1 cannot be used by OoC UE for SL. Because the UL symbols in slot 1 is non-full slot (7 < UL symbols < 14). e.g. When InC UE transmits PSCCH on slot 1, OoC UE will not expect to receive anything on slot 1.**    说明: cid:image001.png@01D61F38.F592DA40    **FL proposal:**  l  **For indication of TDD configuration:**  o    **X=1 bit indicates the number of patterns**  −           **Value 0 indicates one pattern is used.**  −           **Value 1 indicates two patterns are used.**  o    **Y=4 bits indicate the periodicity information**  −           **When one pattern is used, Y indicates the periodicity of the pattern.**  −           **When two patterns are used, Y jointly indicates the periodicities of the two patterns.**  o    **Z=7 bits indicate the UL slots**  −           **UL slots are jointly indicated by 7 bits when two patterns are configured.**  −           **FFS other details.** |
| LGE | I’m fine with the proposal and most of the comments below except one point, that is, the definition of the UL slot.   In your figure below for example, the slot 1 can be signaled as UL slot if the slot satisfies the SL BWP configuration condition in terms of the start and the length of SL symbols within a slot. We didn’t decide yet as you said, so may be discussed further as a FFS point. It’s also related to the SL resource pool configuration discussion. Therefore it’s not fixed yet that the slot 1 cannot be used as SL slot by OOC UE, as depicted in the figure.   Hope we can further clarify this point next time. |
|  |  |