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DSCH Data Rate in UE Capabilities

Introduction.

In last WG2 is was agreed to have parameter "maximum number of bits received during 10 ms for the TTIs (Transmission Time Intervals) that end at the same time". In connection with this it was noted that DSCH (or PDSCH) has some differences as it has frame offset as indicated in Figure 1 with respect to the associated dedicated channel. This contribution proposes the relevant note to clarify the issue in WG2 technical report. This is proposed to be liased to TSG RAN WG2 for the inclusion of the TR on UE capabilities.

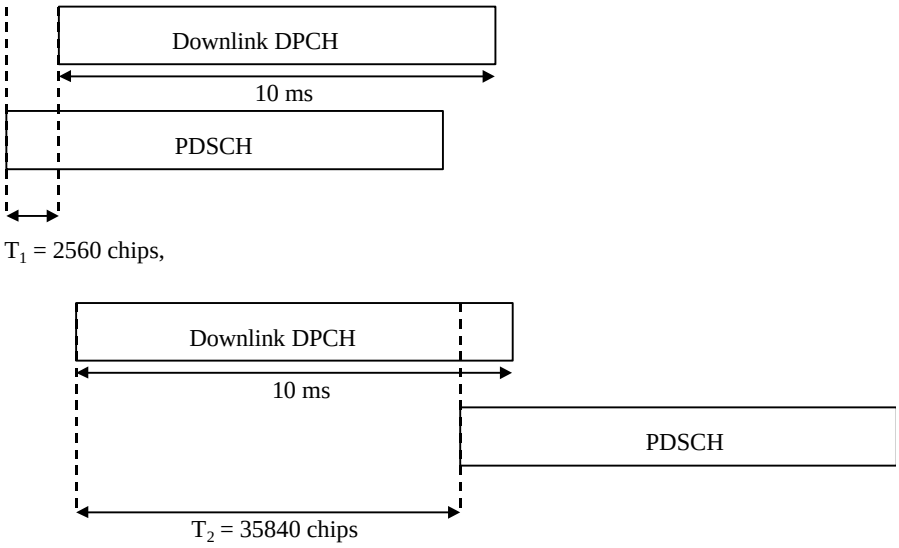

Figure 1. DSHC & DCH timing relation (extreme cases). Note: I could be changed so that T1=0 and T2 max 10 ms. This would minimise the memory requirements.

DSCH channel reception capability vs. DCH reception capability.

- For the despreading hardware there is no impact due difference in timing what so ever compared to a DCH that has the same spreading factor and has aligned frame timing. (The DSCH has naturally varying spreading factor). Point to note in WG2 modelling is that in WG2 specifications the multiple DSCHs means multicode DSCH transmission which is in WG1 specifications described as mapping a single DSCH to multiple PDSCHs. This is a terminology alignment question which just needs to be sorted with WG2. In this respect the earlier parameter in WG2 specification was understandable, support of for more than one PDSCH.

- For the total channel coding effort, the DSCH effect has impact at which point of time the decoding can be done, as such the amount of bits on a DSCH needs the same effort from channel decoding than the same number of bits on a DCH. The impact can be compoensated by having a note that the DSCH decdoding may be completed max 10 ms later than the decoding of the DCH data. This is to compensate for the maximum of 14 slots delay compared to the DCH. As DSCH is intended for NRT data there should be no problems due this, but it's proper to mention for delay budget calculation reasons.

DSCH memory requirements vs. DCH memory requirements

- As the DSCH may be one slot ahead of the associated DCH, it may in such a case require one slot extra memory compared to the DCH. This is not proposed to be reflected in any of the parameter values but should be covered by the individual implementation with a proper note in the UE capabilites (This assuming the memory related parameter proposed is liaised to WG2 to be included in the TR on UE capabilites.) This could be changed also by defining the DSCH timing that it starts always at the same time or max 15 slots later the the DCH frame to avoid even this one slot of extra memory.

What to liaise to W2

- On the proposessing power WG2 should be informed "The DSCH decoding effect has been included in the associated DCH frame for the TTIs that end during the same time. Thus a UE when declaring certain capability of bits that can be handled in 10ms period, can support the same number of bits on the DCH or jointly on the DCH and DSCH. "

- Further if the memory related parameter is to be communicated to WG2, it should be said "The DSCH related memory increase due frame offset shall be accomodated by the implementation of DSCH capable terminals. Such a terminals shall have the same DSCH+DCH data rate capability regardless on the timing offset between DCH and DSCH."

- Further in general the DSCH with multicode capability needs to be explained to WG2 and either WG2 or WG1 (or both) specifications need to be aligned with this respect.

In general more detailed definitions are are difficult as there exists some implementation trade-off possibilites between the memory requirment and processing power available. It's up for the each vendor to take care that their memory/processing power capability actually in the terminal can cove with the declared data rates with DCH and with DCH and DSCH. Similar differences may occur in the timing between FACH and DCH as well when simulatenous decoding is needed.

Thus in a similar way if simulatenous decoding of DCH and FACH (S-CCPCH) is supported, the data joint data rate would be indicated on the UE capability. This might need some further consideration though.