TSG-RAN Working Group1 meeting #6
Espoo, Finland 13-16, July 1999

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Agenda Item:

Source: **NTT DoCoMo**

Title: **Modified Multistage InterLeaver (MIL) fit for 15-slot frame**

Document for: **Decision**

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1. Introduction

In the last WG1 meeting #5, the modified MIL [1] was approved for the channel interleaving of both 1st interleaving and 2nd interleaving and also a further indication on the solution used if the number of slots per frame is changed to 15 was requested [2]. Accordingly, NTT DoCoMo investigated about the optimisation of the modified MIL scheme fit for the new frame structure with 15-slot. We then found the reasonable solution under maintaining BER/FER performance. In this document, such fitting modified MIL scheme for 15-slot frame and its text for TS 25.212 and TS 25.222 are proposed.

2. Proposed modified MIL scheme fit for 15-slot frame

In the solution for 15-slot frame, the only modification of 2nd (intra-frame) interleaving part is done and the 1st (inter-frame) interleaving is not changed at all (this means the channel interleaving modification would not affect the uplink puncturing scheme [3] basically). The modifications of 2nd interleaving are as follows:

(1) The number of column was changed from 32 to 30.
(2) Inter-column permutation pattern which is optimised for 30-column was introduced.

Regarding (1), the 2nd interleaving with 30-column could allow easily performing the uniform DTX placement for all slot in a downlink frame if DTX indication bits are inserted before 2nd interleaving. This is an advantage for total processing load in multiplexing/coding chain because no extra processing is needed for the determination of the uniform DTX placement in the physical channel mapping. Regarding (2), there are some possibilities that the 30-column pattern is made by some partial transformation e.g. bit deleting for the original 32-column pattern. However, this kind of transformed pattern would not be the optimum pattern. Therefore, we introduced a new pattern that is a most optimum pattern for 30-column (see Table 1). Note that the hardware complexity is not different between both cases of using a partial transformed (non-optimum) pattern and an optimum pattern.

Table 1. Inter-column permutation pattern for 2nd interleaving

Number of columns	Inter-column permutation pattern
30	{0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17}

3. Text proposal for 25.212 (and 25.222)

4.2.10 (6.2.8) 2nd interleaving

The 2nd interleaving of channel interleaving consists of two stage operations. In first stage, the input sequence is written into rectangular matrix row by row. The second stage is inter-column permutation. The two-stage operations are described as follows, the input block length is assumed to be K_2.

First Stage:

(1) Set a column number C_2 = ~~32~~30.
(2) Determine a row number R_2 by finding minimum integer R_2 such that,

$$K_2 <= R_2 \times C_2.$$

(3) The input sequence of the 2nd interleaving is written into the $R_2 \times C_2$ rectangular matrix row by row.

Second Stage:

(1) Perform the inter-column permutation based on the pattern $\{P_2(j)\}$ (j=0,1, ..., C-1) that is shown in Table 4-4 (Table 6.2.8-1), where $P_2(j)$ is the original column position of the j-th permuted column.
(2) The output of the 2nd interleaving is the sequence read out column by column from the inter-column permuted $R_2 \times C_2$ matrix and the output is pruned by deleting the non-existence bits in the input sequence, where the deleting bits number l_2 is defined as:

$$l_2 = R_2 \times C_2 - K_2.$$

Table 4-4 (Table 6.2.8-1)

Column number C_2	Inter-column permutation pattern
30	{0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17}

~~Column number C_2~~	~~Inter-column permutation patterns~~
~~32~~	~~{0, 16, 8, 24, 4, 20, 12, 28, 18, 2, 26, 10, 22, 6, 30, 14, 17, 1, 25, 9, 21, 5, 29, 13, 3, 19, 11, 27, 7, 23, 15, 31}~~

References

[1] NTT DoCoMo, “Modified Multistage InterLeaver (MIL) for Channel Interleaving”, TSGR1#5(99)662
[2] Ad hoc #4 chair, “Ad hoc #4 report”, TSGR1#5(99)693
[3] Siemens, “Text proposal for optimised puncturing”, TSGR1#5(99)703