TSG-RAN Working Group1 meeting #6
Espoo, Finland 13-16, July 1999

TSGR1#6(99)927

Agenda Item:

Source: **NTT DoCoMo, Nortel Networks and SAMSUNG Electronics Co.**

Title: **Updated text proposal for Turbo code internal interleaver**

Document for: **Decision**

Introduction

This document proposes an updated text for the approved Turbo code internal interleaver [1], [2], [3] of documents TS 25.212 and TS 25.222. In this update, the editorial changes are made to exactly reflect that the maximum Turbo-coding block size was changed from 8192-bit to 5120-bit [4] (this has been approved in RAN WG1 meeting #5).

Text proposal for TS 25.212 (and TS 25.222)

4.2.3.2.3 (6.2.3.2.3) Turbo code internal interleaver

Figure 4-6 (Figure 6-5) depicts the overall 8-state PCCC Turbo coding scheme including Turbo code internal interleaver. The Turbo code internal interleaver consists of mother interleaver generation and pruning. For arbitrary given block length K, one mother interleaver is selected from the ~~207~~ 134 mother interleavers set. The generation scheme of mother interleaver is described in section 4.2.3.2.3.1 (section 6.2.3.2.3). After the mother interleaver generation, *l*-bits are pruned in order to adjust the mother interleaver to the block length K. The definition of *l* is shown in section 4.2.3.2.3.2 (section 6.2.3.2.3.2).

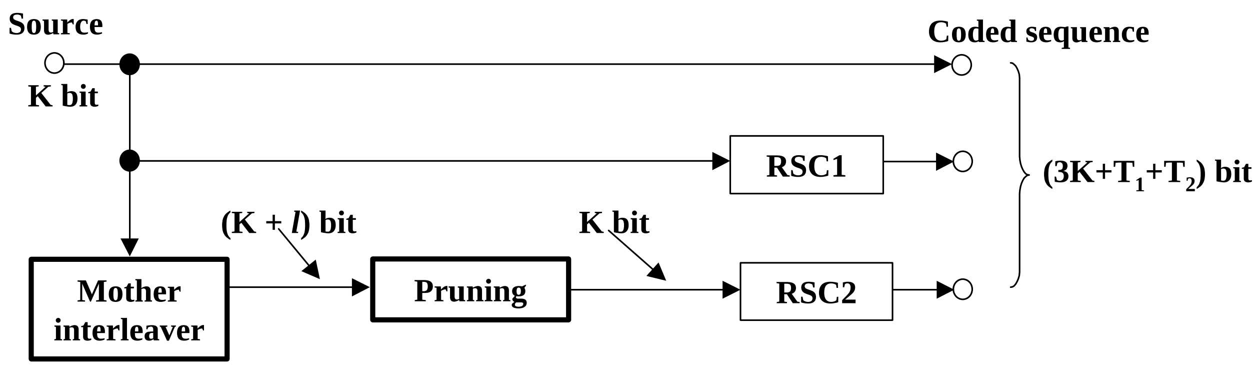

Figure 4-6 (Figure 6-5). Overall 8-state PCCC Turbo Coding

4.2.3.2.3.1 (6.2.3.2.3.1) Mother interleaver generation

The interleaving consists of three stages. In first stage, the input sequence is written into the rectangular matrix row by row. The second stage is intra-row permutation. The third stage is inter-row permutation. The three-stage permutations are described as follows, the input block length is assumed to be K (320 to 5120 bits).

First Stage:

(1) Determine a row number R such that

R=10 (K = 481 to 530 bits; Case-1)

R=20 (K = any other block length except 481 to 530 bits; Case-2)

(2) Determine a column number C such that

Case-1; C = p = *53*

Csae-2;

(i) find minimum prime p such that,

$0 =< (p+1)$-K/R,

(ii) if ($0 =< p$-K/R) then go to (iii),

else C = p+1.

(iii) if ($0 =< p$-1-K/R) then C=p-1,

else C = p.

(3) The input sequence of the interleaver is written into the RxC rectangular matrix row by row.

<u>Second Stage:</u>

<u>A. If C = p</u>

(A-1) Select a primitive root g_0 from Table 4-2 (Table 6.2.3-2).

(A-2) Construct the base sequence $c(i)$ for intra-row permutation as:

$$c(i) = [g_0 \times c(i-1)] \bmod p \text{ , } i = 1,2,\ldots, (p\text{-}2)., \ c(0) = 1.$$

(A-3) Select the minimum prime integer set $\{q_j\}$ (j=1,2,…R-1) such that

g.c.d$\{q_j, p\text{-}1\}$ =1

$q_j > 6$

$q_j > q_{(j-1)}$

where g.c.d. is greatest common divider. And $q_0 = 1$.

(A-4) The set $\{q_j\}$ is permuted to make a new set $\{p_j\}$ such that

$p_{P(j)} = q_j$, j = 0, 1, …. R-1,

where P(j) is the inter-row permutation pattern defined in the third stage.

(A-5) Perform the j-th (j = 0, 1, 2, …, R-1) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod (p-1)) \text{ , } \quad i = 0, 1,2,\ldots, (p\text{-}2)., \text{ and } c_j(p\text{-}1) = 0,$$

where $c_j(i)$ is the input bit position of i-th output after the permutation of j-th row.

<u>B. If C = p+1</u>

(B-1) Same as case A-1.

(B-2) Same as case A-2.

(B-3) Same as case A-3.

(B-4) Same as case A-4.

(B-5) Perform the j-th (j = 0,1, 2, …, R-1) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod (p-1)) \text{ , } \quad i = 0,1,2,\ldots, (p\text{-}2)., \ c_j(p\text{-}1) = 0, \text{ and } c_j(p) = p,$$

(B-6) If (K = C x R) then exchange $c_{R-1}(p)$ with $c_{R-1}(0)$.

where $c_j(i)$ is the input bit position of i-th output after the permutation of j-th row.

<u>C. If C = p-1</u>

(C-1) Same as case A-1.

(C-2) Same as case A-2.

(C-3) Same as case A-3.

(C-4) Same as case A-4.

(C-5) Perform the j-th (j = 0,1, 2, …, R-1) intra-row permutation as:

$$c_j(i) = c([i \times p_j] \bmod (p-1)) \text{ -1, } \quad i = 0,1,2,\ldots, (p\text{-}2),$$

where $c_j(i)$ is the input bit position of i-th output after the permutation of j-th row.

Third Stage:

(1) Perform the inter-row permutation based on the following P(j) (j=0,1, ..., R-1) patterns, where P(j) is the original row position of the j-th permuted row.

P_A: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11} for R=20

P_B: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10} for R=20

P_C: {9, 8, 7, 6, 5, 4, 3, 2, 1, 0} for R=10

The usage of these patterns is as follows:

Block length K: P(j)
320 to 480-bit: P_A
481 to 530-bit: P_C
531 to 2280-bit: P_A
2281 to 2480-bit: P_B
2481 to 3160-bit: P_A
3161 to 3210-bit: P_B
3211 to 5120-bit: P_A

(2) The output of the mother interleaver is the sequence read out column by column from the permuted R × C matrix.

Table 4-2 (Table 6.2.3-2). Table of prime p and associated primitive root

p	g_0	p	g_0	p	g_0	p	g_0	p	g_0
17	3	59	2	103	5	157	5	211	2
19	2	61	2	107	2	163	2	223	3
23	5	67	2	109	6	167	5	227	2
29	2	71	7	113	3	173	2	229	6
31	3	73	5	127	3	179	2	233	3
37	2	79	3	131	2	181	2	239	7
41	6	83	2	137	3	191	19	241	7
43	3	89	3	139	2	193	5	251	6
47	5	97	5	149	2	197	2	257	3
53	2	101	2	151	6	199	3		

~~p~~	~~g0~~	~~p~~	~~g0~~	~~p~~	~~G0~~	~~p~~	~~g0~~	~~p~~	~~g0~~	~~p~~	~~g0~~	~~p~~	~~g0~~	~~p~~	~~g0~~
~~17~~	~~3~~	~~59~~	~~2~~	~~103~~	~~5~~	~~157~~	~~5~~	~~211~~	~~2~~	~~269~~	~~2~~	~~331~~	~~3~~	~~389~~	~~2~~
~~19~~	~~2~~	~~61~~	~~2~~	~~107~~	~~2~~	~~163~~	~~2~~	~~223~~	~~3~~	~~271~~	~~6~~	~~337~~	~~10~~	~~397~~	~~5~~
~~23~~	~~5~~	~~67~~	~~2~~	~~109~~	~~6~~	~~167~~	~~5~~	~~227~~	~~2~~	~~277~~	~~5~~	~~347~~	~~2~~	~~401~~	~~3~~
~~29~~	~~2~~	~~71~~	~~7~~	~~113~~	~~3~~	~~173~~	~~2~~	~~229~~	~~6~~	~~281~~	~~3~~	~~349~~	~~2~~	~~409~~	~~21~~
~~31~~	~~3~~	~~73~~	~~5~~	~~127~~	~~3~~	~~179~~	~~2~~	~~233~~	~~3~~	~~283~~	~~3~~	~~353~~	~~3~~		
~~37~~	~~2~~	~~79~~	~~3~~	~~131~~	~~2~~	~~181~~	~~2~~	~~239~~	~~7~~	~~293~~	~~2~~	~~359~~	~~7~~		
~~41~~	~~6~~	~~83~~	~~2~~	~~137~~	~~3~~	~~191~~	~~19~~	~~241~~	~~7~~	~~307~~	~~5~~	~~367~~	~~6~~		
~~43~~	~~3~~	~~89~~	~~3~~	~~139~~	~~2~~	~~193~~	~~5~~	~~251~~	~~6~~	~~311~~	~~17~~	~~373~~	~~2~~		
~~47~~	~~5~~	~~97~~	~~5~~	~~149~~	~~2~~	~~197~~	~~2~~	~~257~~	~~3~~	~~313~~	~~10~~	~~379~~	~~2~~		
~~53~~	~~2~~	~~101~~	~~2~~	~~151~~	~~6~~	~~199~~	~~3~~	~~263~~	~~5~~	~~317~~	~~2~~	~~383~~	~~5~~		

4.2.3.2.3.2 (6.2.3.2.3.2) Definition of number of pruning bits

The output of the mother interleaver is pruned by deleting the l-bits in order to adjust the mother interleaver to the block length K, where the deleted bits are non-existent bits in the input sequence. The pruning bits number l is defined as:

l = R×C – K,

where R is the row number and C is the column number defined in section 4.2.3.2.3.1 (section 6.2.3.2.3.1).

References

[1] NTT DoCoMo and Nortel Networks, "Text proposal for Turbo code internal interleaver of S1.12, S1.22", TSGR1#4(99)471
[2] NTT DoCoMo and Nortel Networks, "Updated text for Turbo code internal interleaver of 25.212, 25.222", TSGR1#5(99)540
[3] SAMSUNG electronics Co., NTT DoCoMo and Nortel Networks, "Agreement of incorporating PIL modification into 25.212, 25.222", TSGR1#5(99)735
[4] Nokia, "Maximum turbo coding block size: text proposal", TSGR1#5(99)549