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Comparison between fixed-step and adaptive-step closed loop power control algorithms in compressed mode

Abstract: Two different types of algorithms are currently proposed for closed-loop power control in compressed mode: adaptive-step and fixed-step algorithms.
This contribution presents simulation results showing that the adaptive-step algorithm has lower performances than fixed-step proposals due to the high sensitivity of the adaptive-step algorithm to errors (power control command errors, channel estimation errors, SIR estimation errors, …). Moreover, the adaptive-step proposal significantly increases the system complexity (modification of the slot structure, power offsets by a fractional number of dB within each slot, increased peak-to-average ratio,…).

1 Introduction

Different proposals are currently discussed for power control algorithm in compressed mode. All proposals aim to hasten the recovery of a SIR (signal-to-interference ratio) closed the target SIR after each transmission gap.

In this contribution, we evaluate the complexity and performances of different schemes with the simulation parameters agreed at the last meeting. The evaluated schemes are :

- FSPC-1, FSPC-2, FSPC-3 : fixed-step algorithm, where the same algorithm as in normal mode is applied but with a larger step size (2 dB instead of 1 dB) during a few slots after each transmission gap (called recovery period). This scheme is evaluated with a recovery period length of 8 slots (FSPC-1) or 16 slots (FSPC-2). The algorithm FSPC-3 is identical to FSPC-2 but with 2 additional TPC bits on the reverse link in order to improve the reliability of power control commands.
- FSPC-4: fixed-step algorithm, where the same algorithm as in normal mode is applied but with a larger step size (2 dB instead of 1 dB) after each transmission gap. We revert to the normal algorithm when we observe a sign inversion in the received power control commands. Thus, the recovery period length is not fixed but adapted for each recovery period.
- ASPC : adaptive-step algorithm, where the step size can take 4 values (0, 1, 2 and 3 dB) and is adapted during 16 slots after each transmission gap. The step size is indicated via a power offset

between the TPC symbols and the previous symbols. Additionally, the pilot symbols power is increased by 2 dB or a second field with 60% additional pilot symbols is added before the TPC bits in case of DTX in downlink.

2 Slot structure

In downlink compressed mode, when DTX is used at the end of the first data field, 60% additional pilot symbols are added between the first data field and TPC symbols for the adaptive-step proposal. Thus, this proposal requires to change the slot structure of the downlink signal during several slots after each transmission gap in case of DTX.
This will increase the modulation and channel estimation complexity for the adaptive-step power control algorithm, since two different slot-structures will have to be considered.

Fixed-step power control algorithms present the advantage of an unchanged slot structure by comparison (however, FSPC-3 requires to add 2 TPC bits during recovery frames).

3 Power offsets

For the fixed-step power control algorithms, the power of each field is the same as in normal mode.

For the adaptive-step power control algorithm, the power variations during each slot can be significant. Indeed :
- the pilot symbols have an energy 2 dB larger than the data symbols (except in downlink with DTX),
- the TPC symbols are either not transmitted (when the step size is 0 dB) or are transmitted with an energy that depends of the step size and that can be up to 4.8 dB larger than the data symbols in both downlink and uplink.

Therefore, the adaptive-step algorithm (ASPC) will have several impacts on the system performances and complexity, such as:

- **Power amplification**

First, the accurate control of the power offsets will have to be done in the digital part, since the analog power amplifiers have a too long reaction time to be able to vary the power for only one or two bits. This will increase the required resolution of the digital-to-analog converter. Moreover, the power control will have to be balanced between the analog and digital parts since the dynamic range of the digital part will not be sufficient for the required accuracy. Thus, this will increase the UE transmitter complexity. Furthermore, the average increase of power per slot is about
- 0.371 dB if the step is 0 dB,
- 0.629 dB if the step is 1 dB,
- 0.872 dB if the step is 2 dB,
- 1.108 dB if the step is 3 dB,

Such an accuracy seems to be hardly achievable. It would require too many bits for quantification if amplification is performed in the digital part and such an accuracy cannot be achieved with analog amplification.

- **Peak-to-average ratio/Cell range**

In uplink, the large power variations during each slot will increase significantly the peak-to-average ratio and therefore will require a power amplifier of higher grade.
In addition, the cell range will have to be reduced because of the necessity to keep some margin for the power increase that is required in the adaptive-step proposal. Otherwise, near cell boundaries where compressed mode is expected to be needed, it will not be possible to have this power increase for pilot

and TPC symbols (since the transmit power will be closed to the maximum transmit power).

- **Interference seen by other users**

For the adaptive-step algorithm, the power increase for TPC and pilot symbols during each slot will increase the interference seen by other users and will therefore decrease their performances. This interference increase is not negligible since the TPC symbols power can be up to 4.8 dB above the data bits power. This is not taken into account in the presented link level simulations but will have some additional negative effect on the system capacity.

4 Uplink/downlink schemes

The adaptive-step power control proposal is different in uplink and downlink because of the second field of pilot bits that is added in downlink in case of DTX.

On the other hand, the fixed-step power control algorithms offer identical schemes in uplink and downlink, which makes these algorithms more attractive.

5 Impact of harmonization process

The harmonization process does not impact the fixed-step power control algorithms.

However, it will affect the adaptive-step proposal. Indeed, it is likely that the number of pilot bits of the DPCCH will be reduced to 0 or 2 because of the common pilot channel and that the channel estimation is done on the common pilot channel (except when smart antennas are used). It will impact the adaptive-step power control algorithm, since the pilot bits were used to improved the reliability of the power-offset measurements.

6 Link-level performances

As agreed in the last WG1 meeting, the link-level performances of the different schemes have been compared for speech service, pedestrian A environment, SIR estimation performed on pilot bits and speed ranging from 3 to 100 km/h. Detailed parameters are given in appendix.

In these link-level simulations, both links are simulated at the same time in order to have very accurate modeling of power control commands. Each link has been simulated at the chip level, thus taking into account spreading, scrambling and inter-chip interference created by the channel.

Simulation results are shown for the uplink, where the power control algorithm applied on the uplink power control is one of the proposed algorithms and the downlink power control algorithm is always the standard power control algorithm (the power control step is always 1 dB). The E_b/N_0 of the reverse link is the target E_b/N_0 and is the same for all schemes (but depends on the speed).

For each speed, four outputs are shown as agreed in the last meeting:
- The target Eb/N0 for a BER of 10^{-3} when the BER is averaged over all frames,
- The received SIR variance taking into account all frames (given for the target Eb/N0),
- The target Eb/N0 for a BER of 10^{-3} when the BER is averaged over recovery frames (a recovery frame is the first frame after a compressed frame),
- The received SIR variance taking into account only recovery frames (given for the target Eb/N0).

The most important output is obviously the first one since the target Eb/N0 when the BER is averaged over all frames has a direct impact on the required transmit power and thus on the system capacity.

Therefore, when the Eb/N0 are different, the scheme with lowest Eb/N0 is better.

When the Eb/N0 are equal for two schemes, the SIR variance (when averaged over all frames) can then be considered to know which scheme is the best since it will have an impact on the interference seen by other users. However, this impact will be low compared to the impact of the target E_b/N_0.

The two outputs on the recovery frames give useful information but must be analyzed very carefully, since the performances of the frames just following the recovery frames are not always equal for the different algorithms. Thus, a scheme that performs better during the recovery frames can have globally lower performances. Therefore, the two first outputs must be rather considered to compare the different schemes, since they take into account all frames.

6.1 Target Eb/N0 when BER averaged over all frames

Speed (km/h)	FSPC-1	FSPC-2	FSPC-3	FSPC-4	ASPC
3	7.85	7.9	**7.8**	8.05	7.9
10	9.4	9.4	**9.4**	9.65	9.5
20	**10.25**	**10.25**	**10.25**	10.35	**10.25**
40	**11.05**	11.15	11.1	11.25	11.25
100	10.8	11.1	11.1	**10.75**	11.1

Table 1: target E_b/N_0 for a BER of 10^{-3}, when BER averaged over all frames

These simulation results show that FSPC-1, FSPC-2 and FSPC-3 perform identically or better than the adaptive-step power control algorithm (ASPC) for all speeds. The best performances are obtained with FSPC-1 and FSPC-3, the gain over the adaptive-step algorithm being up to 0.3 dB. Since FSPC-1 is less complex than FSPC-3, we believe that FSPC-1 is preferable.

The performance degradation of the adaptive-step power control algorithm is mainly due to the increased energy overhead of this proposal due to larger energy on pilot and TPC bits and to the fact that the step is not well adapted because of errors.

This performances loss of the adaptive-step proposal does not include other performances degradations that can be caused by other effects mentioned in previous sections: increased peak-to-average ratio, …

6.2 SIR variance averaged over all frames

Speed (km/h)	FSPC-1	FSPC-2	FSPC-3	FSPC-4	ASPC
3	3.3	3.7	3.5	**3**	3.3
10	5.9	6.1	5.9	5.8	**5.7**
20	11.4	11.2	**11.0**	11.3	**11.0**
40	17.7	17.1	17.1	17.7	**16.8**
100	23.0	23.2	23.0	22.8	**22.7**

Table 2: SIR variance for the target E_b/N_0 averaged over all frames

The SIR variance is larger for the fixed-step power control proposals, except at 3 km/h. This is mainly due to the lower TPC error rates in the adaptive-step power control. However, this difference of SIR variances will have a negligible impact on the system capacity since it is only significant when the SIR variance is already pretty large (>10 dB). Thus, the decision between the different schemes should be mainly based on the target E_b/N_0 given in table 1.

6.3 Target Eb/N0 for a BER of 10^{-3} when BER averaged over recovery frames

Speed (km/h)	FSPC-1	FSPC-2	FSPC-3	FSPC-4	ASPC
3	8.1	8.1	**7.55**	8.6	8.2
10	9.8	9.4	**9.1**	10.15	**9.1**
20	10.5	10.4	**9.65**	11.2	10.1
40	10.95	10.4	**9.85**	11.6	10.0
100	10.6	**10.15**	10.2	10.9	10.4

Table 3: target E_b/N_0 for a BER of 10^{-3}, when BER averaged **only over recovery frames**

For the fixed-step proposal, the simulation results of table 3 show that a recovery period of 16 slots (FSPC-2) instead of 8 (FSPC-1) enables to improve the performances during the recovery frames. However, as shown in section 6.1, the overall performances (i.e. when the BER is averaged over all frames) of FSPC-2 are lower than the performances of FSPC-1. Indeed, when the recovery period length is 16 slots, the BER in the frame just following the recovery frame is also impacted and has degraded performances than when the recovery period length is 8 slots (this has been checked by simulations). Thus, globally, FPSC-1 is better than FPSC-2.

These simulation results also show that a larger reliability on TPC commands (obtained with a larger energy on TPC bits for ASPC or additional TPC bits for FSPC-3) enable to improve significantly the performances during the recovery frames compared to FSPC-2.
The overall performances of FSPC-3 are also slightly better than FSPC2. However, the overall performances of ASPC are lower than FSPC-2 (see section 6.1). Indeed :
- The average BER in the frame just following the recovery frame is usually larger for ASPC than for FSPC-2.
- The energy overhead of the ASPC scheme is significant (around 0.2 dB).

Also note that FSPC-3 has equal or better performances than ASPC at all speeds which enables to show that the gain of ASPC over FSPC-1 and FPSC-2 during recovery frames is mainly due to the increase energy on TPC bits, and not to the adaptive step. This increased reliability can also be achieved by fixed-step proposals (as shown with FSPC-3) still keeping a much lower complexity than ASPC. However, since FSPC-3 has globally not better performances than FSPC-1 but a larger complexity, we rather suggest that FSPC-1 be chosen.

6.4 SIR variance averaged on recovery frames

Speed (km/h)	FSPC-1	FSPC-2	FSPC-3	FSPC-4	ASPC
3	4.7	5.7	5.1	**3.7**	4.3
10	7.1	7.5	6.9	7	**6.2**
20	12.3	11.6	**10.7**	12.6	**10.7**
40	17.4	15.3	14.5	17.5	**13.4**
100	23.8	23.5	22.6	23.2	**21.7**

Table 4: SIR variance for the target E_b/N_0 averaged **only over recovery frames**

The same comments as in section 6.2 apply. Additionally, as mentioned in the previous section, the SIR variance in frame just following recovery frame is also impacted by the different schemes and is not taken into account in Table 4. Thus, Table 2 where the SIR variance is averaged over all frames should rather be considered to compare the different schemes.

7 Conclusion

The fixed-step power control proposal FSPC-1 has been previously shown to improve significantly the performances compared to ordinary power control algorithm with step size always equal to 1 dB (up to 1.1 dB, see [1], [2] and [3]). This proposal is very simple and implies almost no change since the same power control algorithm as in normal mode is applied but with a larger step size.

On the other hand, the adaptive-step proposal presents degraded performances at the cost of a higher complexity (change of slot structure, power change up to 4.8 within each slot, …).

Thus, we recommend that the fixed-step proposal FSPC-1 be included in the specifications. Since the additional complexity to have different variants of the scheme FSPC-1 is very low, we believe that we should allow a few variants to have optimize performances in all situations, as proposed in [9].

8 References

[1] UMTS RAN WG1 TSGR#4(99)342, "Improved closed loop power control algorithm in slotted mode" (Alcatel), *April, 99*.

[2] UMTS RAN WG1 TSGR#5(99)542, "Additional results for fixed-step closed loop power control algorithm in compressed mode" (Alcatel), *June, 99.*

[3] UMTS RAN WG1 TSGR#5(99)544, " Parameters setting for fixed-step closed loop power control algorithm in compressed mode" (Alcatel), *June, 99.*

[4] UMTS RAN WG1 TSGR#5(99)638, Comparison between fixed-step and adaptive-step closed loop power control algorithms in compressed mode" (Alcatel), *June, 99.*

[5] UMTS RAN WG1 TSGR#4(99)409, "Adaptive Step Power Control (ASPC) for Slotted Mode" (Panasonic), *April, 99.*

[6] UMTS RAN WG1 TSGR#5(99)586, "Comparative results for power control schemes associated with compressed mode " (Panasonic), *June, 99.*

[7] UMTS RAN WG1 TSGR#5(99)649, "Power offset estimation in ASPC method" (Nokia), *June, 99.*

[8] UMTS RAN WG1 TSGR#5(99)822, "Optimum Recovery Period Power Control Algorithms for Slotted Mode " (Philips), *July, 99.*

[9] UMTS RAN WG1 TSGR#5(99)881, "Text proposal for specifications 25.214 and 25.231 on power control in compressed mode" (Alcatel, Nortel, Philips), *July, 99*

Appendix: detailed simulation parameters

Parameters	Values, assumptions, …
Service	**Speech**
Carrier frequency	2 GHz
Channel	Indoor to Outdoor and Pedestrian A channel where the delays of the different paths are multiple of the chip period.
Type of simulations	Both links are simulated at the same time at chip level.
Link direction for which the performances are estimated	Uplink
Uplink power control	- Infinite dynamic range, - One-slot delay - The power-control algorithm is one of the proposed algorithm in recovery zones or the standard power control algorithm with step equal to 1 dB otherwise.
Downlink power control	- Infinite dynamic range, - One-slot delay - The power-control algorithm is always the standard power control algorithm with step size equal to 1 dB.
Eb/N0 scaling	Eb is computed as the received power for each information bit including all overhead (coding, tail, pilot, TPC, TFCI, rate matching, CRC)
Rake receiver	2 fingers. An ideal path searcher with fixed delays is used. The oversampling rate is the chip rate.
Channel estimation method	Channel estimation is based on the present pilot group and pilot groups before and after the present slot. The different pilot groups are multiplied by a weighting factor. The different weights only depend on speed and are : - 3 km/h : (1, 1, 1, 1, **1**, 1, 1) - 10 km/h : (1, 1, 1,1, **1**, 1, 1) - 20 km/h : (0.9, 1, 1, 1, **1**, 1, 1) - 40 km/h : (0.7, 0.8, 0.9, 1, **1**, 1, 0.9) - 100 km/h: (0.2, 0.6, 0.9, **1**, 0.9, 0.6) where the current slot has the weight in bold font.
Slotted mode	Transmission gap period (TGP) = 64 slots. Transmission gap length (TGL) = 8 slots. The Transmission gap is at the end of the compressed frame.
Information bit rate	8 kbps
Physical channel rate	32 kbps (sf=128)
Number of info bits per frame	80
CRC	16 bits

Coding	Convolutional coding Constraint length 9, rate 1/3, 8 tail bits
Rate matching	Repetition: 8 bits
Interleaving	10 ms
Pilot/TPC/TFCI bits per slot	6/2/2 for uplink 8/2/0 for downlink
Number of reception antennas	1 (i e. no antenna diversity)
DPCCH/DPDCH power	-3 dB for uplink 0 dB for downlink (For the Panasonic proposal, it becomes 2 dB during 16 slots after each transmission gap)
Inter-users interference	Modeled as AWGN noise. It is assumed constant and known in the simulations.

Table 1: Simulation parameters