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Agenda Item:
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Title: A method to classify the interleaved symbols of 1st MIL interleaver using some property
Document for: Discussion

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1. Introduction

In this document, we propose a novel method to apply the same rate matching algorithm used for down-link to up-link classifying output symbols of the 1st MIL interleaver in up-link. Recently, Siemens, LGIC, and Fujitsu have proposed rate matching algorithms with different algorithms for convolutional coding and turbo coding, respectively[1]-[5]. Also, Siemens and Nortel have investigated rate matching algorithms for both down-link and up-link, respectively [6]-[7]. However, the different characteristics of convolutional codes and turbo codes make it difficult to find an optimal solution for all cases[8]. The rate matching algorithm can be simply designed for the down-link, since rate matching procedure operates before 1st MIL interleaver. But in the up-link, rate matching procedure occurs after 1st MIL interleaver and must be operated on the 1st MIL interleaved sequence. Initially, it seemed almost impossible to find an optimal algorithm, which satisfies all constraints without modifying the 1st MIL or output pattern for turbo encoder. However, this contribution will show that the 1st MIL interleaved sequence can be easily classified into the three flows containing systematic information, parity symbols part 1, and parity symbols part 2. The key idea is that simple de-multiplexing after the 1st MIL interleaver can separate code symbols into three flows, systematic information, parity 1, and parity 2. This is done due to the good property of MIL 1st interleaver for transmission time interval of 10, 20, 40, 80msec.

In this contribution, we show that this property can be used for a rate matching algorithm in the up-link and promises a unified rate matching scheme for both convolutional codes and turbo codes for up/down links.

2. 1st MIL algorithm description

The 1st MIL interleaving of channel interleaving consists of two stage operations. In first stage, the input sequence is written into rectangular matrix row by row. The second stage is inter-column permutation. The two-stage operations are described as follows, the input block length is assumed to be K_1.

First Stage:

(1) Select a column number C_1 from Table 1.
(2) Determine a row number R_1 by finding minimum integer R_1 such that,

$$K_1 <= R_1 \times C_1.$$

(3) The input sequence of the 1st interleaving is written into the $R_1 \times C_1$ rectangular matrix row by row.

Second Stage:

(1) Perform the inter-column permutation based on the pattern $\{P_1(j)\}$ (j=0,1, ..., C-1) that is shown in, where $P_1(j)$ is the original column position of the j-th permuted column.

(2) The output of the 1st interleaving is the sequence read out column by column from the inter-column permuted $R_1 \times C_1$ matrix and the output is pruned by deleting the non-existence bits in the input sequence, where the deleting bits number I_1 is defined as:

$$I_1 = R_1 \times C_1 - K_1.$$

Table 1 1st MIL interleaving algorithm for interleaving span

Interleaving span	Column number C_1	Inter-column permutation patterns
10 ms	1	{0}
20 ms	2	{0,1}
40 ms	4	{0,2,1,3}
80 ms	8	{0,4,2,6,1,5,3,7}

3. Output symbol patterns of 1st MIL

Figure 1 illustrates an input symbol pattern for 1st MIL interleaver. All symbols are written in the interleaver memory sequentially as shown in Figure 1. In Figure 1 to 5, numbers are input symbol's order. For simplicity of description, we use the following notations for systematic information symbols, parity bits part 1, and parity bits part 2, respectively.

- Systematic information symbol ***(s)*** :

- Parity bits part 1 ***(p1)*** :

- Parity bits part 2 ***(p2)*** :

Figure 2 illustrates the 1st MIL interleaved symbol pattern for 20msec interleaving span. It is shown that the 1st MIL interleaved symbols are classified into the three flows containing systematic information, parity bits part 1, and parity bits part 2. So, the 1st MIL interleaved symbols are classified into the three flows using de-multiplexing with period of 3.

Figure 3 illustrates the 1st MIL interleaved symbol pattern for 40msec interleaving span. It is also shown that the 1st MIL interleaved symbols are classified into the three flows containing systematic information, parity bits part 2, and parity bits part 1. So, the 1st MIL interleaved symbols are classified into the three flows using de-multiplexing with period of 3.

Figure 4 illustrates the 1st MIL interleaved symbol pattern for 80msec interleaving span. It is also shown that the 1st MIL interleaved symbols are classified into the three flows containing systematic information, parity bits part 1, and parity bits part 2. So, the 1st MIL interleaved

symbols are classified into the three flows using de-multiplexing with period of 3.

Figure 5 illustrates the rate matching scheme using this good property of the 1st MIL interleaver. De-multiplexer classifies the 1st MIL interleaved symbols. So, the same rate matching algorithm used for down-link can be used for up-link without additional algorithm or algorithm modification.

4. Conclusion

In this contribution, we proposed a novel method to classify output symbols of the 1st MIL interleaver in the up-link. It was shown that the 1st MIL interleaved sequence can be easily classified into the three flows containing systematic information, parity bits part 1, and parity bits part 2. Thus, the same rate matching algorithm used for down-link can be used for up-link with only simple de-multiplexing with period of 3.

5. References

[1] "Comparison of downlink puncturing algorithms", LGIC, TSGR1#5(99)654(1999-06).
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[8] 3GPP TSG RAN WG1 Multiplexing and channel coding (FDD) TS 25.212 v2.0.0 (1999-06)
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1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72
73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88
89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104
105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120
121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136
137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152
153	154	155	156	157	158	159	160

Fig. 1. Input symbol pattern for 1st MIL interleaver (N=160, R=1/3).

1	3	5	7	9	11	13	15
17	19	21	23	25	27	29	31
33	35	37	39	41	43	45	47
49	51	53	55	57	59	61	63
65	67	69	71	73	75	77	79
81	83	85	87	89	91	93	95
97	99	101	103	105	107	109	111
113	115	117	119	121	123	125	127
129	131	133	135	137	139	141	143
145	147	149	151	153	155	157	159
2	4	6	8	10	12	14	16
18	20	22	24	26	28	30	32
34	36	38	40	42	44	46	48
50	52	54	56	58	60	62	64
66	68	70	72	74	76	78	80
82	84	86	88	90	92	94	96
98	100	102	104	106	108	110	112
114	116	118	120	122	124	126	128
130	132	134	136	138	140	142	144
146	148	150	152	154	156	158	160

Fig. 2. Output symbol pattern for 1st MIL interleaver.(N=160, R=1/3, **20msec** interleaving span).

1	5	9	13	17	21	25	29
33	37	41	45	49	53	57	61
65	69	73	77	81	85	89	93
97	101	105	109	113	117	121	125
129	133	137	141	145	149	153	157
3	7	11	15	19	23	27	31
35	39	43	47	51	55	59	63
67	71	75	79	83	87	91	95
99	103	107	111	115	119	123	127
131	135	139	143	147	151	155	159
2	6	10	14	18	22	26	30
34	38	42	46	50	54	58	62
66	70	74	78	82	86	90	94
98	102	106	110	114	118	122	126
130	134	138	142	146	150	154	158
4	8	12	16	20	24	28	32
36	40	44	48	52	56	60	64
68	72	76	80	84	88	92	96
100	104	108	112	116	120	124	128
132	136	140	144	148	152	156	160

Fig. 3. Output symbol pattern for 1st MIL interleaver. (N=160, R=1/3, **40msec** interleaving span).

1	9	17	25	33	41	49	57
65	73	81	89	97	105	113	121
129	137	145	153	5	13	21	29
37	45	53	61	69	77	85	93
101	109	117	125	133	141	149	157
3	11	19	27	35	43	51	59
67	75	83	91	99	107	115	123
131	139	147	155	7	15	23	31
39	47	55	63	71	79	87	95
103	111	119	127	135	143	151	159
2	10	18	26	34	42	50	58
66	74	82	90	98	106	114	122
130	138	146	154	6	14	22	30
38	46	54	62	70	78	86	94
102	110	118	126	134	142	150	158
4	12	20	28	36	44	52	60
68	76	84	92	100	108	116	124
132	140	148	156	8	16	24	32
40	48	56	64	72	80	88	96
104	112	120	128	136	144	152	160

Fig. 4. Output symbol pattern for 1st MIL interleaver. (N=160, R=1/3, **80msec** interleaving span).

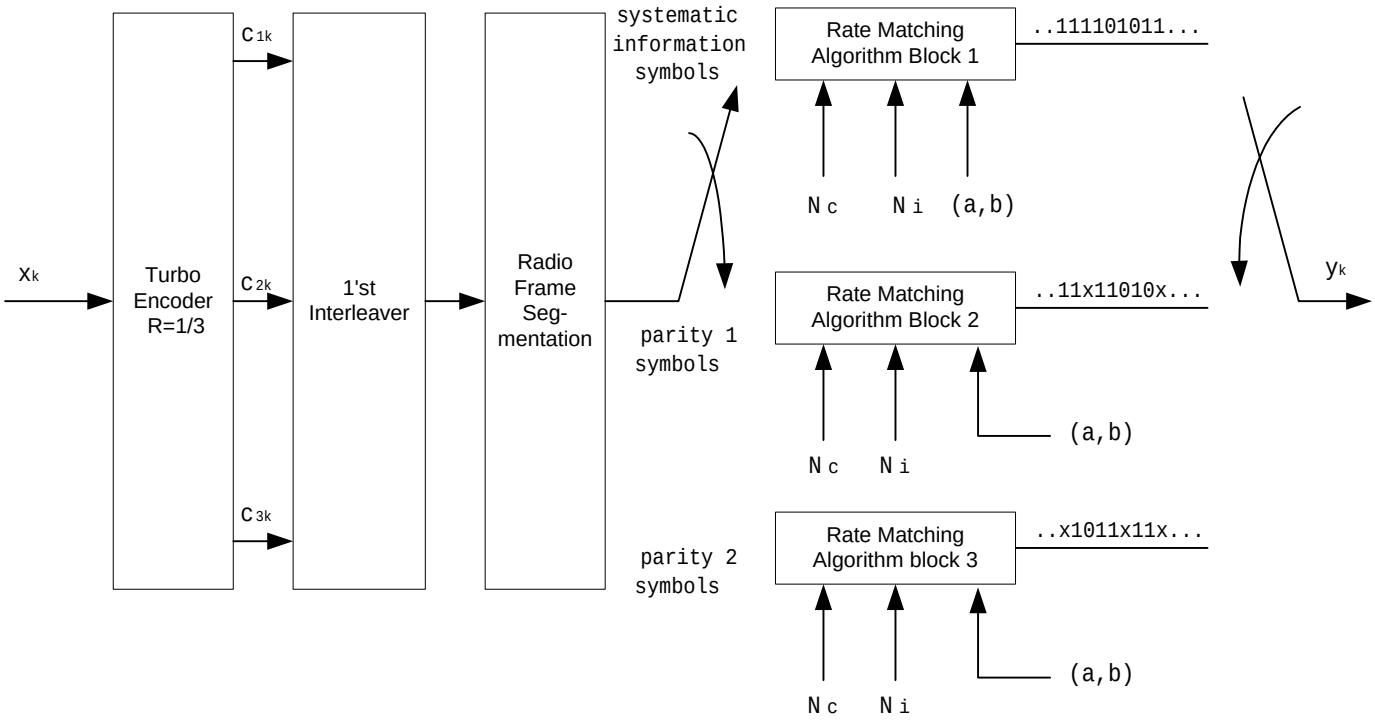

Fig. 5. A conceptual block diagram of the proposed rate matching scheme for both convoultional codes and turbo codes (Up-link) where x represents punctured bit.