TSG-RAN Working Group 1 meeting #5 Cheju, Korea June 1-4, 1999

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Agenda item:	Ad Hoc 4, item 7
Source:	Ericsson
Title:	Channel Interleaver Evaluation
Document for:	For information

1 Abstract

There are currently two proposals for channel interleaver. Final selection of channel interleaver, based on simulation results, should be done at WG1 meeting number 5. Simulation cases have been agreed upon in Ad Hoc 4. Ericsson has simulated some of these test cases and the results are presented in this document. Ericsson's simulation results do not show any significant differences in performance for the two proposals.

2 Simulation cases

Ericsson has simulated the test cases in the table below. Note that format 11 and 12 have been modified in Ericsson's simulations. The difference compared to the agreed parameters is that tail bits have been added for each frame. This would correspond to the case when 8 transport blocks is received in each transmission time interval. The interleaving is still carried out over 8 frames. The only reason for this change of parameters was that no modifications were then needed in our simulation chain. It is believed that this simulation case is at least as interesting as the original one, and it is therefore presented although it can not be directly compared with other companies results.

Format #	Input data	Tail for Conv.	Coded data	Puncturing		Punctured data		Dummy	DPDCH
	bit/TrBlk	bit/TrBlk	bit/TrBlk	bit/frame	%	bit/frame	%	bit/frame	bit/frame
1	206	8	642	2	0,31	640	100,0	0	640
2	258	8	798	158	19,80	640	100,0	0	640

Format #	Input data	Tail for Conv.	Coded data	Puncturing	9	Punctured dat	a	Dummy	DPDCH
	bit/frame	bit/frame	bit/frame	bit/frame	%	bit/frame	%	bit/frame	bit/frame
11	846	8	2562	2	0,08	2560	100,0	0	256
12	1058	8	3198	638	19,95	2560	100,0	0	256

Results



