TSG-RAN Working Group1 meeting #2
Yokohama 22-25, February 1999

TSGR1#2(99)097

Agenda Item: **4**

Source: **NTT DoCoMo**

Title: **A Study on Merging the Turbo-interleaver Candidates**

Document for: **Discussion**

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1. Introduction

This document introduces a merger of schemes in the turbo-internal interleaver candidates, i.e., GF [1], one-dimensional AL [2], two-dimensional AL [3] and MIL interleaver [4]. The target of the merger is selection of excellent schemes from the candidate interleavers and combination of them in order to achieve high performance with reasonable implementation complexity. In the following section of the document, the merger interleaver scheme is described and the performance is evaluated in terms of BER and FER. Note that the merger is not the final version, and it is now under development. So suggestions and comments are welcome.

2. Proposed Turbo-interleaver

Fig. 1 depicted the block diagram of the merger interleaver assuming the length of 5128 bits. The interleaver consists of three stages. In the first stage, the input sequence of the interleaver is written into the rectangular buffer row by row where the number of the rows is 8 and the number of bits in a row is 641 (= 5128 bit / 8 bit). The number of bits in a frame should be a prime number. In the second stage, both a mapping based on Logarithm function of Galois-Field and a permutaion based on complete residual system are used to permute each row. The mapping based on Logarithm function of GF is already used in GF-interleaver. The permutation based on complete residual system is already used in AL-interleaver. So, it can be said that the schemes included in GF and AL interleavres are merged in the second stage of the merger interleaver. Furthermore, in the third stage, the permutations of inter-rows are the same as MIL. Therefore, the interleaver can be stated to be a merger of GF, AL, and MIL interleaver.

3. Performance of the proposed interleaver

Figs. 3 (a), (b) and (c) show the BER and FER curves of the proposed interleavers assuming AWGN channel. Interleaver bit length of Fig. 3 (a), (b) and (c) are 328, 664, and 5128, respectively. Employing the combination use of bit-repetition and puncturing schemes, these interleavers can be adoptable to the input sequence of 320, 640 and 5120 bits.

References

[1] “Description of the GF Interleaver for Turbo codes”, Hughes Network Systems, Tdoc SMG2 UMTS L1 765/98
[2] “Algebraic interleavers for turbo codes”, CANON CRF, Tdoc SMG2 UMTS L1 571/98
[3] “Low complexity algebraic interleaver for UTRA turbo codes”, Nortel Nteworks, Tdoc SMG2 UMTS L1 051/99
[4] “Description of Multi-stage InterLeaver (MIL) for 8-state Turbo codes”, NTT DoCoMo, Tdoc SMG2 UMTS L1 027/99

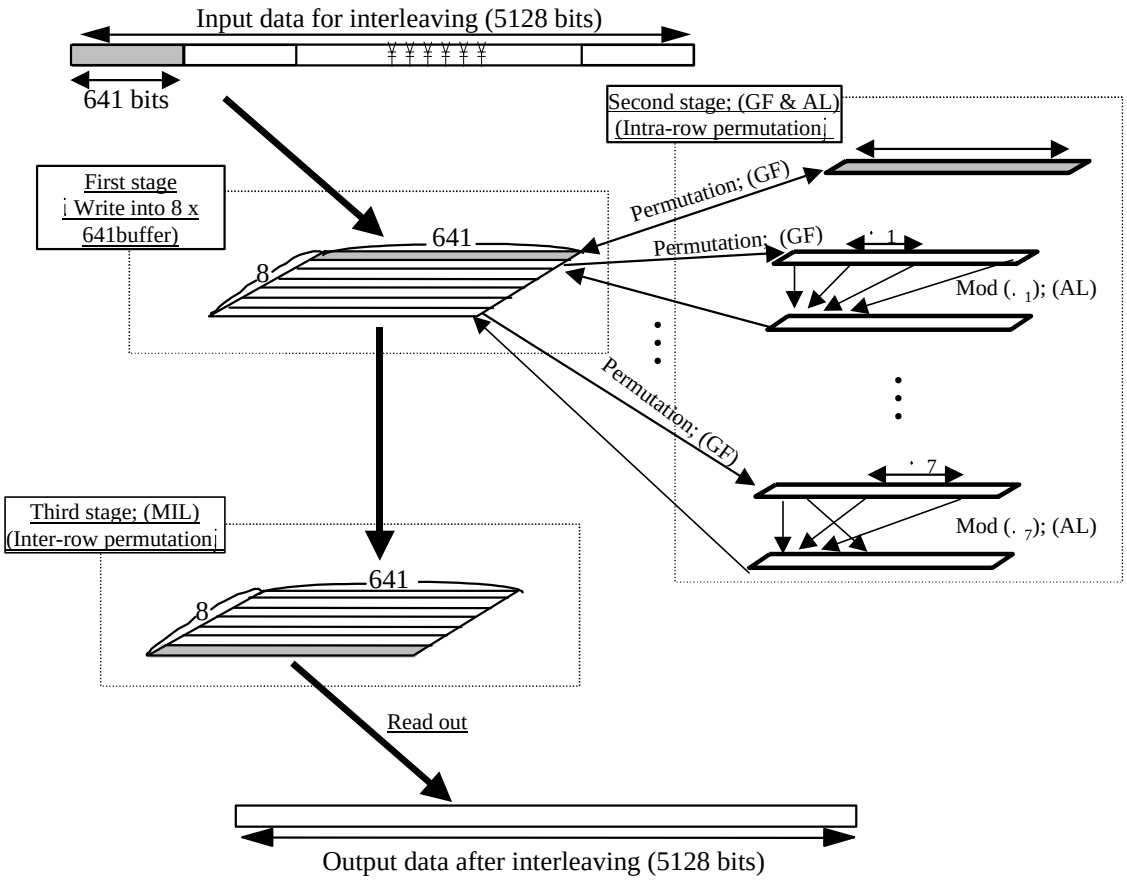


Fig. 1 Block diagram of the merger interleaver.

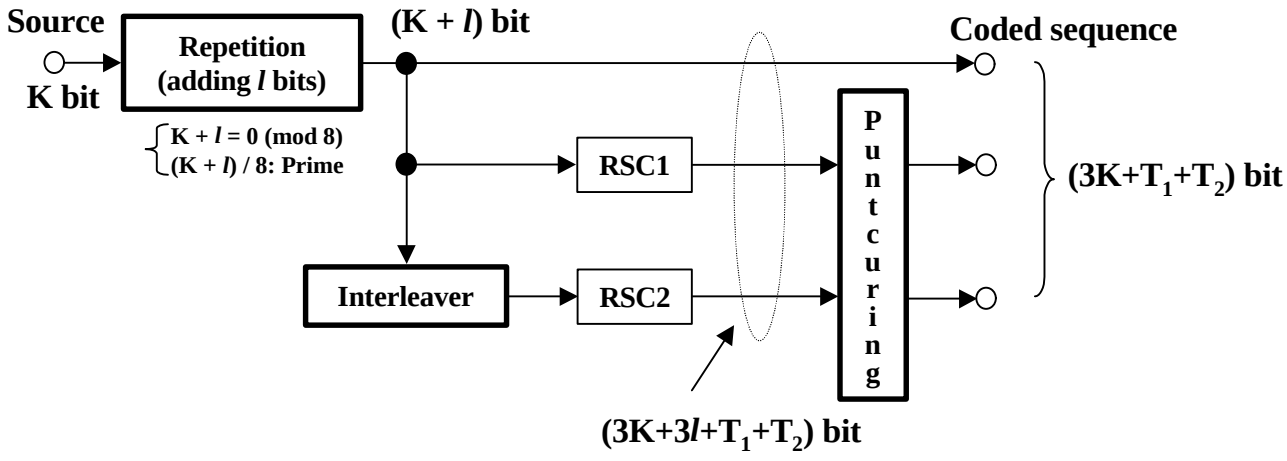
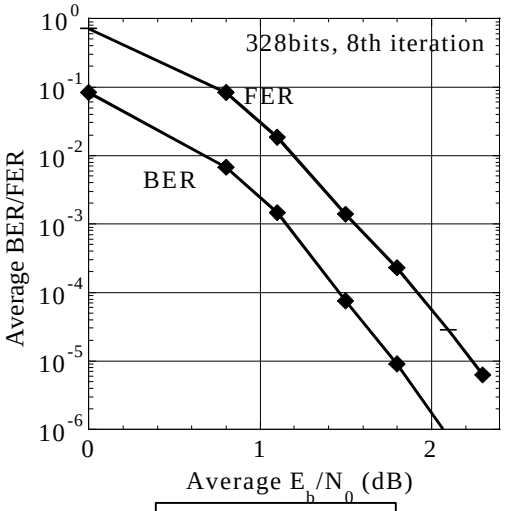
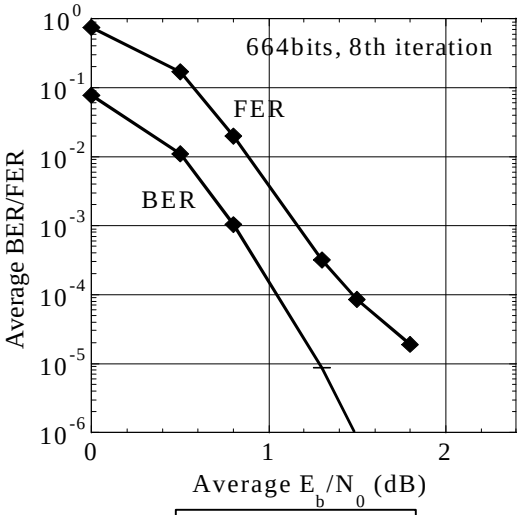


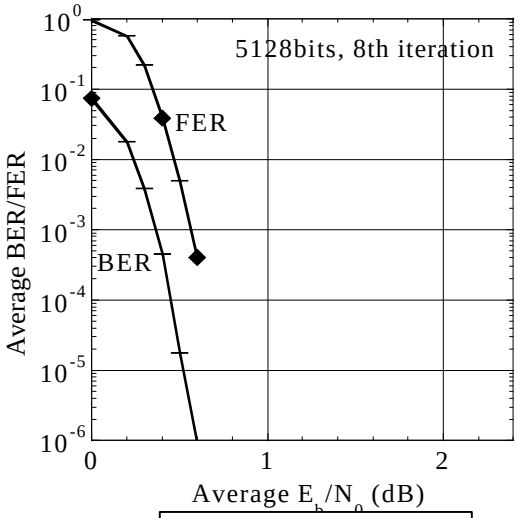
Fig. 2 Block diagram of turbo encoder.



(a) 328-bit frame



(b) 664-bit frame



(c) 5128-bit frame

Fig. 3 The BER/FER performance comparison of the merger interleaver under AWGN.