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INTRODUCTION

In this document, we present a thorough comparison of three concatenated coding schemes: two parallel concatenated convolutional codes (PCCC in the following, also known as "turbo codes"), and one serially concatenated convolutional codes [1] (SCCC, in the following). Three information block sizes are considered, i.e., 320, 640 and 5,120 bits, in the whole document, whereas in parts of it also the block sizes of 80 and 160 are given some attention. First, we analyse the code performance using the average interleaver known as uniform interleaver over additive white Gaussian noise (AWGN) channel, devoting a particular attention to the interleaving gain and error floor phenomena. Then, we compare the three codes in terms of achievable free distance, and use a fast algorithm to compute the code actual free distances with some specific interleavers. Successively, we simulate the three schemes over the AWGN channel. Finally, we show simulation results for the 8-state PCCC and the 4-state SCCC schemes over the correlated fading channel at mobile speed of 3 and 30 km/h.

The codes to be compared

In all numerical results, we will consider three rate 1/3 candidate codes, one SCCC and two PCCCs, namely:

• The SCCC is a rate 1/3 code, whose structure is shown in Figure 1. It is formed by an outer code with rate 2/3 obtained by puncturing a systematic, recursive, rate ½ convolutional code with generating matrix $G^{(o)}(Z) = (1, (1+Z^2)/(1+Z+Z^2))$ (the rate 2/3 is obtained by puncturing every other parity-check bit), and an inner code consisting of a rate ½ systematic recursive convolutional code with the same previous generating matrix, i.e $G^{(i)}(Z) = (1, (1+Z^2)/(1+Z+Z^2))$



Figure 1. Structure of the rate 1/3 SCCC encoder.

• The first PCCC is a rate 1/3 code, whose structure is shown in Figure 2. It is formed by two 4-state, systematic, recursive convolutional codes concatenated in parallel through an interleaver. The two constituent encoders have generating matrix $G(Z) = (1, (1 + Z^2)/(1 + Z + Z^2))$.



Figure 2: Structure of the rate 1/2 4 -state PCCC encoder.

• The second PCCC is a rate 1/3 code, whose structure is shown in Figure 3. It is formed by two 8-state, systematic, recursive convolutional codes concatenated in parallel through an interleaver. The two constituent encoders have generating matrix

$$G(Z) = (1, (1 + Z + Z^3))/(1 + Z^2 + Z^3)).$$



Figure 3: Structure of the rate ¹/₂ 8 *–state PCCC encoder.*

Interleaver gain

We have proved in [1] for serial concatenation (but the same result holds true for parallel concatenation) that for large interleaver size the frame error probability for maximum-likelihood decoding can be upper bounded as:

$$P_f(e) \approx \sum_h C_h N^{a(h)} \operatorname{erfc}\left(\sqrt{\frac{hR_c E_b}{N_0}}\right)$$

Where the coefficient C_h does not depend on N, h is the code word weight, and N is the information block s

A similar expression holds true for the bit error probability, where the exponent $\alpha(h)$ of *N* is equal to the previous value decreased by one.

For each weight *h*, the interleaver gain is then strictly related to the exponent $\alpha(h)$. Negative exponents mean that for increasing interleaver sizes the contribution of that weight to the error probability will decrease.

In Figure 4 we report the exponent $\alpha(h)$ as a function of the weight *h* for the three codes. It is clear that both PCCCs have some values of *h* for which there is no interleaving gain (α =0), whereas for the SCCC all *h* present interleaving gain (α <0). Thus, for the average PCCC codes, the frame error probability will not decrease with increasing interleaver sizes, whereas for SCCC it will decrease as *N*⁻¹. On the other hand, the bit error probability will decrease as *N*⁻¹ for PCCCs, and as *N*⁻² for the SCCC.



Figure 4: Exponent of interleaver size versus codeword weight for the three considered codes. To make things clearer, we also report the main numerical values in Table 1.

Codeword weight	4 PCCC	8 PCCC	4 SCCC
5			-1
6			-2
7	-1		-1
8	-1	-2	-2
9	-1	-1	-1
10	0	-1	-2
11	-1	-1	-1
12	0	-1	-1
13	-1	-1	-1
14	0	0	-1
15	-1	-1	-1
16	0	-1	-1
17	-1	-1	-1
18	0	0	-1
19	-1	-1	-1
20	0	-1	-1
21	-1	-1	-1
22	0	0	-1
23	-1	-1	-1
24	0	-1	-1

Table 1: Exponent of interleaver size versus codeword weight

Results on achievable free distance

The error floor of concatenated codes with interleavers is related to their relatively low free distance. Previously, we have seen, using the concept of uniform interleaver, that the behaviour of SCCCs is better than that of PCCCs because of the larger interleaving gain. Here, we will add some considerations dealing specifically with the achievable free distance of SCCCs and PCCCs with specific, actual interleavers.

In Figure 5, Figure 6 and Figure 7 we plot the cumulative average weight multiplicity for the three codes using uniform interleavers of 5 sizes versus the code word Hamming weight. To be more specific in Figure 5, referring to the case of 4-state-based SCCC, we read for an abscissa of 15 and N=160, a value equal to 1 for the ordinate. This means that the sum of all the multiplicities of error events with weight less than or equal to 15 is 1, for the average code employing the uniform interleaver. It can be seen that the curves increase with the weight *h*, with different slopes depending on the block size. This reflects the difficulty of finding an actual interleaver being able to destroy all error events with large weights, and sets a limit to the achievable free distance.



Figure 5: Cumulative average coefficient of 4 state SCCC versus codeword weight

Distance Profile 4-state PCCC



Figure 6: Cumulative average coefficient of 4 state PCCC versus codeword weight.



Figure 7: Cumulative average coefficient of 8 state PCCC versus codeword weight.

Our experience tells us that, typically, a randomly chosen interleaver will yield a free distance of the code around the abscissa corresponding to the crossing of the curves with the ordinate equal to 1, whereas a careful optimization of the interleaver can permit an increase of the free distance up to the intersection of the curves with the ordinate equal to 10, and slightly beyond. Relying on this experience, we thus say that, as an example for N=320, we can hope to reach a

free distance around 13 for the 4-state-based PCCC, to 18 for the 8-state-based PCCC, and to 28 for the 4-state-based SCCC.

In Table 2, we report the computed free distances for the three codes using several interleavers, some already available on the reflector, and some optimised by ourselves (see the companion document [2]). It can be seen that the agreement with the previous guess based on Figs. 5-7 is amazing. In particular, the values in the table show that, for a given interleaver size, SCCC significantly outperforms both PCCCs. As an example, for N=320, SCCC with an optimized HNS interleaver yields a free distance larger than 29 (and less than 36), whereas the 8-state-based PCCC, with the MIL interleaver (we did not find HNS interleavers of this size on the reflector), yields a free distance of 17.

		S-random	HNS	MIL	Nortel	
8 0	4 SCCC			18/1/6	22/1/8	
1 6 0	4 SCCC	22/1/2	-	23/1/6	24/2/8	
3 2	4 PCCC	16/4/8		14/1/1	18/1/2	
	8 PCCC			17/1/1	17/1/3	
	4 SCCC	29 < <i>d</i> <=31	29< <i>d</i> <= 32	25/1/5	29/1	
6 4	4 PCCC	18/5/10	12/1/2	16/1/2	20/1/2	
	8 PCCC		18/1/2	14/3/6		
	4 SCCC	29 < <i>d</i> <= 36	29< <i>d</i> <= 36	29/2/18	25/10	
5 1	4 PCCC			22/1/2	24/692/2768	
	8 PCCC			>24		
	4 SCCC			<36/1/5 (>29)		

Table 2: Free distances of the three codes with various interleaver. First number is the free distance, the second is the number of nearest neighbours, and the third is the cumulative weight of information sequence generating the free distance codewords

Returning back to the curves of Figs. 5-7, we notice that the curves for PCCCs at the ordinate equal to 10 are tightly grouped together when varying the interleaver size, meaning that the expected increase in free distance is quite limited when acting on the interleaver size. On the other hand, the curves for the SCCC intersect the ordinate 10 at very different Hamming weight, significantly increasing with the interleaver size. This means that it is much easier to obtain a larger free distance for SCCC by acting on the interleaver size.

An important consequence of this different behaviour is that, if we want to increase the rate by puncturing, PCCCs may reach insufficient free distances that push the error

floor to unacceptably high values of the error probabilities.

If, as for standard convolutional codes, the free distance were the main criterion for the choice, this would point to the SCCC as the best code without any doubt. This also means that SCCC is certainly better than PCCCs in terms of error floor, so that, no matter what the interleaver size is, sooner or later the curve for the SCCC will cross and improve over those of the PCCCs.

The simulated performance over AWGN

In this section, we consider the performance of the three codes with an actual interleaver and the suboptimum iterative decoding algorithm based on sliding-window, log-map APP algorithms quantized to 8 bits.

The interleavers have been chosen based on their availability on the reflector. For N-320 and 5120, they will be MIL interleaver for all the three codes, for N=640 we will use the MIL interleaver for SCCC, the MIL and HNS interleavers for the 8-state-based PCCC, and the ????? for the 4-state-based PCCC. (a discussion on the performance of different interleavers is presented in a companion document [2]). Since for SCCCs the interleaver operates on the outer encoded bits, which include three bits for terminating the outer encoder trellis, its size N_I is chosen according to the following table:

Information block size (N)	Interleaver size (N_I)	
320	483	
640	963	
5120	7683	

In Figure 8, Figure 9 and Figure 10 we show the simulated frame and bit error probabilities for the three codes and the three interleaver lengths for transmission over an AWGN channel. Since we are particularly interested in investigating the phenomenon known as *error floor*, we have performed 100 iterations of the decoding algorithm.



Comparison between concatenated schemes (Information block size 320) 100 iterations, MIL interleavers

Figure 8: Bit and frame error probabilities over the AWGN channel for N=320, three codes and MIL interleaver with 100 iterations.



Comparison between concatenated schemes (Information block size 640) 100 iterations

Figure 9: Bit and frame error probabilities over the AWGN channel for N=640, three codes and various interleavers with 100 iterations.



Comparison between concatenated schemes (Information block size 5120) 100 iterations, MIL interleavers

Figure 10: Bit and frame error probabilities over the AWGN channel for N=5120, three codes and MIL interleaver with 100 iterations.

Figure 8, referring to N=320, shows that both PCCCs exhibit an error floor. The 4-state-based PCCC presents the FER error floor around 10^{-4} , and a BER error floor at 10^{-6} ; the 8-state-based PCCC shows the error floors at 10^{-5} (FER) and 10^{-7} (BER). The 4-state-based PCCC is very weak and critical around the targeted FER and BER, as it looses around 0.5 dB at BER= 10^{-6} with respect to both SCCC and 8-state-based PCCC. In terms of FER, the performance are quite bad, owing to the small free distance.

Figure 9 refers to N=640. If we compare first the performance of the 8-state-based PCCCs using the HNS and MIL interleavers, we notice the weakness of the latter, exhibiting an early error floor. This is due to the fact that MIL interleaver in this case presents a significantly smaller free distance with respect to HNS (14 versus 18, see previous table). In terms of error floor, 4-state PCCC shows it around BER=10⁻⁶ and FER=10⁻⁴. SCCC does not show error floor for bit or frame error probabilities. The yields an advantage of about 1.0 dB over the 8-state-based PCCC at FER=10⁻⁵, whereas the BER curves would cross each other slightly below 10⁻⁶.

Finally, Figure 10 reports the result for N=5120. Here, the error floors of the 4-state PCCC are evident at BER=10⁻⁶ and FER=10⁻³. 8-state PCCC starts showing the error floor for the FER around 10⁻⁴, whereas SCCC does not. At BER=10⁻⁶ 8-state PCCC yields an advantage of less than 0.3 dB over SCCC, whereas only SCCC seems to be able to reach a FER=10⁻⁵.

The simulated performance over the correlated fading channel

The simulations have been performed in the following conditions:

• The channel is the Phase-2 channel with the receiver implementing the receiver scheme proposed by HNS.

- For each E_b/N₀, we have simulated up to 1.5 million of frames (for *N*=320 and 640), and 150,000 frames for *N*=5,120, with a time-saving criterion that stopped the simulation when 100 frame errors had been counted.
- The interleavers are the ones kindly supplied by NTT-DoCoMo for SCCC, and the GF interleavers of HNS for PCCC, and correspond to the three information block sizes of *N*=320, 640, 5120.
- Only two codes have been simulated, namely the SCCC and the 8-state-based PCCC, since the 4-state-based PCCC had been shown to present an error floor that makes it significantly weaker than the other two at low frame and bit error probabilities.
- The iterative decoder is based on a sliding-window log-MAP algorithm, quantized on 8 bits, and performs up to 10 iterations [3].

The phase-2 channel at 3 km/h

INFORMATION BLOCK SIZE N=320

In Figure 11 and Figure 12 we report we report the simulation results referring to SCCC with N=320, in terms of frame and bit error probabilities, for a number of iterations ranging from 1 to 10. In the case of the frame error probability, we also report, for each simulated signal-to-noise ratio, the **average number of iterations** that should have been performed in the case of a stopping rule based on the use of an ideal error detecting code (see also the previous document [4] describing the use of a cyclic code as an error detecting code).

SCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 320



Figure 11: Frame error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=320, 1 to 10 iterations, v=3km/h.



Figure 12: Bit error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=320, 1 to 10 iterations, v=3km/h.

In Figure 13 and Figure 14 we report the analogous results for the PCCC.



Figure 13: Frame error probability versus bit SNR for the 8-state PCCC with MIL interleaver, N=320, 1 to 10 iterations, v=3km/h.



PCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 320

Figure 14: Bit error probability versus bit SNR for the 8-state PCCC with MIL interleaver, N=320, 1 to 10 iterations, v=3km/h.

INFORMATION BLOCK SIZE N=640

In Figure 15 and Figure 16 we report we report the simulation results referring to SCCC with N=640, in terms of frame and bit error probabilities, for a number of iterations ranging from 1 to 10.



SCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 640

Figure 15: Frame error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=640, 1 to 10 iterations, v=3km/h.



SCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2)

Figure 16 Bit error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=640, 1 to 10 iterations, v=3km/h.

In Figure 17 and Figure 18 we report the analogous results for the PCCC.



PCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 640

Figure 17: Frame error probability versus bit SNR for the 8-state PCCC with HNS interleaver, N=640, 1 to 10 iterations, v=3km/h.



PCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 640

Figure 18: Bit error probability versus bit SNR for the 8-state PCCC with HNS interleaver, N=640, 1 to 10 iterations, v=3km/h.

INFORMATION BLOCK SIZE N=5,120

In Figure 19 and Figure 20 we report we report the simulation results referring to SCCC with N=5,120, in terms of frame and bit error probabilities, for a number of iterations ranging from 1 to 10.



Figure 19: Frame error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=5120, 1 to 10 iterations, v=3km/h.



SCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 5120

Figure 20: Bit error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=5120, 1 to 10 iterations, v=3km/h.

In Figure 21 and Figure 22 we report the analogous results for the PCCC.



Figure 21: Frame error probability versus bit SNR for the 8-state PCCC with MIL interleaver, N=5120, 1 to 10 iterations, v=3km/h.



PCCC Simulation results - Phase 2 channel v=3 km/h with HNS receiver (method 2) Information block size 5120

Figure 22: Bit error probability versus bit SNR for the 8-state PCCC with MIL interleaver, N=5120, 1 to 10 iterations, v=3km/h.

The phase-2 channel at 30 km/h

INFORMATION BLOCK SIZE N=320

In Figure 23 and Figure 24 we report we report the simulation results referring to SCCC with N=320, in terms of frame and bit error probabilities, for a number of iterations ranging from 1 to 10. In the case of the frame error probability, we also report, for each simulated signal-to-noise ratio, the **average number of iterations** that should have been performed in the case of a stopping rule based on the use of an ideal error detecting code (see also the previous document [4] describing the use of a cyclic code as an error detecting code).



Figure 23: Frame error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=320, 1 to 10 iterations, v=30 km/h.



SCCC Simulation results - Phase 2 channel v=30 km/h with HNS receiver (method 2)

Figure 24: Bit error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=320, 1 to 10 iterations, v=30 km/h.

In Figure 25 and Figure 26 we report the analogous results for the PCCC.



Figure 25: Frame error probability versus bit SNR for the 8-state PCCC with MIL interleaver, N=320, 1 to 10 iterations, v=30 km/h.





Figure 26: Bit error probability versus bit SNR for the 8-state PCCC with MIL interleaver, N=320, 1 to 10 iterations, v=30 km/h.

INFORMATION BLOCK SIZE N=640

In Figure 27 and Figure 28 we report we report the simulation results referring to SCCC with N=640, in terms of frame and bit error probabilities, for a number of iterations ranging from

1 to 10.



Figure 27: Frame error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=640, 1 to 10 iterations, v=30 km/h.



SCCC Simulation results - Phase 2 channel v=30 km/h with HNS receiver (method 2)

Figure 28: Bit error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=640, 1 to 10 iterations, v=30 km/h.



In Figure 29 and Figure 30 we report the analogous results for the PCCC.

PCCC Simulation results - Phase 2 channel v=30 km/h with HNS receiver (method 2) Information block size 640

Figure 29: Frame error probability versus bit SNR for the 8-state PCCC with HNS interleaver, N=640, 1 to 10 iterations, v=30 km/h.

PCCC Simulation results - Phase 2 channel v=30 km/h with HNS receiver (method 2) Information block size 640



Figure 30: Bit error probability versus bit SNR for the 8-state PCCC with HNS interleaver, N=640, 1 to 10 iterations, v=30 km/h.

INFORMATION BLOCK SIZE N=5,120

In Figure 31 and Figure 32 we report we report the simulation results referring to SCCC with



N=5,120, in terms of frame and bit error probabilities, for a number of iterations ranging from 1 to 10.

Figure 31: Frame error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=5120, 1 to 10 iterations, v=30 km/h.



SCCC Simulation results - Phase 2 channel v=30 km/h with HNS receiver (method 2) Information block size 5120

Figure 32: Bit error probability versus bit SNR for the 4-state SCCC with MIL interleaver, N=5120, 1 to 10 iterations, v=30 km/h.

In this case, we had no time to simulate the PCCC.

Comparison between SCCC and PCCC

In this section, we compare the performance of SCCC and PCCC by plotting together the curves pertaining to the 10-th iteration of the decoding algorithm in the same system conditions. For theses curves, we also plot, for each signal-to-noise ratio, the **confidence** *interval* obtained as explained in [5]. In short, its meaning is that, with a probability of 0.99, the estimated error probability will lie within the plotted interval. It is important to state that the analysis is rigorous for the frame error probability in case of independent frame errors, as it happens on AWGN or independent Rayleigh fading channels, and can be considered as an approximation for the bit error probability. For Phase 2 channel, especially at low mobile speed, the hypothesis of independent frame errors may be questionable.

The Phase 2 channel at 3 km/h

In Figure 33 we plot the bit and frame error probabilities for SCCC and PCCC in the case of N=320 and Phase-2 channel at 3 km/h.



Figure 33: Frame and Bit error probability comparison between 8-state PCCC and 4-state SCCC with N=320, 10 iterations, v=3km/h. MIL interleavers.

In Figure 34 we plot the bit and frame error probabilities for SCCC and PCCC in the case of N=640 and Phase-2 channel at 3 km/h.



Comparison PCCC-SCCC - v=3km/h Information block size 640

Figure 34: Frame and Bit error probability comparison between 8-state PCCC and 4-state SCCC with N=640, 10 iterations, v=3km/h. MIL (SCCC) and HNS (PCCC) interleavers.

In Figure 35 we plot the bit and frame error probabilities for SCCC and PCCC in the case of N=5120 and Phase-2 channel at 3 km/h.



Comparison 8-state PCCC vs 4-state SCCC - v=3 km/h Information block size 5120

Figure 35: Frame and Bit error probability comparison between 8-state PCCC and 4-state

The Phase 2 channel at 30 km/h

In Figure 36 we plot the bit and frame error probabilities for SCCC and PCCC in the case of N=320 and Phase-2 channel at 30 km/h.



Figure 36: Frame and Bit error probability comparison between 8-state PCCC and 4-state SCCC with N=320, 10 iterations, v=30km/h. MIL interleavers.

In Figure 37 we plot the bit and frame error probabilities for SCCC and PCCC in the case of N=640 and Phase-2 channel at 30 km/h.



Comparison PCCC-SCCC - v=30 km/h Information block size 640

Figure 37: Frame and Bit error probability comparison between 8-state PCCC and 4-state SCCC with N=640, 10 iterations, v=30km/h. MIL (SCCC) and HNS (PCCC) interleavers.

For N=5120 there are no comparisons for the lack of the PCCC simulation.

In the following table, we report the comparisons made at a bit error probability of 10⁻⁶ and a frame error probability of 10⁻⁵. For completeness, we also report the comparison obtained on an AWGN channel. The (*) refers to extrapolated results.

		AWGN				
	SCCC,	PCCC,	SCCC,	PCCC,	SCCC,	PCCC,
	N=320	N=320	N=640	N=640	N=5120	N=5120
BER, 10^{-6}	2.1 dB	1.9 dB	1.55 dB	1.32 dB	0.72 dB	0.45 dB
FER, 10 ⁻⁵	2.1 dB	> 3 dB (*)	1.55 dB	2.5 dB (*)	0.8 dB (*)	>1.5 dB (*)
		Phase 2,				
		3 km/n				
	SCCC,	PCCC,	SCCC,	PCCC,	SCCC,	PCCC,
	N=320	N=320	N=640	N=640	N=5120	N=5120
BER, 10^{-6}	5.17 dB	5. dB	3.9 dB	3.61 dB	2.9 dB	2.6 dB
FER, 10^{-5}	5.17 dB	>5.5 dB (*)	3.62 dB	> 4.0 dB (*)	3.0 dB (*)	2.9 dB (*)
		Phase 2,				
		30 km/h				
	SCCC,	PCCC,	SCCC,	PCCC,	SCCC,	PCCC,
	N=320	N=320	N=640	N=640	N=5120	N=5120
BER, 10^{-6}	6.19 dB	5.8 dB	4.95 dB	4.72 dB	3.18 dB	
FER, 10^{-5}	6.17 dB	6 dB (*)	5.02 dB	4.8 dB	3.22 dB (*)	

From the curves and table, we derive the following comments (see also the important observations in the following section):

- For an information block size of 320 bits, we distinguish between AWGN channel, 3 and 30 km/h:
 - Over the AWGN channel, PCCC is better than SCCC at a bit error probability of 10⁻⁶ by 0.2 dB, whereas, in terms of frame error probability of 10⁻⁵, SCCC outperforms PCCC by 1 dB.
 - At 3 km/h, PCCC outperforms SCCC by less than 0.2 dB in terms of bit error probability at 10⁻⁶, whereas in terms of frame error probability SCCC is better than PCCC (more than 0.3 dB at 10⁻⁵).
 - At 30 km/h, there is an advantage of PCCC over SCCC in terms of bit error probability (slightly less than 0.4 dB). Again, in terms of frame error probability SCCC yields a gain of more than 0.2 dB over PCCC.
- For an information block size of 640 bits, we distinguish again among the AWGN channel, and the two speeds of 3 and 30 km/h:
 - Over the AWGN channel, PCCC is better than SCCC at a bit error probability of 10⁻⁶ by less than 0.2 dB, whereas, in terms of frame error probability of 10⁻⁵, SCCC

outperforms PCCC by over 1.0 dB.

- At 3 km/h and a bit error probability of 10⁻⁶ PCCC yields a gain of slightly less than 0.3 dB over SCCC. In terms of frame error probability, SCCC shows a gain of about 0.4 dB over PCCC, at a frame error probability of 10⁻⁵.
- For the case of 30 km/h, PCCC outperforms SCCC by slightly more than 0.2 dB at a bit error probability of 10^{-6} , and a gain of less than 0.2 dB is present also at a frame error rate of 10^{-5} .
- For an information block size of 5120 bits, we distinguish again among the AWGN channel, and the two speeds of 3 and 30 km/h:
 - Over the AWGN channel, PCCC is better than SCCC at a bit error probability of 10⁻⁶ by less than 0.3 dB, whereas, in terms of frame error probability of 10⁻⁵, SCCC outperforms PCCC by over 0.7 dB.
 - At 3 km/h and a bit error probability of 10⁻⁶ PCCC yields a gain of 0.3 dB over SCCC. In terms of frame error probability, PCCC shows a gain of about 0.1 dB over SCCC, at a frame error probability of 10⁻⁵.
 - For the case of 30 km/h, we only have the results for SCCC, so that no comparison is possible.

Fundamental system observations

In this section, we make some methodological critical comments on the choice of bit versus frame error probability as a criterion to choose the coding scheme. Let us first point out the following facts:

- In all simulation results presented in this document (and also in companion documents of other companies), the ratio between frame and bit error probabilities is less than 200. This means that the **bit error probability conditioned on a frame error is higher than 10**³.
- In the SMG2 document entitled "Submission of Proposed Radio Transmission Technologies", the quality threshold is defined as BER=10⁻³ (speech) or BER=10⁻⁶ (LCD)." This means that we can consider as outage condition for the LCD system a bit error probability lower than 10⁻⁶. Based on the previous item, we can also say that the system outage probability coincides with the frame error probability (this for both speech and LCD services), so that the percentage of time in which the user has a sufficiently good quality is equal to: (1- FER)x100. As an example, a system reliability goal limiting the system outage time to less than 10 minutes per year results in a required frame error rate of 1.9x10⁻⁵.
- As a consequence of the previous items, we can affirm that **the average bit error probability has a very poor (if any) meaning in terms of system quality, since either it is zero (when the frame is correct), or it is above the quality threshold, when the frame is in error.** It is questionable whether applications can be found tolerating a large average bit error probability over large frames. When dealing with data packet transmission, the previous statement is even stronger.
- The **real indicator of the service quality is indeed the frame error probability**, and, moreover, we need a way to estimate the reliability of the frames (see the previous document [4]): when a frame error is detected, the system is in outage, and according to strategy, FEC or ARQ, the frame should be discarded or a retransmission should be asked for.

Conclusions

As conclusions, we state the following:

- Based on the results over the AWGN channel (also confirmed in previous ETSI documents), 4-state-based PCCC exhibits a sensible error floor for both bit and frame error probabilities that makes it much weaker than 4-state SCCC and 8-state-based PCCC. It should then be discarded from the candidate codes.
- SCCC, for all information block sizes, yields a significantly larger free distance than 4- and 8-state PCCCs. Moreover, PCCCs show error floor very near the error performance measures. When dealing with rate-compatible codes, or when increasing the code rate by puncturing, the free distance would increase to values rising the error floors to unacceptably high values.

- In all simulated cases, the behaviour of SCCC does not show error floors, and the curves of BER and FER decrease regularly in a parallel shape.
- For all considered channels and frame sizes, the advantage of 8-state-based PCCC over the 4-state-based SCCC is less than 0.3 dB at a bit error probability of 10⁻⁶.
- If, based on the observations of the previous section, we use the frame error rate as a measure of the quality of the coded scheme, the extensive results presented in this document show that the serial concatenation (SCCC) of two low complex, 4-state convolutional codes is almost uniformly better than the parallel concatenation (PCCC).
- The steeper slope of its curves makes SCCC more robust than PCCC to severe channel conditions and **suitable to the cases and applications in which frame error probabilities lower than 10**⁵ (or bit error probabilities lower than 10⁶) were needed.
- The companion document on implementation complexity comparison [6] shows that the 4-state SCCC is also less complex than the 8-state PCCC for all block sizes, and that its power consumption is lower.

Thus, we propose to use, at least for high data rate services (for low data rate see the companion document [7]), the rate 1/3 SCCC scheme based on a rate 2/3 outer, rate $\frac{1}{2}$ inner encoders described in this document.

References

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