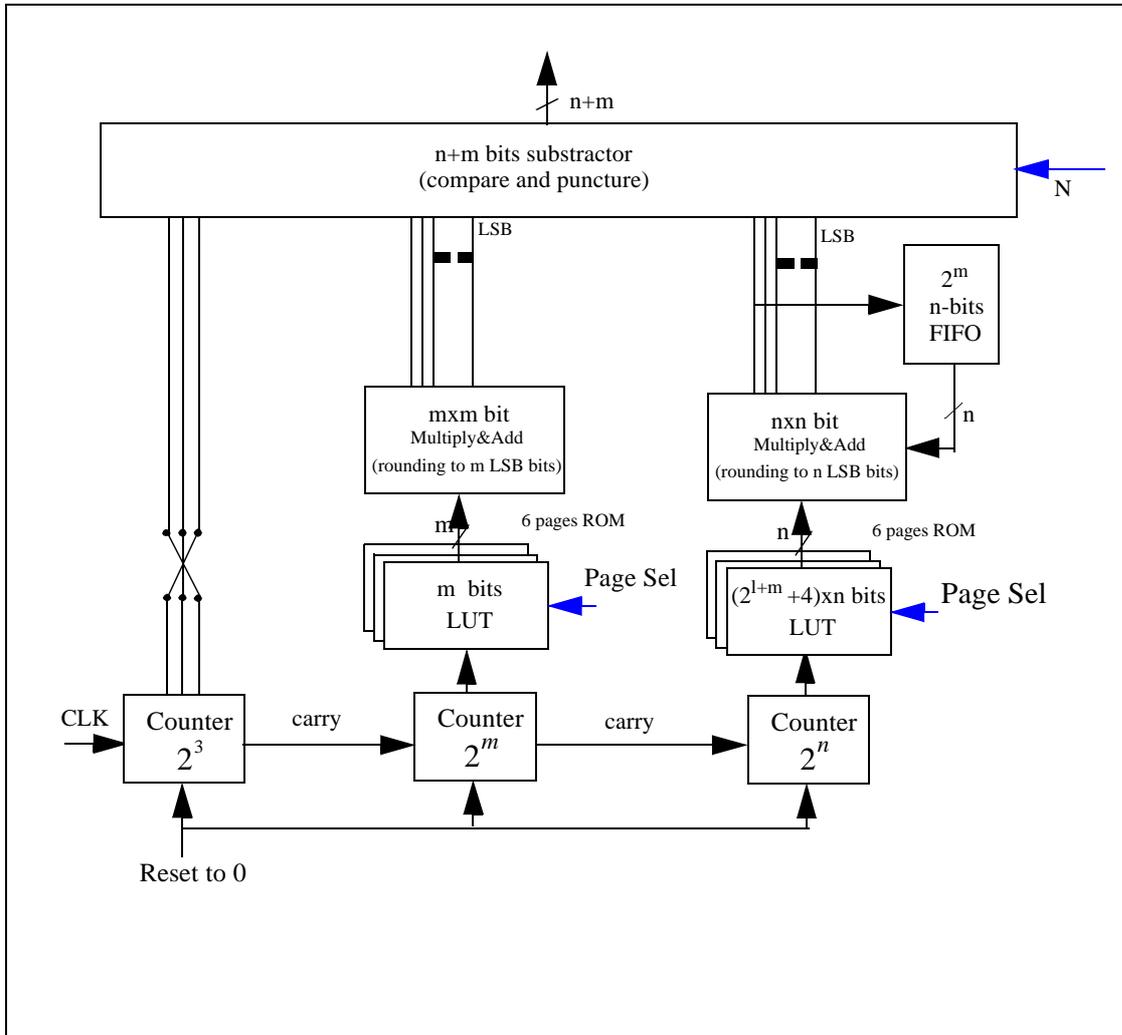

2.2.3 Implementation

The hardware implementation of the multi-stage Turbo interleaver is shown in Figure 2.

FIGURE 2. Implementing of Multi-Stage Turbo Interleaver



Summary and Conclusions:

In this contribution, we analysis the key elements and commonality for three turbo interleavers and furthermore a merging proposal for one-stage and multi-stage turbo interleaver are discussed.

2.2.2 Column Permuting Algorithm

The column permuting rule is as follows:

Select $\{m,n\}=\{1,32\} \{4,16\} \{8,16\} \{8,32\} \{8,64\} \{16,64\}$

For $i=1$ to 2^n

For $l=1$ to 2^m

$$r(l) = [\alpha_k l] \bmod 2^m$$

For $j=1$ to 8

$$j_r = \text{Bit_Rev}(j)$$

$$k = [j_r] \bmod 4$$

$$c_{j_r}(i) = [\alpha_k i + \beta_{j_r}] \bmod 2^n$$

$$I[(i-1)2^{m+n} + (l-1)2^m + j] = j_r 2^{n+m} + r(l)2^n + c_{j_r}(i)$$

end

end

end

2.2 Combined Multi-Stage Turbo Interleaver

2.2.1 Interleaver Framework and Parameters

- Concatenation of 2-D interleaving
- Bit-Reversal permuting the outer rows
- Row-specific column permuting rules
- The parameters of 2-D matrix are defined in Table-2.

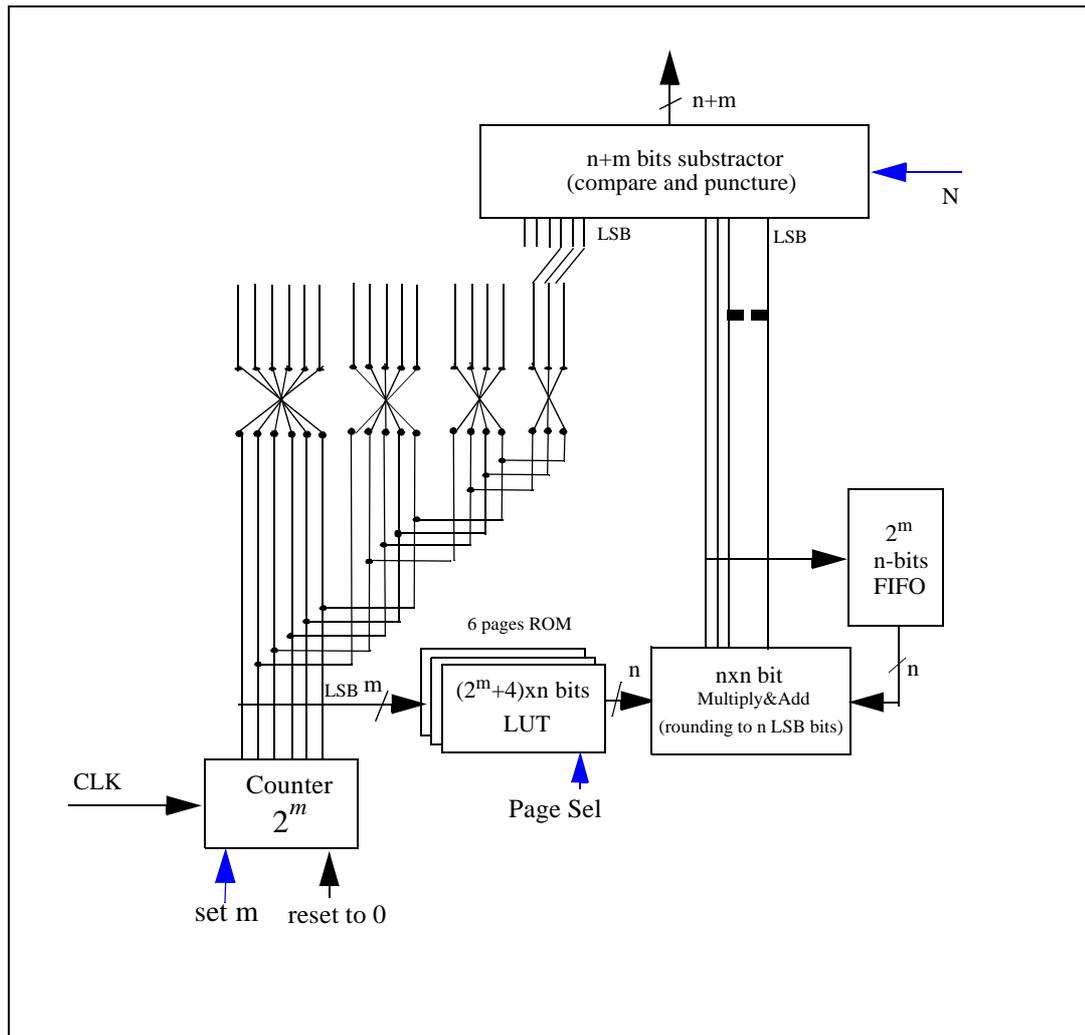
TABLE 2. Interleaver Parameters for 3GPP

α_j $j = 1 \dots 2^n$	L=8*32 (l,m,n)=(3,0,5)	L=8*4*16 (l,m,n)=(3,2,4)	L=8*8*16 (l,m,n)=(3,3,4)	L=8*8*32 (l,m,n)=(3,3,5)	L=8*8*64 (l,m,n)=(3,3,6)	L=8*16*64 (l,m,n)=(3,3,7)
$j = 4l + 0$						
$j = 4l + 1$						
$j = 4l + 2$						
$j = 4l + 3$						
β_j						
$j = 1$						
...						
$j = 2^n$						
γ_j						
$j = 1$						
...						
$j = 2^m$						

2.1.3 Implementation

The hardware implementation of the one-stage Turbo interleaver is shown in Figure 1. Such an implementation are designed for immunizing both memory (ROM/RAM) and gate counts of the computing units.

FIGURE 1. Implementation of One-Stage Turbo Interleaver



2.0 Synthesis of Turbo Interleaver for 3GPP

2.1 Combined One-Stage Turbo Interleaver

2.1.1 Interleaver Framework and Parameters

- Bit-Reversal permuting the rows
- Reduced row-specific column permuting rules
- The parameters of 2-D matrix are defined in Table-2.

TABLE 1. Interleaver Parameters for 3GPP

α_j	L=8*32 (m,n)=(3,5)	L=16*32 (m,n)=(4,5)	L=16*64 (m,n)=(4,6)	L=32*64 (m,n)=(5,6)	L=32*128 (m,n)=(5,7)	L=64*128 (m,n)=(6,7)
$j = 4l + 0$						
$j = 4l + 1$						
$j = 4l + 2$						
$j = 4l + 3$						
β_j						
$j=1$						
....						
$j=64$						

2.1.2 Column Permuting Algorithm

The column permuting rule is as follows:

Select $\{m,n\}=\{8,32\} \{16,32\} \{32,32\} \{32,64\} \{64,64\} \{64,128\}$

For $i=1$ to 2^n

$c_j(0) = 1$

For $j=1$ to 2^m

$j_r = \text{Bit_Rev}(j)$

$k = [j_r] \text{mod} 4$

$c_{j_r}(i) = [\alpha_k c_{j_r}(i-1) + \beta_j] \text{mod} 2^n$

$I[(i-1)2^m + j] = j_r 2^n + c_{j_r}(i)$

end

end

1.2 Commonality of Three Turbo Interleavers

As we can see, there are several common features among the three interleavers namely:

- Bit-reversal for row permuting (GF/MIL)
- Multi-stage interleaving by sub-interleaver partitioning (MIL/AL)
- Range prunable design (prunable bits, GF: $<2^{m-1}$, MIL: <8 , AL: <3)
- Row specific column permuting (GF/MIL/AL)

1.3 Implementation Complexity

For ASIC implementation, using congruential recursive rule to compute the index permuting requires the least ROM and gates.

From the flexibility point of view, the 2^m size prunable mother interleaver design is most flexible to adapt to arbitrary desirable frame size. On the other hand, the MIL interleaver requires so-called determining and synthesizing processes to configure an arbitrary given size interleaver, this can only be done only in the initialization software, in hardware, a total 20, reconfigurable RAM or counter have to be designed.

1.0 Elements of the 3GPP Candidate Turbo Interleavers

Four Turbo interleavers are currently considered as candidates for the selection for the 3GPP standard:

- MIL Interleaver
- GF Interleaver
- 2-D Algebraic Interleaver (AL-N)
- 1-D Algebraic Interleaver (AL-C)

After extensive performance evaluations during the UTRA Turbo ad_hoc studies. These Turbo interleaver offer similar good performance. The purpose of this contribution is to present a study to highlight the basic features of first three interleaver and to look into some possibilities to synthesis a combined interleaver design for 3GPP.

1.1 Basic Features of Three Turbo Interleavers

The MIL/GF/AL turbo interleavers are two dimensional (2-D) interleaver.

The basic feature for the MIL Turbo interleaver are:

- For 8-State PCCC, convert the frame into a 2-D $8 \times N$ block matrix
- Permuting 8 rows bit-inverted bit reversal
- Partitioning each row into different sub 2-D interleavers (2nd Stage)
- Continue to partition from 2nd stage until the 2-D interleaver size matched PIP

The basic feature for the GF Turbo interleaver are:

- Design mother interleaver with size 2^m
- To prune the mother interleaver to the arbitrary frame size
- Row permuting by bit reversal to ensure non-consecutive puncture
- Column permuting by using Zech algorithm in GF

The basic feature for the 2-D Algebraic Turbo interleaver are:

- Congruential rule for both column and rule permuting for simple implementation
- Coset partitioning
- Exact frame design or minimized puncturing design

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Title: Comparison of Turbo Interleavers for 3GPP

Source: Nortel Networks¹

0.0 Summary

In this contribution, we present a comparison study of Turbo Interleavers proposed for 3GPP based on the complexity. The possible synthesis of combined turbo interleaver schemes are discussed.

1 Contact Person: Catherine Gauthier, Nortel Networks
1 Place des Freres Montgolfier, 78042 Guyancourt, France
Tel:+33 1 39 44 57 47
Fax:+33 1 39 44 50 12
e_mail: gauth@nortel.com