TSG-RAN meeting #20 RP-030251
HÄMEENLINNA, Finland, 3 - 6 June

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1#32: Two documents were covered and agreed upon. These documents covered the following aspects:
- link level simulation results for Release 5 type (HSDPA) bearers.
- mobility.

RAN4#27: A document covering the radio aspects of the reference configuration for the higher chip rate study was presented and agreed upon.

List of Completed elements (for complex work items):
- Higher chip rate reference configuration.
- Simulation assumptions
- Link level simulation results for Release 5 type bearers
- Backwards compatibility and mobility sections of feasibility study

List of open issues:
- Link level performance for Release 99 type bearers
- System level performance
- Complexity analysis.
- Feasibility analysis.

Estimates of the level of completion (when possible):
35-40%

SI completion date review resulting from the discussion at the working group:
RAN#22 (Dec 2003)

References to WG's internal documentation and/or TRs:

R1-030634 “TR25.895 v1.0.1 : Analysis of higher chip rates for UTRA TDD evolution”