

Status Report for SI to TSG

Study Item Name: Improvement of Inter-frequency and inter-system measurement for 1.28Mcps TDD

SOURCE: Rapporteur

TSG: RAN

WG: WG1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1:

In RAN1#30,

[1][2] [3] discussed function impact on power control, uplink synchronization and signalling issues due to asymmetric pattern and pattern combination schemes. Several comments were proposed to further revise the related text proposal in [1][2]. It was concluded that more generic and high level analysis on signalling impact were needed for [3] and then WG2/WG3 will in WI phase address SRNC/CRNC signalling flows etc. Usage of DTX was proposed in [4] to be studied for inter-frequency and inter-system measurement while there were concerns about availability of DTX for this measurement purpose.

In RAN1#31:

[5][6] [7] presented further revised documents on above issues. It was commented [5] needs also consider higher interference level offset to cover enough generic case and simulation is needed to verify performance analysis in [6]. [7] was commented that some re-wording and more consideration are needed. Finally, these three documents were noted and further results and re-wording are needed in the next meeting. [8] gave the text proposal for the conclusion part of TR25.888. It was postponed to wait for further progress on previous topics, therefore [8] was not presented in RAN1.

RAN2: There is no progress since the last TSG RAN meeting.

RAN3: There is no progress since the last TSG RAN meeting.

RAN4: There is no need of further progress.

List of Completed elements (for complex work items):

RAN1:

Agreement on the study areas of the SI

Completion of the performance evaluation and simulation for the asymmetric time slot allocation pattern to all the possible scenarios with configuration 4 DL, 3 UL time slot.

Completion of the performance evaluation and simulation for the combination of different time slot allocation pattern with configuration 4 DL, 3 UL time slot.

RAN2: Clarification of the SI.

RAN3: Completion of internal skeleton TR for signalling support.

RAN4: Agreement on the impact to the WG4 related specifications

List of open issues:

- Further performance results and analysis on power control impact and uplink synchronization impact for asymmetric pattern and pattern combination schemes.
- More consideration and re-wording for the signalling impact analysis for asymmetric pattern and pattern combination schemes.

Estimates of the level of completion (when possible):

55 %

SI completion date review:

Considering still some open issues and current RAN1 meeting schedule, it is proposed to change the completion date from Mar. 2003 to Sep. 2003 in TSG RAN #21.

References to WG's internal documentation and/or TRs:

- [1] 3GPP TSG R1 030046 "Analysis of asymmetric pattern and pattern combination scheme impact on power control", Samsung Electronics, Jan. 2003.
- [2] 3GPP TSG R1 030047 "Analysis of asymmetric pattern and pattern combination scheme impact on uplink synchronisation", Samsung Electronics, Jan. 2003.
- [3] 3GPP TSG R1 030056 "Analysis of Signalling impact on the improvement of Inter-frequency and inter-system measurement for 1.28Mcps TDD", Samsung Electronics, Jan. 2003.
- [4] 3GPP TSG R1 030097 " Analysis on inter-frequency and inter-system measurement with DTX & DCA", Siemens, Jan. 2003.
- [5] 3GPP TSG R1 030214 "Further analysis of asymmetric pattern and pattern combination scheme impact on power control", Samsung Electronics, Feb. 2003.
- [6] 3GPP TSG R1 030215 "Further analysis of asymmetric pattern and pattern combination scheme impact on uplink synchronisation", Samsung Electronics, Feb. 2003.
- [7] 3GPP TSG R1 030216 "Further analysis of signalling impact on the improvement of inter-frequency and inter-system measurement for 1.28Mcps TDD", Samsung Electronics, Feb. 2003.
- [8] 3GPP TSG R1 030217 "Text proposal for conclusion part of TR25.888", Samsung Electronics, Feb. 2003.