TSG-RAN Meeting No. 15 *TSGRP-020120*
March 5-8, 2002 Jeju, Korea

Status Report for SI to TSG

Study Item Name: Mitigating the Effect of CPICH Interference at the UE

SOURCE: Rapporteur (Shimon Moshavi, Intel) **TSG:** RAN **WG: 4**

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Ref. to WI sheet: RAN_Work_Items.doc, Study Item 8

Progress Report since the last TSG (for all involved WGs):

Several additional contributions were presented at the previous RAN 4 meeting (#21) on this topic [20-28]. Additional link level simulations were reported in [20,21]. An assessment of the link level simulation scenarios that were included in V1.0.0 of the TR [15] was presented in [22], which led to the removal of some of the scenarios in V2.0.0 of the TR presented here [27]. A view of the costs and benefits of CPICH interference mitigation was summarized in [23], and a number of additional potential benefits were described in [24]. An analysis of the effects of timing errors on CPICH mitigation accuracy was presented in [25], with a response document presented in [26].

A proposed way forward for the Study was presented in [28], which was endorsed by RAN 4. This document included the text for the Conclusion/Recommendations section of the TR, and a recommendation for a new Work Item to be proposed at the current RAN meeting, (see RP-020124 of this meeting, "WI Proposal: Improving receiver performance requirements for the FDD UE"). The document represented the consensus that various feasible approaches exist to provide some improvements in Release 6 UE receiver performance requirements, although it was stressed that each company should be free to choose its preferred approach to meet any new requirements. Based on document [28], the contents of Version 2.0.0 of the Technical Report 25.991 were agreed upon at the meeting. The exact text of the TR has been available on the RAN4 email reflector since Feb. 8, 2002.

List of Completed elements (for complex work items):

In addition to background material [1-4,6,7], the Study has addressed 3 main areas:

- Radio Network Simulations to Evaluate Capacity Gains - Extensive voice capacity simulations were reported by Intel, Nokia, Motorola, and Telia, with compatible results [8-12]. In addition, one set of data capacity simulations (for 64 kbps and 144 kbps services) was presented illustrating increased gains over the voice capacity scenario [9]. Reference [12] also addressed scenarios where CPICH power is constrained to be large due to regulatory requirements.
- Link Level Simulations to Evaluate Feasible Accuracy of Cancellation: Reference [9] reported extensive simulation results illustrating a relatively high degree of cancellation accuracy for the cases considered. Reference [13] considered the performance of CPICH mitigation under extreme pessimistic timing error conditions, and found that gains remain, although reduced. Reference [16] found relatively high cancellation accuracy is feasible even in a 7-sector scenario, which included both stronger cells in a handover state, and weaker neighbor cells.
- Complexity - Reference [5] addressed the implementation complexity of mitigating CPICH interference effects by providing upper bounds on gate count, DSP requirements, and current consumption. Reference [14] considered gate count and confirmed the results in [5]. Reference [9] extended the complexity assessment to Transmit Diversity and Multi-Code operation. Reference [19] corrected the power consumption estimate given in [5].

List of open issues:

None

Estimates of the level of completion (when possible):

100%

SI completion date review resulting from the discussion at the working group:

March 2002

References to WG's internal documentation and/or TRs:

[1] 3GPP TSGR1-00-1371, “CPICH interference cancellation as a means for increasing DL capacity,” Intel Corporation, Nov. 2000.

[2] 3GPP TSGR1-00-0030, “Further Results on CPICH Interference Cancellation as A Means for Increasing DL Capacity,” Intel Corporation, Jan. 2001.

[3] 3GPP TSGR4-01-0238, “CPICH Interference Cancellation as a Means for Increasing DL Capacity,” Intel Corporation, Feb. 2001.

[4] 3GPP TSGRP-01-0177, “Mitigating the Effect of CPICH Interference at the UE,” Intel Corporation, Mar. 2001.

[5] 3GPP TSGR4-01-0650, “On the Implementation Complexity of CPICH Interference Cancellation,” Intel Corporation, May 2001.

[6] 3GPP TSGR4-01-1014, “On the potential capacity gain of CPICH interference mitigation,” Intel Corporation, July 2001.

[7] 3GPP TSGR4-01-1015, “Study description for SI: Mitigating the effect of CPICH interference at the UE,” Intel Corporation, July 2001.

[8] 3GPP TSGR4-01-0967, “CPICH cancellation,” Motorola, July 2001.

[9] 3GPP TSGR4-01-1330, “Feasibility Assessment for CPICH Interference Mitigation”, Intel Corporation, September 2001.

[10] 3GPP TSGR4-01-1230, “CPICH cancellation, 2-way soft handoff capacity gain” Motorola, September 2001.

[11] 3GPP TSGR4-01-1202, “Simulation results for CPICH interference mitigation” Nokia, September 2001.

[12] 3GPP TSGR4-01-1256, “Capacity gain from CPICH cancellation”, Telia, September 2001.

[13] 3GPP TSGR4-01-1231, “CPICH cancellation, UE sample time offsets,” Motorola, September 2001.

[14] 3GPP TSGR4-01-1232, “CPICH cancellation complexity” Motorola, September 2001.

[15] 3GPP TSGR4-011499, “TR 25.991 V1.0.0 Feasibility Study of the Mitigation of the Effect of the Common Pilot Channel (CPICH) Interference at the User Equipment,” Rapporteur, Nov. 2001.

[16] 3GPP TSGR4-011455, “CPICH Interference Mitigation Accuracy,” Intel Corp., Nov. 2001.

[17] 3GPP TSGR4-011453, “Link Level Simulation Results for CPICH Cancellation,” Nokia, Nov. 2001

[18] 3GPP TSGR4-011392, “Comments on the CPICH Interference Cancellation Scheme,” Ericsson, Nov. 2001.

[19] 3GPP TSGR4-011483, “Correction on CPICH Interference Mitigation Complexity,” Intel Corp. Nov. 2001.

[20] 3GPP TSGR4-020274, “Link simulation results for CPICH mitigation,” Nokia, Jan. 2002.

[21] 3GPP TSGR4-020358, “Simulations of the CPICH mitigation scheme,” Ericssion, Jan. 2002.

[22] 3GPP TSGR4-020273, “Received signal levels in SHO area and noise rise in special scenarios,” Nokia, Jan. 2002.

[23] 3GPP TSGR4-020440, “Costs and benefits of CPICH interference mitigation,” Intel Corp., Jan. 2002.

[24] 3GPP TSGR4-020338, “Additional benefits from CPICH interference mitigation,” Intel Corp., Jan. 2002.

[25] 3GPP TSGR4-020353, “Impact of timing errors on accuracy of CPICH cancellation,” Qualcomm, Jan. 2002.

[26] 3GPP TSGR4-020439, “Response to R4-020353 ‘Impact of timing errors on accuracy of CPICH Cancellation,” Intel Corp., Jan. 2002.

[27] 3GPP TSGR4-020520, “Proposed way-forward for CPICH interference mitigation SI,” Intel Corp., Jan. 2002.

[28] 3GPP TSGRP-020121, “TR 25.991 V2.0.0 Feasibility Study of the Mitigation of the Effect of the Common Pilot Channel (CPICH) Interference at the User Equipment,” Rapporteur, Mar. 2002.