

**Source:** Rapporteur

**Title:** Status Report of SI "Mitigating the Effect of CPICH Interference at the UE"

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This document provides a status report of the Study Item "Mitigating the Effect of CPICH Interference at the UE". TSG-RAN WG4 is the lead working group for this study item. A technical report has not yet been created.

#### **RAN WG4**

At the most recent RAN WG4 meeting, (RAN4 #17), a contribution (Tdoc TSG-R4-0650) was presented that addressed the implementation complexity of mitigating CPICH interference effects, by considering a particular form of interference cancellation. The contribution described the concept of selecting only the stronger CPICH interference terms for estimation and cancellation, in order to reduce complexity. It also provided an upper-bound evaluation of complexity in terms of hardware gate count, DSP requirements, and current consumption. Additional simulation results for performance evaluation, and input from additional companies on this SI were requested.