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Postal address

3GPP support office address

650 Route des Lucioles - Sophia Antipolis
Valbonne - FRANCE
Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Internet

http://www.3gpp.org

Contents

Foreword

This Technical Specification has been produced by the 3rd Generation Partnership Project (3GPP).

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of the present document, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

Version x.y.z

where:

- x the first digit:
  - 1 presented to TSG for information;
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  - 3 or greater indicates TSG approved document under change control.
- y the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.
- z the third digit is incremented when editorial only changes have been incorporated in the document.

1 Scope

The present document is the Technical Report of the Release 2000 work item “Terminal Power Saving Feature”.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

?? References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.

?? For a specific reference, subsequent revisions do not apply.

?? For a non-specific reference, the latest version applies.

[1] 3G TS 25.211 (V3.2.0): "Example 1, using sequence field".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply.

Example: text used to clarify abstract rules by applying them literally.

3.2 Symbols

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

CFN Connection Frame Number
DPCCH Dedicated Physical Control Channel
DPCH Dedicated Physical Channel
DSCH Downlink Shared Channel
PDSCH Physical Downlink Shared Channel

4 Background and Introduction

Battery life is an important resource in UE side but there’s few explicit features dedicated to UE battery saving in Release 99 specification. In order to enhance the UE battery life with respect to Release 99, terminal power saving feature is under discussion for in Release 2000 work item. In this technical report, the requirements and detail solutions are described.

5 Requirements to the Solution

This section describes the requirements to the solution of terminal power saving feature. It includes the level of changes and expected gains with respect to Release 99.

5.1 Level of Changes with respect to Release 99

5.1.1 Gated DPCCH Transmission Scheme in FDD

Detail parameters and procedure of gated DPCCH transmission is covered in subclause 6.1.

5.1.1.1 Required Changes in UE

When a UE supports gated transmission, the UE should have a capability of determining turn-on and turn-off time slot of uplink and/or downlink for transmission and reception. In gating mode, the uplink power should be adjusted based on the power control command in latest downlink turned-on time slot.

5.1.1.2 Required Changes in Node B

When a Node B supports gated transmission, Node B should be able to determine uplink and/or downlink turn-on and turn-off time slot for transmission and reception. In gating mode, the downlink power should be adjusted based on the power control command in latest uplink turned-on time slot.

5.2 Expected Gain with respect to Release 99

In Release 99, UE battery life was not considered explicitly as a requirement to the specification. With the terminal power saving features, UE battery life can be extended with respect to Release 99 and the interference can also be reduced by the reduced transmission power in uplink and/or downlink.

6 Terminal Power Saving Features

In this section, the solutions for the terminal power saving features are described.

6.1 Gated DPCCH Transmission Scheme in FDD

Gated DPCCH transmission scheme (hereafter, “gating” or “gating mode” are used interchangeably.) is basically reduced power control rate operation to get power saving and interference reduction. Gating can be applied when the UE is in Cell-DCH State with DSCH. When both UTRAN and UE support gating, UTRAN can initiate the gated DPCCH transmission by higher layer signaling. UTRAN can terminate the gating by higher layer signaling [or physical indication such as TFCI]. Gated DPCCH transmission is a scheme where transmitter turns off its transmission intermittently when there is no traffic data to transmit on both uplink and downlink DPDCH. Gating should be terminated before transmitting traffic data.

There are two kinds of period in gating mode depending on the transmission of (non-traffic) DPDCH during gating. In Normal Gating Period, DPDCH is not transmitted and this mode is described in section 6.2.3.1. However, even during gating mode, DPDCH can be transmitted without terminating the gating exceptionally for the short length signaling message. This Embedded DPDCH Period is described in section 6.1.3.2.

6.1.1 Related Parameters

When the call is setup, UTRAN and UE negotiate the gating capability and parameters. The parameters controlling the gating operation are:

Table 1. Gating Parameters

Gating Rate	1	1/3	1/5

Gating Mode	Downlink Only	Uplink and Downlink

6.1.2 Initiation and Termination Indication of Gated DPCCH Transmission

The gated DPCCH transmission can be initiated by the UTRAN's command to UE. Gated DPCCH transmission can be terminated by UE's request followed by UTRAN's permission or by UTRAN's notice to UE. That is, UTRAN determines whether gated DPCCH transmission is initiated or terminated. Gating is initiated by higher layer signaling, and terminated either by higher layer signaling or alternatively by TFCI defined differently during gating for informing gating should be terminated.

6.1.3 Operation in Gated DPCCH Transmission Mode

During gating mode, higher layer signaling message can be transmitted without terminating the gating. The transmitter operation when the DPDCH is not transmitted (Normal Gating Period) is covered in section 6.1.3.1. The transmitter operation when the DPDCH is transmitted (Embedded Gating Period) is covered in section 6.1.3.2. Figure 1 and 2 are the conceptual state transition diagram of "uplink and downlink" and "downlink only" gated DPCCH transmission, respectively.

6.1.3.1 Normal Gating Period

6.1.3.1.1 Uplink and Downlink Gating

In Normal Gating Period, UE shall turn its transmitter on only for the time slots specified in Table 3 and turn its transmitter off in all other time slots.

In Normal Gating Period, UTRAN shall turn on the transmission of TFCI all the time slots. On the other hand, UTRAN shall turn on the transmission of TPC and PILOT field only for the time slots specified in Table 2. UTRAN shall turn off the transmission in remaining part.

6.1.3.1.2 Downlink Only Gating

In Normal Gating Period, UE shall always turn on its transmitter and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI) in downlink only gating mode. Because TPC field can be updated only for the associated downlink turn-on time slot, downlink power control rate and operation should not be changed during gating.

In Normal Gating Period, UTRAN shall turn on the transmission of TFCI in all the time slots. On the other hand, UTRAN shall turn on the transmission of TPC and PILOT only for the time slots specified in Table 2. UTRAN shall turn off the transmission in remaining part.

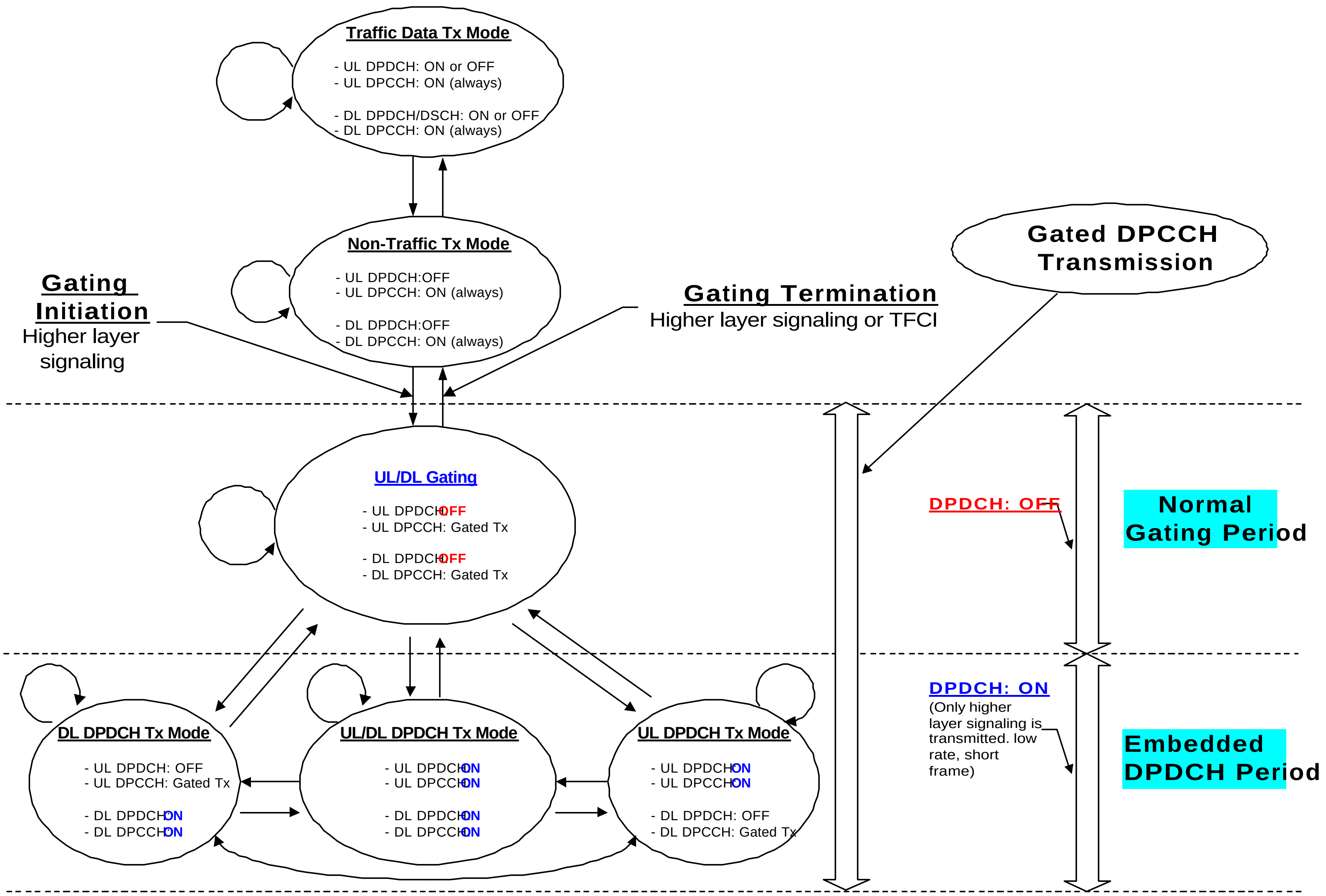

Figure 1. Conceptual State Transition Diagram of Gating: Uplink and Downlink Gating

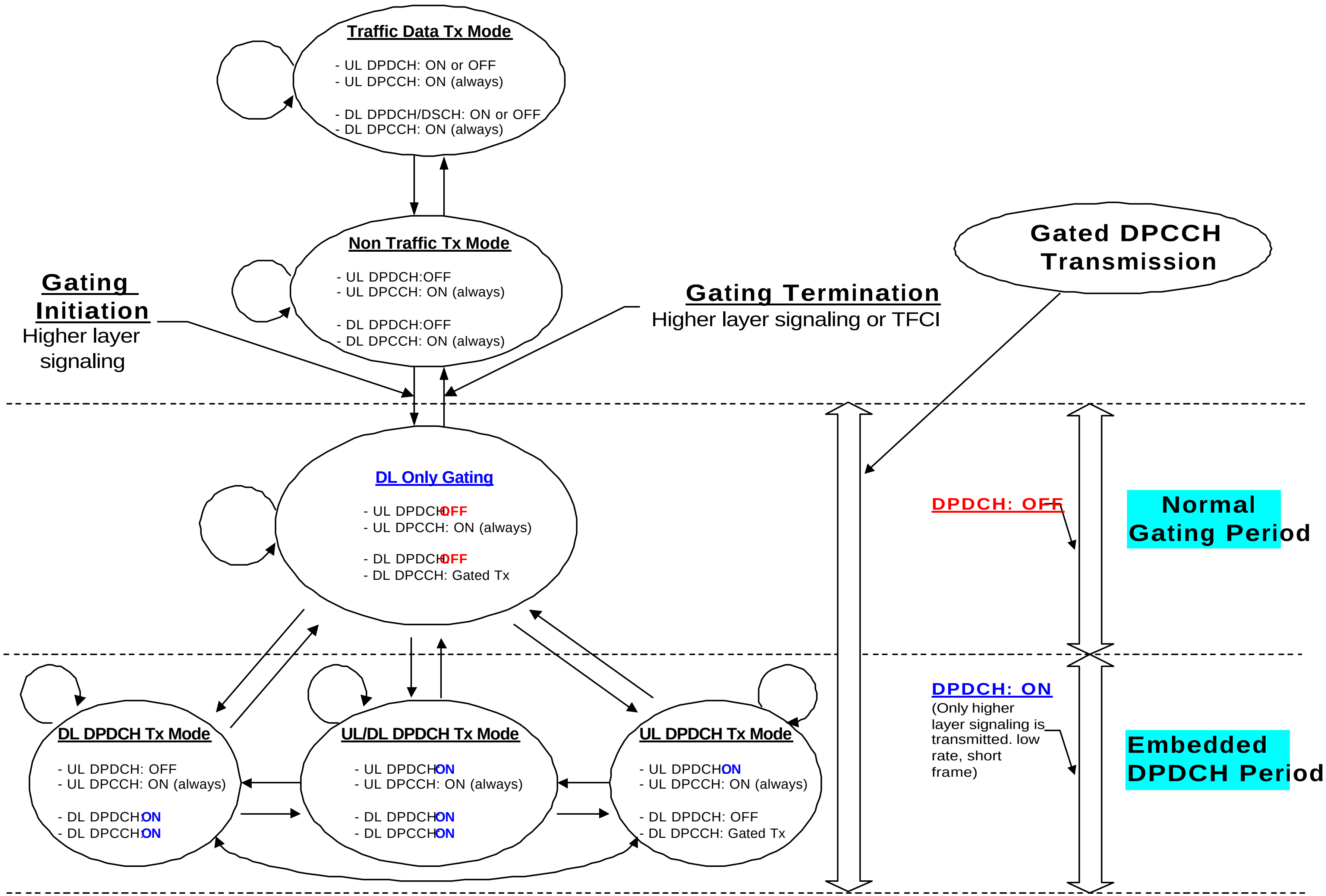

Figure 2. Conceptual State Transition Diagram of Gating: Downlink Only Gating

6.1.3.2 Embedded DPDCH Period

There are a number of advantages by permitting transmission of higher layer signaling message without terminating the gating. First, unnecessary signaling to initialise and terminate gating can be avoided. Second, the average duration of gating can be increased and terminal power consumption can be decreased further.

In Embedded DPDCH Period in gating mode, L1 control information (DPCCH) should be transmitted in all the time slots to help reception but the power control rate should not be changed. That is, if DPDCH is transmitted in downlink in gating mode, UTRAN turns-on all the time slots, but UE shall not change the uplink turn-on and turn-off time slot, and vice versa.

6.1.3.2.1 Uplink and Downlink Gating

In Embedded DPDCH Period in uplink, UE shall turn its transmitter on all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI) but TPC shall be updated only at the time slot specified in Table 3.

In Embedded DPDCH Period in downlink, UTRAN shall turn its transmission on all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC) but TPC shall be updated only for the time slot specified in Table 2.

6.1.3.2.2 Downlink Only Gating

In Embedded DPDCH Period in uplink, UE shall turn its transmitter on all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI) but TPC and shall be updated only after receiving downlink time slot specified in Table 2.

In Embedded DPDCH Period in downlink, UTRAN shall turn its transmission on all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC) but TPC shall be updated only for the time slot specified in Table 2.

6.1.4 Detection of DPDCH frame during Gating

During gating, higher layer signaling message can be transmitted in uplink and/or downlink DPDCH frame, but receiver should detect the frame because the receiver does not know the transmitter period (Normal Gating or Embedded DPDCH Period). UE can determine the existence of downlink DPDCH frame by decoding downlink TFCI because downlink TFCI field is always transmitted. In uplink, UTRAN shall not use TFCI to detect the uplink DPDCH frame since part of uplink TFCI in a frame may not be transmitted. One possible solution for the frame detection in UTRAN is the pilot energy comparison. Pilot energy in the uplink time slots that do not contain pilot during gating is compared to pilot energy in those slots that contains pilot during gating. If this is above threshold, then UTRAN decodes the uplink TFCI and uplink DPDCH frame.

6.1.5 DPCCH Switch-On Time Slot

6.1.5.1 Downlink DPCCH Switch-On Time Slot

In downlink, UTRAN shall turn on the transmission of TFCI all the time slots while turn on the transmission of TPC and PILOT only for the time slots specified in Table 2. In the table, the CFN of the radio frame is denoted by i, and the range of the gating group number j defined in subclause 6.1.5.3 is $j = 0, 1, 2, 3, 4$ for gating rate 1/3, and $j = 0, 1, 2$ for gating rate 1/5. The function $s(i,j)$ used for the reference pattern is defined in subclause 6.1.5.3.

Table 2. Switched-on Time Slots for downlink DPCCH.

Gating rate	Switched-on Time Slots for downlink DPCCH fields		
	Pilot	TPC	TFCI
1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
1/3	j ? 3 + $s(i,j)$ – 1	j ? 3 + $s(i,j)$	All slots (0, 1, …, 14)
1/5	j ? 5 + $s(i,j)$ – 1	j ? 5 + $s(i,j)$	All slots (0, 1, …, 14)

6.1.5.2 Uplink DPCCH Switch-On Time Slot

In uplink, UE shall turn on the transmission of PILOT, TFCI, TPC, and FBI only for the time slots specified in Table 3.

Table 3. Switched-on Time Slots for uplink DPCCH.

Gating rate	Switched-on Time Slots for uplink DPCCH fields Pilot, TFCI, FBI, TPC
1	All slots (0, 1, …, 14)
1/3	$j ? 3 + s(i,j)$
1/5	$j ? 5 + s(i,j)$

6.1.5.3 Reference Pattern

15 slots of the radio frame are divided into N gating groups, each group consists of S consecutive slots. For gating rate 1/3, $N = 5$ and $S = 3$, and for gating rate 1/5, $N = 3$ and $S = 5$. Denote the CFN of the current radio frame by i, $i = 0, 1, 2, \ldots, 255$. Further define the 19 bit sequence $(a_{18}, a_{17}, \ldots, a_0) = (1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1)$.

Table 4. Summary of Reference Pattern *s(I, j)*

Parameter	Value	
CFN	0, 1, …, 255 (8bits)	
$a_{18}, a_{17}, \ldots, a_0$	1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1	
gating rate	1/3	1/5
Number of gating group (N)	5	3
Gating group size (S)	3	5

For CFN i, $i = 0, 1, 2, \ldots, 255$, concatenated CFN $C_i ? i ? 256 ? i$, and gating group j, the function $s(i, j)$ is defined as

$$s(i,j) ? \begin{cases} (A_j ? C_i)_{10} \bmod (S ? 1) ? 1, & j ? 0 \\ (A_j ? C_i)_{10} \bmod S, & j ? 1,\ldots,N ? 2 \\ S ? 1, & j ? N ? 1 \end{cases}, \quad i ? 0,1,\ldots,255$$

where $(X)_{10}$ represents the decimal representation of the number X, and $X ? Y$ denotes bit-wise modulo 2 addition of the binary representation of the numbers X and Y. And $A_j ? \sum_{k ? j}^{j ? 15} 2^{k ? j} a_k$, $j=0,1,\ldots,N-2$.

6.1.6 Power Control

6.1.6.1 Power Control Parameters

In this subclause, the power control parameters during and after the gated DPCCH transmission.

- DPC_MODE 0

  In DPC_MODE 0, if gated DPCCH transmission is not initiated, the UE sends a unique TPC command in each slot and the TPC command generated is transmitted in the first available TPC field in the uplink DPCCH.

  During gated DPCCH transmission, both of the transmit time slot and receive time slot in uplink and downlink are not continuous. UE sends a unique TPC command in each switch-on transmit time slot and the TPC command generated based on the switch-on receive time slot is transmitted in the first available TPC field in the uplink DPCCH.

- DPC_MODE 1

In DPC_MODE 1, if gated DPCCH transmission is not initiated, the UE repeats the same TPC command over 3 slots and the new TPC command is transmitted such that there is a new command at the beginning of the frame.

During gated DPCCH transmission, DPC_MODE 1 cannot be used because the transmission of DPCCH field is not continuous. One possible solution is that during gating, DPC_MODE 0 is used instead of DPC_MODE 1 without explicit signaling.

- Algorithm 1

In Algorithm 1, if gated DPCCH transmission is not initiated, UE shall derive a TPC_cmd based on the TPC command(s) received in each slot.

During gated DPCCH transmission, the UE derives a unique TPC command in each switch-on downlink time slot and adjust its transmission power in the first available switch-on transmit time slot.

- Algorithm 2

In Algorithm 2, if gated DPCCH transmission is not initiated, UE shall process received TPC commands on a 5-slot cycle. It emulates smaller step sizes than the minimum power control step specified in subclause 5.1.2.2.1, or to turn off uplink power control by transmitting an alternating series of TPC commands.

During gated DPCCH transmission, Algorithm 2 cannot be used because the downlink transmission of DPCCH field is not continuous. One possible solution is that during gating, Algorithm 1 is used instead of Algorithm 2 without explicit signaling.

- Recovery period

During gated DPCCH transmission, the power control rate is reduced by the amount of gating rate. In order to compensate the effect of reduced power control rate during gating, power control recovery period is used similarly to compressed mode.

- Power control step

During gated DPCCH transmission, power control step can be different from non-gating mode in order to compensate the reduced power control rate.

6.1.6.2 Power Control Procedure

In this subclause, the power control procedure is described.

6.1.6.2.1 Uplink and Downlink Gated DPCCH Transmission

In the case that the gated DPCCH transmission is enabled for both uplink and downlink, the power control operations are as follows.

Uplink transmit power adjustment

UE shall adjust the transmit power in switched-on time slot in response to the latest valid downlink TPC. The change in uplink transmit power shall take place immediately before the start of the pilot field on the uplink DPCCH.

Uplink TPC generation and transmission

UE shall generate the uplink TPC based on the latest valid downlink switched-on time slot, and shall transmit the TPC on the next valid uplink switched-on time slot

Downlink transmit power adjustment

UTRAN shall adjust the transmit power in switched-on time slot in response to the latest valid uplink TPC. The change in downlink transmit power shall take place immediately before the start of the pilot field on the downlink DPCCH

Downlink TPC generation and transmission

UTRAN shall generate the downlink TPC based on the latest valid uplink switched-on time slot, and shall transmit the TPC on the next valid downlink switched-on time slot

6.1.6.2.2 Downlink Only Gated DPCCH Transmission

In the case that the gated DPCCH transmission is enabled only for the downlink, then the power control operations are as follows.

Uplink transmit power adjustment

UE shall adjust the transmit power in response to the downlink TPC received in the valid downlink switched-on time slot. And the uplink transmit power shall remain constant until next valid downlink TPC is received. The change in uplink transmit power shall take place immediately before the start of the pilot field on the uplink time slot.

Uplink TPC generation and transmission

UE shall generate and transmit an uplink TPC based on the valid downlink switched-on time slot. And the UE shall transmit the TPC repeatedly before receiving the next valid downlink switched-on time slot.

Downlink transmit power adjustment

UTRAN shall adjust the transmit power in switched-on time slot in response to the repeated uplink TPC(s) which are known to be the same. The change in downlink transmit power shall take place immediately before the start of the pilot field on the switched-on downlink time slot

Downlink TPC generation and transmission

UTRAN shall generate and transmit downlink TPC based on the uplink time slot(s) whose transmit power is known to be the same.

6.1.6.3 Power Control Transition Period

If gating is terminated by physical signaling such as TFCI, then there is a short period of power control transition.

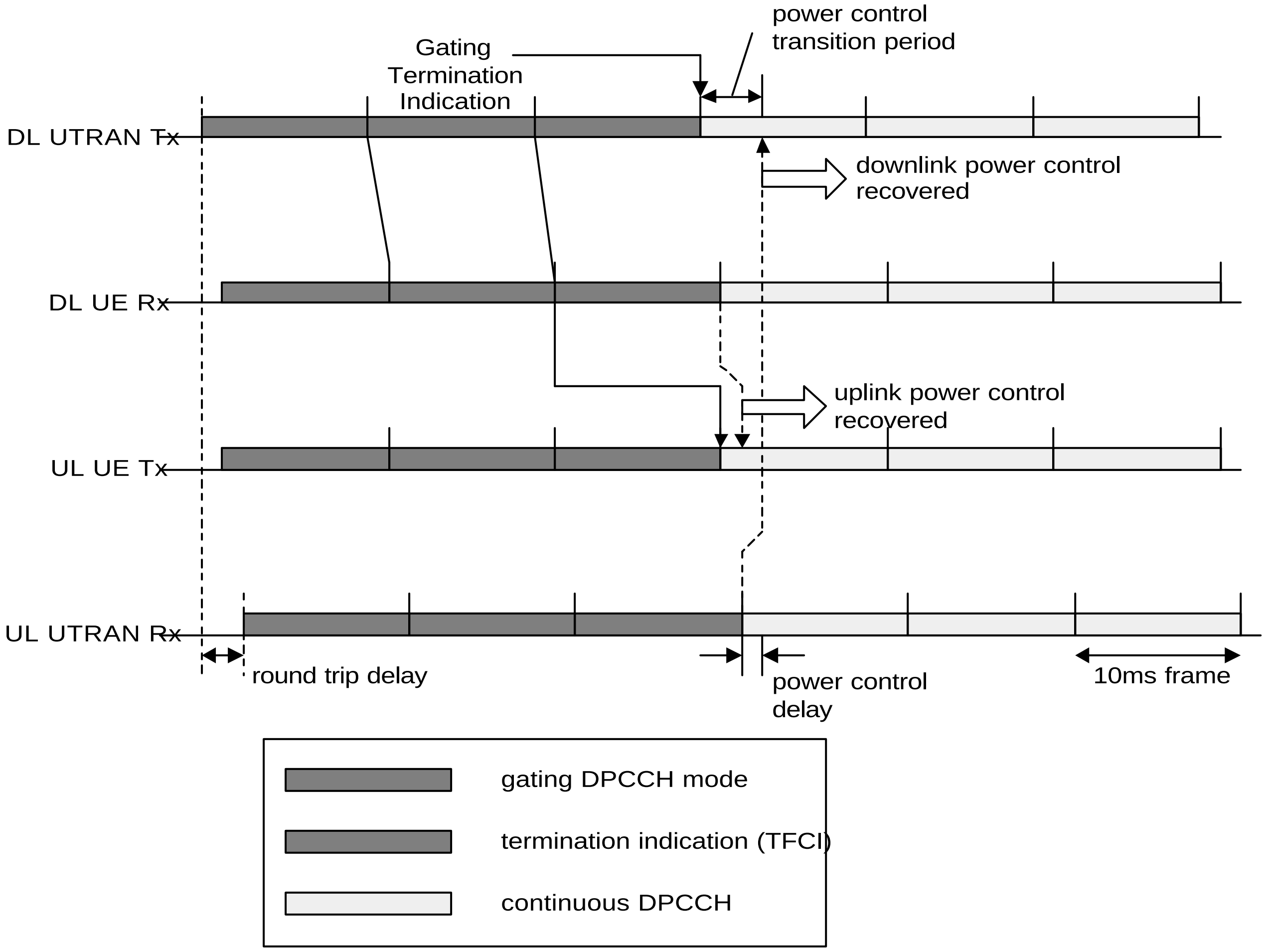

Figure 3. Power control timing and power control transition period

Figure 3 shows the power control timing diagram during transition between gating and non-gating mode. Although there is a short power control transition period (downlink: reduced power control, uplink: fast power control), the duration of transition is comparable to the propagation delay. Therefore, the power control will be stabilised quickly.

6.1.7 Operation with other Features

In this subclause, the required changes in operation of other features when the features are used with gated DPCCH transmission are investigated.

6.1.7.1 Transmit diversity

6.1.7.1.1 Open Loop Transmit Diversity

Since STTD encoding is performed for each time slot unit, there's no impact by gated DPCCH transmission.

6.1.7.1.2 Closed Loop Transmit Diversity

When the gated DPCCH transmission is turned on during closed loop transmit diversity, gating impacts uplink feedback signaling. For closed loop transmit diversity Mode 1, it will work without changes. For closed loop transmit diversity Mode 2, one possible solution is that during gating, Mode 1 is used instead of Mode 2 without explicit signaling. If the Mode 1 is used instead of Mode 2 during gated DPCCH transmission, the Tx diversity mode should be return to Mode 2 without explicit signaling when the gated DPCCH transmission is terminated.

6.1.7.2 Compressed mode

If the compressed mode is initiated during gated DPCCH transmission, gating shall be disabled. It means that the gating should be terminated before inter-frequency and inter-system hard handover.

6.1.7.3 Soft Handover

If any of the Node Bs in the Active set do not support gated transmission, gated DPCCH transmission shall be disabled. In other words, if a new radio link is setup during gating mode and the Node B of the newly added radio link does support gating, then the gating shall be terminated.

6.1.7.4 SSDT

Gated DPCCH shall be disabled when the soft handover is initiated with SSDT.

7 Impacts to WGs

In this subclause, the technical specifications of each WG that may be impacted by each solution for terminal power saving features are listed.

7.1 Gated DPCCH Transmission Scheme

7.1.1 WG1

TS 25.214

7.1.2 WG2

TS 25.301

TS 25.302

TS 25.331

7.1.3 WG3

TS 25.423

TS 25.433

7.1.4 WG4

TS 25.101

8 Performance

8.1 Gated DPCCH Transmission Scheme

8.1.1 Uplink Interference Reduction Gain [1]

In gating mode, the following transmission cases are possible.

- DPCCH only transmission
- DPDCH and DPCCH transmission

That is, as shown in Figure 4, DPCCH is always transmitted but DPDCH can be transmitted when there's data to transmit during gating mode. (Here, for example, DPDCH transfers low rate data such as signaling message that is usually transmitted occasionally. Let "DPDCH frequency" be the probability of transmitting DPDCH during gating mode.)

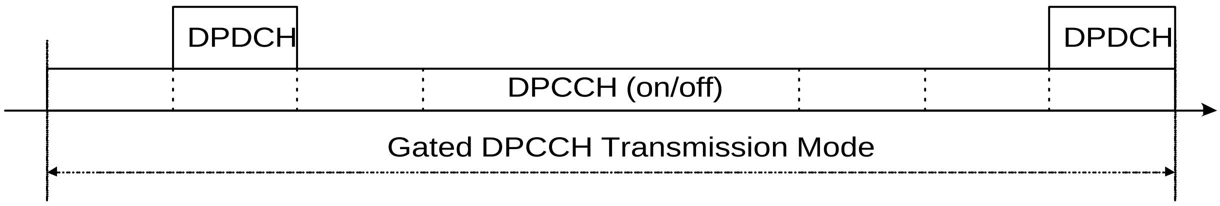

Figure 4. DPDCH Transmission during gated DPCCH transmission mode

The average interference reduction gain is defined as:

Average Uplink interference reduction gain

= (average transmit power when no gating)/(average transmit power when gating)

Note that the average uplink interference reduction gain is defined as the ratio of the average transmission power. Although the transmit power of DPDCH should be increased to compensate the reduced power control rate, the transmit power can be saved during DPCCH only transmission period. Thus the average interference reduction gain highly depends on the DPDCH frequency, and the results are shown with respect to the DPDCH frequency ranges from 1% to 30%.

Simulation and analysis results show that the average interference reduction gain is 4~6dB if the DPDCH frequency is 1%, 2.0~2.5dB if the DPDCH frequency is 10%. Since the average interference reduction gain the ratio of average transmit power, the gated DPCCH transmission provides gain in terms of UE Tx power saving.

8.1.1.1 Link level simulation

8.1.1.1.1 Simulation parameters

The link-level simulation was performed to evaluate the required Eb/No of uplink DPDCH during gated DPCCH transmission mode. Note that the performance of the uplink DPDCH depends on the uplink power control rate (downlink TPC rate). More precisely, the FER of uplink DPDCH is simulated when the downlink TPC is transmitted with rate 1, 1/3, and 1/5. The channel models are CASE1 for 3km/h and CASE3 for 120km/h. The detail simulation parameters are shown in table 5.

Table 5. Simulation parameters (uplink)

Carrier frequency		2.0 GHz
Chip rate		3.84 Mcps
Channel bit rate	DPDCH	60 kbps
	DPCCH	15 kbps
Modulation	Data	BPSK
	Spreading	QPSK
Slot structure	DPCCH	Pilot: 6, TPC: 2, TFCI: 2
	DPDCH	Data: 40
Channel model	Multi-path fading	2-path Rayleigh
	Finger	2 fingers
	Receiver antenna diversity	On
	Doppler frequency [Hz]	5.6(3km/h) , 222(120km/h)
DPCCH/DPDCH [dB]		-5dB
Power control	Dynamic range	Unlimited (assume ideal power amplifier)
	Step size	1.0 dB
	Rate	1500Hz(1/1 gating = no gating), 500Hz(1/3 gating), 300Hz(1/5 gating)
	TPC error	4%
Channel estimation		WMSA

8.1.1.1.2 Simulation results

Figure 5 and 6 show the uplink DPDCH FER when the downlink TPC is transmitted with rate 1, 1/3, and 1/5, where R represents gating rate.

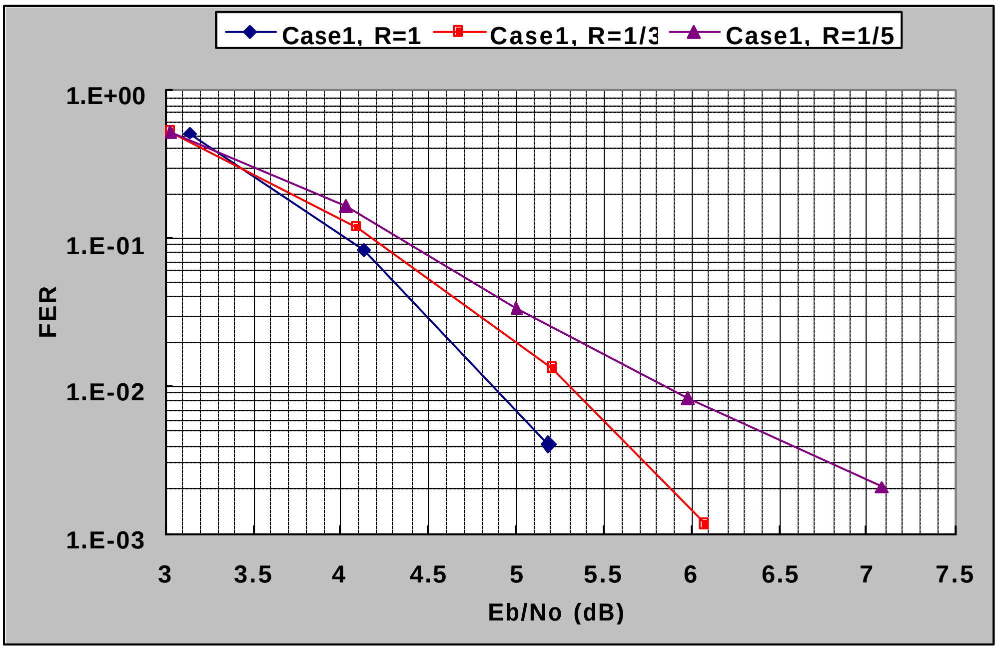

Figure 5. Uplink DPDCH Frame Error Rate with various gating rate and speed (Case 1)

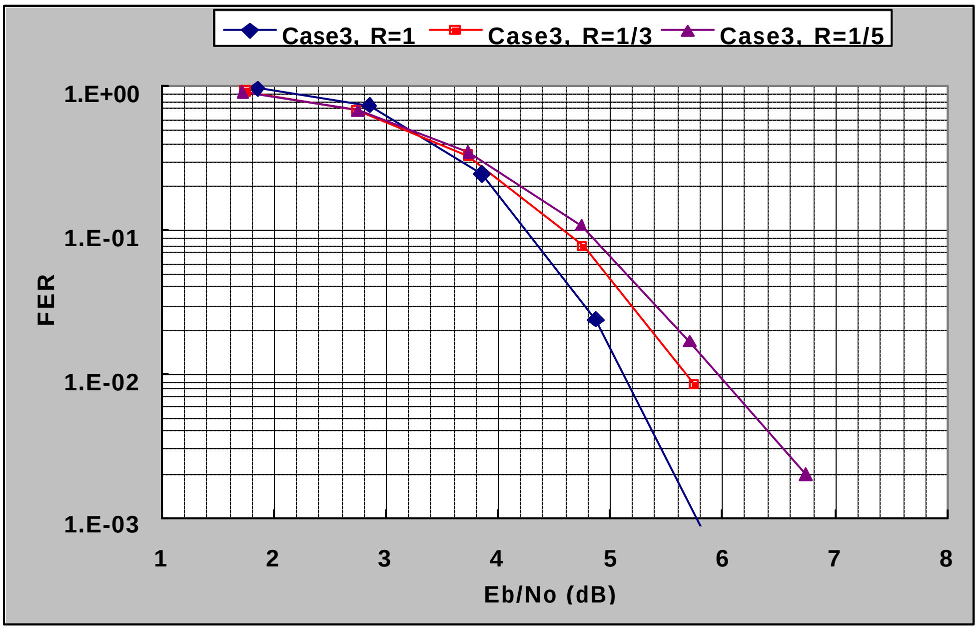

Figure 6. Uplink DPDCH Frame Error Rate with various gating rate and speed (Case 3)

The required transmit Eb/No for the uplink DPDCH to obtain 1% FER is summarised in table 6. In addition, the Eb/No difference compared with gate rate 1 is also given. From the results, we can see that the Eb/No loss by 1/3 rate gating at 3km/h is about 0.42dB, for example. The uplink DPCCH performance loss, which is measured by TPC BER, due to gated DPCCH transmission is max. 0.5dB for gating rate=1/5.

Table 6. Required Tx E_b/N_0[dB] to maintain 1% FER

UE speed	Gating Rate		
	1/1	1/3	1/5
Case1(3km/h)	**4.88**	5.3(+0.42)	5.88(1.0)
Case3(120km/)h	**5.1**	5.68(0.58)	6.0(0.9)

* ( ) indicates Eb/No difference compared with 1/1(no gating)

Tx. $E_b = E_{DPDCH} + E_{DPCCH}$ per one antenna

8.1.1.2 Uplink Interference Reduction Gain

In this subsection we analyse the average uplink interference reduction gain in gated DPCCH transmission mode based on the link simulation results in subsection 2.2. The disadvantage of the gated DPCCH transmission is the increase of the required Eb/No to obtain 1% DPDCH FER. In addition, the transmit power of DPCCH also should be increased due to reduced uplink power control rate. The average uplink interference reduction gain is defined in section 1 and restated for convenience.

Average uplink interference reduction gain

= (Average transmit power when no gating)/(Average transmit power when gating)

In order to see the gain, let's assume the following parameters.

F = DPDCH frequency (%),
R = Gating rate (1, 1/3, or 1/5)
P_{DPCCH} = Power of DPCCH,
P_{DPDCH} = Power of DPDCH = ? ? P_{DPCCH} (? =5dB)
A_{DPCCH} = Additional Eb/No required for DPCCH only transmission (0.5dB)

A_{DPCH} = Additional Eb/No required for DPDCH+DPCCH transmission (Given in table 2)

From the assumed parameters, only DPCCH is transmitted in F% of time, and both (DPDCH+DPCCH) are transmitted in (100-F)% of time. The average uplink interference reduction gain is defined as the ratio of average transmission power as follows.

Average Uplink Interference Reduction Gain

Average uplink interference reduction gain

= 10 * log10 (P(no gating)/P(gating))

where P(no gating) and P(gating) represents the average transmit power when the gated DPCCH transmission is disabled and enabled, respectively.

P(no gating)

The average transmit power when the gated DPCCH transmission is disabled is given by

P(no gating) = (Average transmit power when no gating)

= (100-F) * P_{DPCCH} + F * (P_{DPCCH} + P_{DPDCH})

= (100+ ? ? F) P_{DPCCH}

P(gating)

The average transmit power when the gated DPCCH transmission is enabled is given by

P(gating) = (Average transmit power during only DPCCH transmission when gating)

+ (Average transmit power during (DPDCH+DPCCH) transmission when gating)

During DPCCH only transmission period, the average transmit power is given by

(Average transmit power during only DPCCH transmission when gating)

= (100-F) * P_{DPCCH} * 10^(0.1*A_{DPCCH})* R

During both (DPDCH+DPCCH) transmission period, there is E_{DPCH} loss, so the required power is

(Average transmit power during (DPDCH+DPCCH) transmission when gating)

= F * (P_{DPCCH} + P_{DPDCH}) * 10^(0.1*A_{DPCH}).

Based on the above method, we calculate the average uplink interference reduction gain for 1% DPDCH frequency as table 7 (F=1).

Table 7. Uplink interference reduction [dB] (1% DPDCH frequency)

UE speed	Overall interference reduction gain [dB]	
	1/3	1/5
3km/h	**3.94**	**5.75**
120km/h	**3.93**	**5.77**

Consequently, in case of 1% DPDCH frequency, the uplink interference reduction gain (~5.77dB) can be achieved by gated DPCCH transmission in spite of increasing transmission power of DPDCH during gating. The DPDCH frequency has an important role in the uplink interference reduction gain. Figure 7 shows the average uplink interference reduction gain against the DPDCH frequency. From these figures, we can see that more than 2.5dB gain can be achieved when the DPDCH frequency is 10%, and the gain increases as the DPDCH frequency decreases.

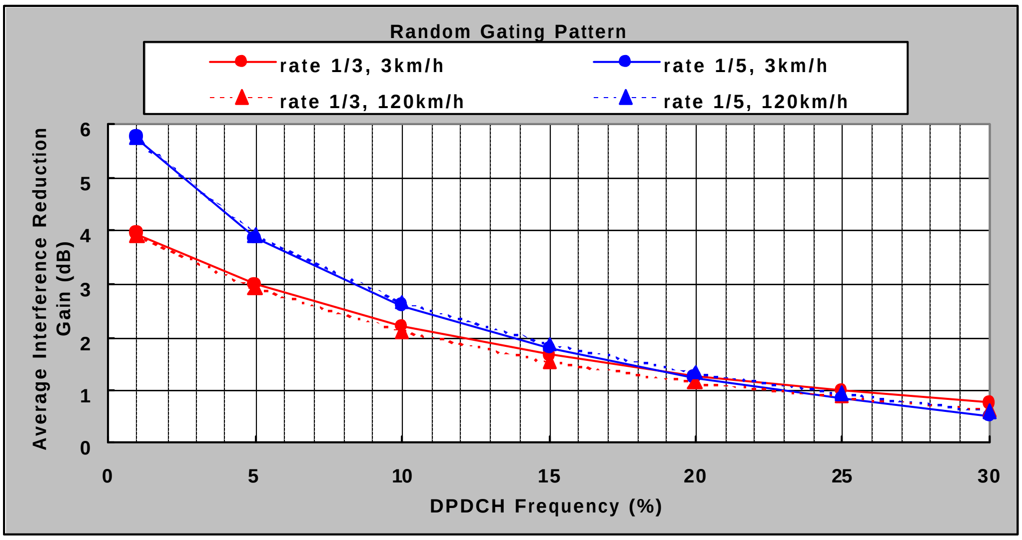

Figure 7. Average uplink interference reduction gain

8.1.1.3 Conclusion

From the simulation and analysis results, the uplink interference reduction gain is enough to use gated DPCCH transmission. If the DPDCH frequency is 10%, the interference reduction gain is about 2.5dB, and the gain increases as the DPDCH frequency decreases. Consequently, the gated DPCCH transmission is beneficial to the interference reduction, that is, the transmit power reduction.

8.1.2 UE Battery Life Enhancement [2]

8.1.2.1 Assumptions and models used in battery life calculations

8.1.2.1.1 Packet model

The same packet model was used as described in [3]. The Figure 8 shows the structure of the packet session, where:

Tp = average duration of one packet call.

Tcr_dch = connection release time for DCH only case.

Tcr_dsch = connection release time for DSCH+DCH case.

One interesting point here is that Tcr_dsch can be quite large, larger than Tcr_dch, which means that it can be so long the connection does not have to be released between each packet call. This is because DCH associated with DSCH could use quite high spreading factor, e.g. SF=256. However, it does not make any difference to the battery life calculations. Meaning , that if the simplified assumption is that gap between two packet calls is equal or larger than Tcr_dch or Tcr_dsch, then following model, explained below can be used in the battery life calculations.

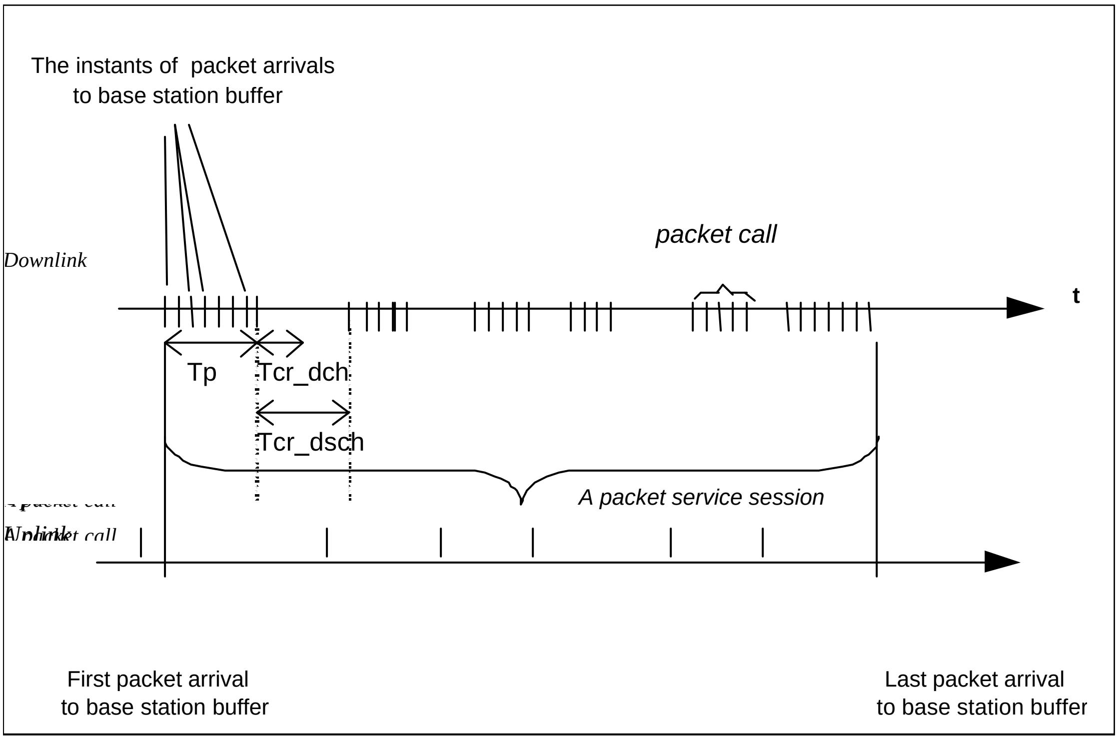

Figure 8. Packet model

Figure 9 shows the timing model, how the gating is assumed to be turned on in the battery calculations. Here Tgat_on is the time after the last packet when the gating is turned on . Note that Tgat_on should be larger than the time interval between individual packet bursts within Tp. Thus the percentage of time that the gating is on during the whole connection is

For DCH only case: $$DPCCH\_gating\_\% \; ? \; \frac{Tcr\_dch \; ? \; Tgat\_on}{Tp \; ? \; Tcr\_dch}$$

For DCH+DSCH case: $$DPCCH\_gating\_\% \; ? \; \frac{Tcr\_dsch \; ? \; Tgat\_on}{Tp \; ? \; Tcr\_dsch}$$

In [3], it was roughly calculated with these equations, that the percentage of time the DPCCH gating could be on, on average:

For DCH only case: DPCCH_gating_% = 0.30

For DCH+DSCH case: DPCCH_gating_% = 0.66

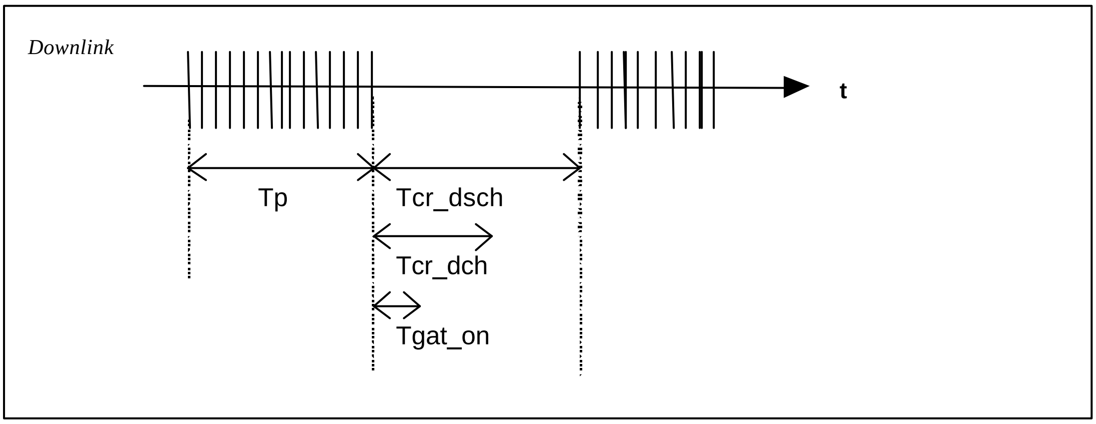

Figure 9. Timing for turning the gating on.

8.1.2.1.2 Assumptions in UE battery life calculations

Following assumptions were used in the simplified UE battery life calculations in [4].

1) First it was assumed what is the percentage of battery consumption of tx side and rx side, respectively, for certain tx power level, when gating is not used. Let's say that with tx power level , txpwr, this results in :

   - tx side consumes N1 mA @ txpwr
   - rx side consumes N2 mA @ txpwr

   No specific data rates were assumed here either in uplink or downlink, for simplification. This is because data rate change in downlink was assumed not to affect the battery consumption so much. The continuous decoding is needed anyway in downlink, since the packet transmission can assumed to restart in any frame and handover measurements are running continuously. If continuous decoding in every frame could be avoided, then we could assume clearly a different figure for rx side battery consumption during gating state, but until then, the same value N2, is assumed for rx side throughout the whole connection.

2) Then it was calculated , what is the tx side battery consumption , if tx gating is used. Separate values were calculated for 1/3 gating and 1/5 gating, with the same corresponding tx power level tx pwr. This resulted in following value:

   - tx side consumes N1_gating mA, during gating @ txpwr

3) Finally it was calculated what is the overall battery life improvement:

$$Battery\_life\_improvement = \frac{N1 + N2}{(1 - DPCCH\_gating\_\%) \cdot N1 + DPCCH\_gating\_\% \cdot N1\_gating + N2}$$

8.1.2.2 UE battery life improvement calculations

The battery life improvement calculations from [4] are repeated here once more , for clarification.

Table 8 and 9 show UE battery lifetime improvements for DCH and DCH+DSCH case, for medium range tx pwr level and high tx power level, respectively. Thus the only difference in calculating DCH case and DCH+DSCH case, is the value used for DPCCH_gating_% value.

Table 8. UE battery life improvement due to gating, with medium range tx power level.

	DPCCH_gating_%	Gating rate	UE battery life improvement
DCH	30 %	1/3	8 %
		1/5	13 %
DCH+DSCH	66 %	1/3	21 %
		1/5	34 %

Table 9. UE battery life improvement due to gating, with maximum tx power level.

	DPCCH_gating_%	Gating rate	UE battery life improvement
DCH	30 %	1/3	10 %
		1/5	16 %
DCH+DSCH	66 %	1/3	26 %
		1/5	44 %

The results show that DPCCH gating means clear UE battery life improvement in DCH+DSCH case. For DCH only case it is maybe not as sensible to utilise it.

8.1.2.3 Conclusion

With the help of DCH+DSCH concept, several packet calls in one packet session can be transmitted during the same connection without connection release between them, and without unnecessary usage of RACH between every packet call. With the help of DPCCH gating concept together with DCH+DSCH concept, we can offer the end user a very flexible and fast packet service in such way, that we do not sacrify the UE battery life too much.

If DPCCH gating would not be specified, the relative long periods (=end user's reading time) between each packet call, will consume UE batteries unnecessarily, which does not make much sense. However, it should be understood, that if operator wants to use long connection release times, he is allowed to do that, since there are no limitations anyway in the specifications, how long the connection release time can be.

8.1.3 References

[1] R1-00-1069, “Revised uplink interference reduction gain of gated DPCCH transmission”, Samsung

[2] R1-00-1029, “Clarification of UE battery life calculations”, Nokia

[3]R1-00-0686, “Discussion paper on DPCCH gating benefits”, Nokia

[4] R1-00-0856, “UE battery life improvement with DPCCH gating”, Nokia

9 Backward Compatibility

A UE based on Release 99 can be used in Release 2000 UTRAN with gated DPCCH transmission capability without any impact because the gating capability is negotiated during call-setup. Similarly, a UE based on Release 2000 with gated DPCCH transmission capability can be used in Release 99 UTRAN without any impact by the same reason. Consequently, the backward compatibility is guaranteed with gated DPCCH transmission in Release 2000.

History

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Tel. : +82-31-779-6624 Fax: +82-31-779-8003 Email : choihk@telecom.samsung.co.kr		
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