### RP-000340

# TSG-RAN Meeting #9 Hawaii, U.S.A. , 20-22 September 2000

Title: Agreed CRs to TS 25.211

Source: TSG-RAN WG1

Agenda item: 5.1.3

No.	R1 T-doc	Spec	CR	Rev	Subject	Cat	Current	New
1	R1-000897	25.211	065	-	Correction of reference	F	3.3.0	3.4.0
2	R1-001047	25.211	066	4	Clarification of paging indicator mapping	F	3.3.0	3.4.0
3	R1-000924	25.211	068	-	Editorial modification of the 25.211 about the CD/CA-ICH	D	3.3.0	3.4.0
4	R1-001091	25.211	070	1	Support of closed loop transmit diversity modes	F	3.3.0	3.4.0
5	R1-001098	25.211	071	-	DPCH initialisation procedure	F	3.3.0	3.4.0
6	R1-001173	25.211	072	3	Correction on indicators	F	3.3.0	3.4.0
7	R1-001048	25.211	074	-	Correction of STTD for DPCH	F	3.3.0	3.4.0
8	R1-001049	25.211	075	-	Clarification of first significant path	F	3.3.0	3.4.0
9	R1-001080	25.211	076	-	Clarification of SCH transmitted by TSTD	F	3.3.0	3.4.0
10	R1-001092	25.211	077	1	Clarification of FBI field	F	3.3.0	3.4.0

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# 2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- [1] 3G TS 25.201: "Physical layer general description".
- [2] 3G TS 25.211: "Physical channels and mapping of transport channels onto physical channels (FDD)".
- [3] 3G TS 25.212: "Multiplexing and channel coding (FDD)".
- [4] 3G TS 25.213: "Spreading and modulation (FDD)".
- [5] 3G TS 25.214: "Physical layer procedures (FDD)".
- [6] 3G TS 25.221: "Transport channels and physical channels (TDD)".
- [7] 3G TS 25.222: "Multiplexing and channel coding (TDD)".
- [8] 3G TS 25.223: "Spreading and modulation (TDD)".
- [9] 3G TS 25.224: "Physical layer procedures (TDD)".
- [10] 3G TS 25.231215: "Physical layer Measurements (FDD)".
- [11] 3G TS 25.301: "Radio Interface Protocol Architecture".
- [12] 3G TS 25.302: "Services Provided by the Physical Layer".
- [13] 3G TS 25.401: "UTRAN Overall Description".

# 3GPP TSG RAN Meeting #9

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# 3 Abbreviations

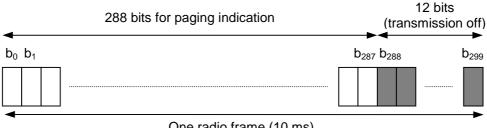
For the purposes of the present document, the following abbreviations apply:

AI	Acquisition Indicator
AICH	Acquisition Indicator Channel
AP	Access Preamble
AP-AICH	Access Preamble Acquisition Indicator Channel
API	Access Preamble Indicator Broadcast Channel
BCH	
CA	Channel Assignment Indicator
CAI	Channel Assignment Indicator CPCH Control Command
CCC	
CCPCH CCTrCU	Common Control Physical Channel
CCTrCH CD	Coded Composite Transport Channel
CD/CA-ICH	Collision Detection
CD/CA-ICH CDI	Collision Detection/Channel Assignment Indicator Channel Collision Detection Indicator
CPCH	Common Packet Channel
CPICH	Common Pilot Channel
CSICH	CPCH Status Indicator Channel
DCH	Dedicated Channel
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
DPDCH	Dedicated Physical Data Channel
DSCH	Downlink Shared Channel
DSMA-CD	Digital Sense Multiple Access - Collison Detection
DTX	Discontinuous Transmission
FACH	Forward Access Channel
FBI	Feedback Information
FSW	Frame Synchronization Word
ICH	Indicator Channel
MUI	Mobile User Identifier
PCH	Paging Channel
P-CCPCH	Primary Common Control Physical Channel
PCPCH	Physical Common Packet Channel
PDSCH	Physical Downlink Shared Channel
<del>PI</del>	- Page Indicator
PICH	Page Indicator Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
RNC	Radio Network Controller
S-CCPCH	Secondary Common Control Physical Channel
SCH	Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
SI	Status Indicator
SSC	Secondary Synchronisation Code
STTD	Space Time Transmit Diversity
TFCI	Transport Format Combination Indicator
TSTD	Time Switched Transmit Diversity
TPC	Transmit Power Control
UE LITRAN	User Equipment
UTRAN	UMTS Terrestrial Radio Access Network

#### 5.3.3.9 Paging Indicator Channel (PICH)

The Paging Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the pPaging iIndicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.

Figure 24 illustrates the frame structure of the PICH. One PICH radio frame of length 10 ms consists of 300 bits ( $b_0$ ,  $b_1$ , ...,  $b_{299}$ ). Of these, 288 bits ( $b_0$ ,  $b_1$ , ...,  $b_{287}$ ) are used to carry pPaging indicators. The remaining 12 bits are not formally part of the PICH and shall not be transmitted. The part of the frame with no transmission is reserved for possible future use.



One radio frame (10 ms)

#### Figure 24: Structure of Paging Indicator Channel (PICH)

In each PICH frame, Np pPaging iIndicators {PI<sub>0</sub>, ..., PI<sub>Np-1</sub>} are transmitted in each PICH frame, where Np=18, 36, 72, or 144

The PI calculated by higher layers for use for a certain UE, is <u>associated mapped</u> to the paging indicator  $PI_{pq}$ , where gpis computed as a function of the PI computed by higher layers, the SFN of the P-CCPCH radio frame during which the start of the PICH radio frame occurs, and the number of paging indicators per frame (Np):

$$p = \left(PI + \left\lfloor \left( \left(18 \times \left(SFN + \lfloor SFN / 8 \rfloor + \lfloor SFN / 64 \rfloor + \lfloor SFN / 512 \rfloor\right)\right) \mod 144 \right) \times \frac{N}{144} \right\rfloor \right) \mod N$$

$$q = \left(PI + \left\lfloor \left( \left(18 \times \left(SFN + \lfloor SFN / 8 \rfloor + \lfloor SFN / 64 \rfloor + \lfloor SFN / 512 \rfloor\right)\right) \mod 144 \right) \times \frac{Np}{144} \right\rfloor \right) \mod Np$$

Further, the PI calculated by higher layers is associated with the value of the paging indicator  $P_a$ . If a paging indicator in a certain frame is set to "1" it is an indication that UEs associated with this paging indicator and PI should read the corresponding frame of the associated S-CCPCH.

The PI bitmap in the PCH data frames over Iub contains indication values for all higher layer PI values possible. Each bit in the bitmap indicates if the paging indicator associated with that particular PI shall be set to 0 or 1. Hence, the calculation in the formula above is to be performed in Node B to make the association between PI and  $P_{q_2}$ 

The mapping from  $\{PI_0, ..., PI_{Np-1}\}$  to the PICH bits  $\{b_0, ..., b_{287}\}$  are according to table 22.

#### Table 22: Mapping of Ppaging lindicators Pq(PI) to PICH bits

Number of <u>paging indicators</u> PI per frame (Np)	Pł <sub>pg</sub> = 1	Pl <sub>pg</sub> = 0
N <u>p</u> =18	${b_{16gp},, b_{16gp+15}} = {-1, -1,, -1}$	${b_{16qp},, b_{16qp+15}} = {+1,+1,,+1}$
N <u>p</u> =36	$\{b_{8qp}, \dots, b_{8qp+7}\} = \{-1, -1, \dots, -1\}$	$\{b_{8qp}, \ldots, b_{8qp+7}\} = \{+1, +1, \ldots, +1\}$
N <u>p</u> =72	${b_{4gp}, \ldots, b_{4gp+3}} = {-1, -1, \ldots, -1}$	${b_{4gp},, b_{4gp+3}} = {+1, +1,, +1}$
N <u>p</u> =144	$\{b_{2qp}, b_{2qp+1}\} = \{-1, -1\}$	$\{b_{2qp}, b_{2qp+1}\} = \{+1, +1\}$

If a Paging Indicator in a certain frame is set to "1" it is an indication that UEs associated with this Paging Indicator should read the corresponding frame of the associated S CCPCH.

When transmit diversity is employed for the PICH, STTD encoding is used on the PICH bits as described in subclause 5.3.1.1.1.

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 $\tau_{p-a} = 12800$  chips

 $\tau_{p-m} = 20480$  chips (4 access slots)

The parameter AICH\_Transmission\_Timing is signalled by higher layers.

# 7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE  $\tau_{p-a1}$  chips prior to the reception of downlink access slot number n, n =0, 1, ...,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-ICH\_CD/CA-ICH is identical to RACH Preamble and AICH. The timing relationship between CD-ICH\_CD/CA-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The  $T_{cpch}$  timing parameter is identical to the PRACH/AICH transmission timing parameter. When  $T_{cpch}$  is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-ICHCD/CA-ICH.

 $\tau_{p-p}$  = Time to next available access slot, between Access Preambles.

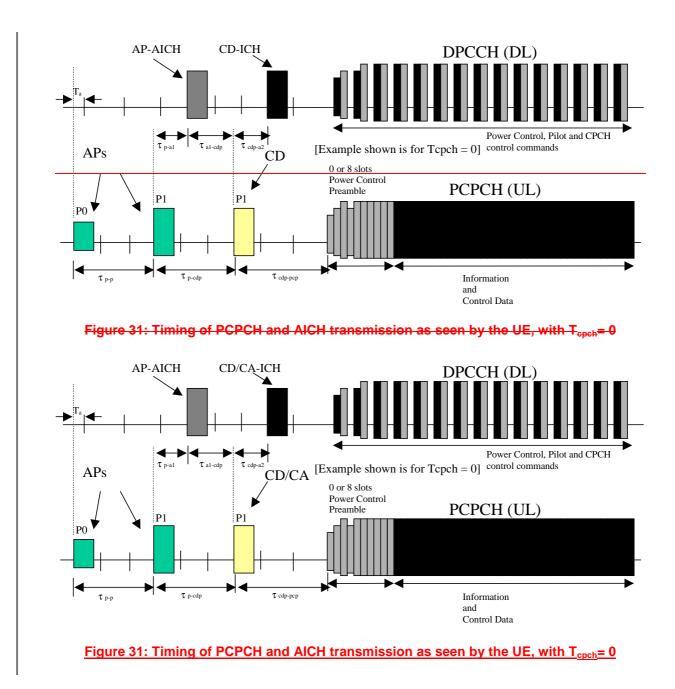
Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

- Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.
- $\tau_{p-a1} =$  Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T<sub>cpch</sub>
- $\tau_{a1-cdp} =$  Time between receipt of AP-AICH and transmission of the CD Preamble  $\tau_{a1-cdp}$  has a minimum value of  $\tau_{a1-cdp, min} = 7680$  chips.
- $\tau_{p-cdp} = Time between the last AP and CD Preamble. <math>\tau_{p-cdp}$  has a minimum value of  $\tau_{p-cdp-min}$  which is either 3 or 4 access slots, depending on  $T_{cpch}$
- $\tau_{cdp-a2} = Time between the CD Preamble and the CD-ICHCD/CA-ICH has two alternative values: 7680 chips or 12800 chips, depending on T<sub>cpch</sub>$
- $\tau_{cdp-pcp}$  = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on  $T_{cpch}$ .

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 31 illustrates the PCPCH/AICH timing relationship when  $T_{cpch}$  is set to 0 and all access slot subchannels are available for PCPCH.



# 7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 32.

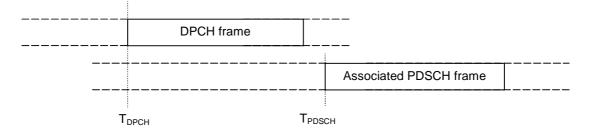


Figure 32: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted  $T_{DPCH}$  and the start of the associated PDSCH frame is denoted  $T_{PDSCH}$ . Any DPCH frame is associated to one PDSCH frame through the relation 46080 chips  $\leq T_{PDSCH} - T_{DPCH} < 84480$  chips, i.e. the associated PDSCH frame starts anywhere between three slot after the end of the DPCH frame up to 18 slots behind the end of the DPCH frame.

# 7.6 DPCCH/DPDCH timing relations

# 7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

# 7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

# 7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately  $T_0$  chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame.  $T_0$  is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of  $T_0$  can be found in [5].

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#### 5.3.1 Downlink transmit diversity

Table 10 summarizes the possible application of open and closed loop transmit diversity modes on different downlink physical channel types. Simultaneous use of STTD and closed loop modes on the same physical channel is not allowed. In addition, if Tx diversity is applied on any of the downlink physical channels it shall also be applied on P-CCPCH and SCH. Regarding CPICH transmission in case of transmit diversity, see subclause 5.3.3.1.

Furthermore, the transmit diversity mode used for a PDSCH frame shall be the same as the transmit diversity mode used for the DPCH associated with this PDSCH frame. During the duration of the PDSCH frame, and within the slot prior to the PDSCH frame, the transmit diversity mode (open loop or closed loop) on the associated DPCH may not change. However, changing from closed loop mode 1 to mode 2 or vice versa, is allowed.

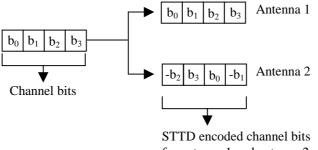
Table 10: Application of Tx diversity modes on downlink physical channel types
"X" – can be applied, "–" – not applied

Physical channel type	Open lo	Closed loop	
	TSTD	STTD	Mode
P-CCPCH	-	Х	-
SCH	Х	-	_
S-CCPCH	-	Х	-
DPCH	-	Х	Х
PICH	-	Х	-
PDSCH	-	Х	Х
AICH	_	Х	_
CSICH	-	Х	_

#### 5.3.1.1 Open loop transmit diversity

#### 5.3.1.1.1 Space time block coding based transmit antenna diversity (STTD)

The open loop downlink transmit diversity employs a space time block coding based transmit diversity (STTD). The STTD encoding is optional in UTRAN. STTD support is mandatory at the UE. STTD encoding is applied on blocks of 4 consecutive channel bits. A block diagram of a generic STTD encoder for channel bits  $b_0$ ,  $b_1$ ,  $b_2$ ,  $b_3$  is shown in the figure 8 below. Channel coding, rate matching and interleaving is done as in the non-diversity mode. The bit  $b_i$  is real valued {0} for DTX bits and {1, -1} for all other channel bits.



for antenna 1 and antenna 2.

#### Figure 8: Generic block diagram of the STTD encoder

5.3.1.1.2 Time Switched Transmit Diversity for SCH (TSTD)

Transmit diversity, in the form of Time Switched Transmit Diversity (TSTD), can be applied to the SCH. TSTD for the SCH is optional in UTRAN, while TSTD support is mandatory in the UE. TSTD for the SCH is described in subclause 5.3.3.4.1.

### 5.3.1.2 Closed loop transmit diversity

Closed loop transmit diversity is described in [5]. <u>The support of both closed loop transmit diversity</u> <u>modes is optional in UTRAN and mandatory at the UE</u> Both closed loop transmit diversity modes shall be supported at the UE and may be supported in the UTRAN.

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# 5.2 Uplink physical channels

### 5.2.1 Dedicated uplink physical channels

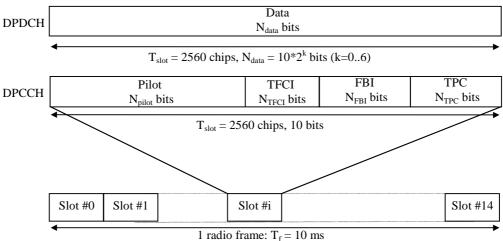
There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry the DCH transport channel. There may be zero, one, or several uplink DPDCHs on each radio link.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous transport format combination of the transport channels mapped to the simultaneously transmitted uplink DPDCH radio frame. There is one and only one uplink DPCCH on each radio link.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each radio frame of length 10 ms is split into 15 slots, each of length  $T_{slot} = 2560$  chips, corresponding to one power-control period.



1 radio frame.  $\Gamma_f = 10 \text{ ms}$ 

Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH slot. It is related to the spreading factor SF of the DPDCH as  $SF = 256/2^k$ . The DPDCH spreading factor may range from 256 down to 4. The spreading factor of the uplink DPCCH is always equal to 256, i.e. there are 10 bits per uplink DPCCH slot.

The exact number of bits of the uplink DPDCH and the different uplink DPCCH fields ( $N_{pilot}$ ,  $N_{TFCI}$ ,  $N_{FBI}$ , and  $N_{TPC}$ ) is given by table 1 and table 2. What slot format to use is configured by higher layers and can also be reconfigured by higher layers.

The channel bit and symbol rates given in table 1 and table 2 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The FBI bits are used to support techniques requiring feedback from the UE to the UTRAN Access Point, including closed loop mode transmit diversity and site selection diversity transmission (SSDT). The structure of the FBI field is shown in figure 2 and described below.

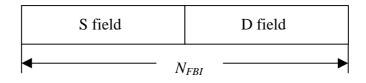


Figure 2: Details of FBI field

The S field is used for SSDT signalling, while the D field is used for closed loop mode transmit diversity signalling. The S field consists of 0, 1 or 2 bits. The D field consists of 0 or 1 bit. The total FBI field size  $N_{FBI}$  is given by table 2. Simultaneous use of SSDT power control and closed loop mode transmit diversity requires that the S field consists of 1 bit. The use of the FBI fields is described in detail in [5].

Table	1: D	PDCH	fields
-------	------	------	--------

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N <sub>data</sub>
0	15	15	256	150	10	10
1	30	30	128	300	20	20
2	60	60	64	600	40	40
3	120	120	32	1200	80	80
4	240	240	16	2400	160	160
5	480	480	8	4800	320	320
6	960	960	4	9600	640	640

There are two types of uplink dedicated physical channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 2. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the uplink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, DPCCH slot formats with TFCI fields are changed. There are two possible compressed slot formats for each normal slot format. They are labelled A and B and the selection between them is dependent on the number of slots that are transmitted in each frame in compressed mode.

Slot Form at #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N <sub>pilot</sub>	N <sub>TPC</sub>	NTFCI	N <sub>FBI</sub>	Transmitted slots per radio frame
0	15	15	256	150	10	6	2	2	0	15
0A	15	15	256	150	10	5	2	3	0	10-14
0B	15	15	256	150	10	4	2	4	0	8-9
1	15	15	256	150	10	8	2	0	0	8-15
2	15	15	256	150	10	5	2	2	1	15
2A	15	15	256	150	10	4	2	3	1	10-14
2B	15	15	256	150	10	3	2	4	1	8-9
3	15	15	256	150	10	7	2	0	1	8-15
4	15	15	256	150	10	6	2	0	2	8-15
5	15	15	256	150	10	5	1	2	2	15
5A	15	15	256	150	10	4	1	3	2	10-14
5B	15	15	256	150	10	3	1	4	2	8-9

#### Table 2: DPCCH fields

The pilot bit patterns are described in table 3 and table 4. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "1".)

	Ν	pilot =	3		Npilo	<sub>t</sub> = 4			Ν	pilot =	5				N <sub>pilo</sub>	<sub>t</sub> = 6		
Bit #	0	1	2	0	1	2	3	0	1	2	3	4	0	1	2	3	4	5
Slot #0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
1	0	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1	1	0
2	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
3	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0
4	1	0	1	1	1	0	1	1	0	1	0	1	1	1	0	1	0	1
5	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
6	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0
7	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
8	0	1	1	1	0	1	1	0	1	1	1	0	1	0	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
11	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1
12	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
13	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1
14	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1

Table 3: Pilot bit patterns for uplink DPCCH with  $N_{pilot}$  = 3, 4, 5 and 6

			Ν	pilot =	7						Npilo	<sub>t</sub> = 8			
Bit #	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7
Slot #0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
1	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0
2	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
3	1	0	0	1	0	0	1	1	0	1	0	1	0	1	0
4	1	1	0	1	0	1	1	1	1	1	0	1	0	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
6	1	1	1	1	0	0	1	1	1	1	1	1	0	1	0
7	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
8	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
11	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
13	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1
14	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1

The relationship between the TPC bit pattern and transmitter power control command is presented in table 5.

Table	5: TP	C Bit	Pattern
-------	-------	-------	---------

TPC Bit	Pattern	Transmitter power
N <sub>TPC</sub> = 1	N <sub>TPC</sub> = 2	control command
1	11	1
0	00	0

Multi-code operation is possible for the uplink dedicated physical channels. When multi-code transmission is used, several parallel DPDCH are transmitted using different channelization codes, see [4]. However, there is only one DPCCH per radio link.

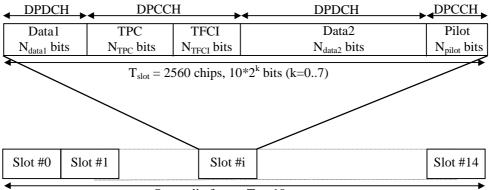
A power control preamble may be used for initialisation of a DCH. Both the UL and DL DPCCHs shall be transmitted during the power control preamble. The length of the power control preamble is a UE-specific higher layer parameter,  $N_{pcp}$  (see [5], section 5.1.2.4), signalled by the network. The UL DPCCH shall take the same slot format in the power control preamble as afterwards, as given in table 2. When,  $N_{pcp} > 0$  the pilot patterns from slot #(15-  $N_{pcp}$ ) to slot #14 of table 3 and table 4 shall be used. The timing of the power control preamble is shown in Figure 33described in [5], subclause 4.3.2.27.7. The TFCI field is filled with "1" bits.

# 5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare subclause 5.2.1.

Figure 9 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length  $T_{slot} = 2560$  chips, corresponding to one power-control period.



One radio frame,  $T_f = 10 \text{ ms}$ 



The parameter k in figure 9 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as  $SF = 512/2^k$ . The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields ( $N_{pilot}$ ,  $N_{TPC}$ ,  $N_{TFCI}$ ,  $N_{data1}$  and  $N_{data2}$ ) is given in table 11. What slot format to use is configured by higher layers and can also be reconfigured by higher layers.

There are basically two types of downlink Dedicated Physical Channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 11. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the downlink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, a different slot format is used compared to normal mode. There are two possible compressed slot formats that are labelled A and B. Format B is used for compressed mode by spreading factor reduction and format A is used for all other transmission time reduction methods. The channel bit and symbol rates given in table 11 are the rates immediately before spreading.

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate	SF	Bits/ Slot		DCH /Slot		PCCH its/Slo		Transmitted slots per radio frame
		(ksps)			N <sub>Data1</sub>	N <sub>Data2</sub>	N <sub>TPC</sub>	NTFCI	N <sub>Pilot</sub>	N <sub>Tr</sub>
0	15	7.5	512	10	0	4	2	0	4	15
0A	15	7.5	512	10	0	4	2	0	4	8-14
0B	30	15	256	20	0	8	4	0	8	8-14
1	15	7.5	512	10	0	2	2	2	4	15
1B	30	15	256	20	0	4	4	4	8	8-14
2	30	15	256	20	2	14	2	0	2	15
2A	30	15	256	20	2	14	2	0	2	8-14
2B	60	30	128	40	4	28	4	0	4	8-14
3	30	15	256	20	2	12	2	2	2	15
ЗA	30	15	256	20	2	10	2	4	2	8-14
3B	60	30	128	40	4	24	4	4	4	8-14
4	30	15	256	20	2	12	2	0	4	15
4A	30	15	256	20	2	12	2	0	4	8-14
4B	60	30	128	40	4	24	4	0	8	8-14
5	30	15	256	20	2	10	2	2	4	15
5A	30	15	256	20	2	8	2	4	4	8-14
5B	60	30	128	40	4	20	4	4	8	8-14
6	30	15	256	20	2	8	2	0	8	15
6A	30	15	256	20	2	8	2	0	8	8-14
6B	60	30	128	40	4	16	4	0	16	8-14
7	30	15	256	20	2	6	2	2	8	15
7A	30	15	256	20	2	4	2	4	8	8-14
7B	60	30	128	40	4	12	4	4	16	8-14
8	60	30	128	40	6	28	2	0	4	15
8A	60	30	128	40	6	28	2	0	4	8-14
8B	120	60	64	80	12	56	4	0	8	8-14
9	60	30	128	40	6	26	2	2	4	15
9A	60	30	128	40	6	24	2	4	4	8-14
9B	120	60	64	80	12	52	4	4	8	8-14
10	60	30	128	40	6	24	2	0	8	15
10A	60	30	128	40	6	24	2	0	8	8-14
10B	120	60	64	80	12	48	4	0	16	8-14
11	60	30	128	40	6	22	2	2	8	15
11A	60	30	128	40	6	20	2	4	8	8-14
11B	120	60	64	80	12	44	4	4	16	8-14
12	120	60	64	80	12	48	4	8*	8	15
12A	120	60	64	80	12	40	4	16*	8	8-14
12B	240	120	32	160	24	96	8	16*	16	8-14
13	240	120	32	160	28	112	4	8*	8	15
13A	240	120	32	160	28	104	4	16*	8	8-14
13B	480	240	16	320	56	224	8	16*	16	8-14
14	480	240	16	320	56	232	8	8*	16	15
14A	480	240	16	320	56	224	8	16*	16	8-14
14B	960	480	8	640	112	464	16	16*	32	8-14
15	960	480	8	640	120	488	8	8*	16	15
15A	960	480	8	640	120	480	8	16*	16	8-14
15B	1920	960	4	1280	240	976	16	16*	32	8-14
16	1920	960	4	1280	248	1000	8	8*	16	15
16A	1920	960	4	1280	248	992	8	16*	16	8-14

#### Table 11: DPDCH and DPCCH fields

\* If TFCI bits are not used, then DTX shall be used in TFCI field.

NOTE1: Compressed mode is only supported through spreading factor reduction for SF=512 with TFCI.

NOTE2: Compressed mode by spreading factor reduction is not supported for SF=4.

The pilot bit patterns are described in table 12. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "11".) In table 12, the transmission order is from left to right.

In downlink compressed mode through spreading factor reduction, the number of bits in the TPC and Pilot fields are doubled. Symbol repetition is used to fill up the fields. Denote the bits in one of these fields in normal mode by  $x_1, x_2, x_3, ..., x_X$ . In compressed mode the following bit sequence is sent in corresponding field:  $x_1, x_2, x_1, x_2, x_3, x_4, x_3, x_4, ..., x_X$ .

	N <sub>pilot</sub> = 2	N <sub>pilo</sub> (*		N <sub>pilot</sub> = 8 (*2)				N <sub>pilot</sub> = 16 (*3)							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	11	11	11	11	11	10	11	11	11	10	11	11	11	10
1	00	11	00	11	00	11	10	11	00	11	10	11	11	11	00
2	01	11	01	11	01	11	01	11	01	11	01	11	10	11	00
3	00	11	00	11	00	11	00	11	00	11	00	11	01	11	10
4	10	11	10	11	10	11	01	11	10	11	01	11	11	11	11
5	11	11	11	11	11	11	10	11	11	11	10	11	01	11	01
6	11	11	11	11	11	11	00	11	11	11	00	11	10	11	11
7	10	11	10	11	10	11	00	11	10	11	00	11	10	11	00
8	01	11	01	11	01	11	10	11	01	11	10	11	00	11	11
9	11	11	11	11	11	11	11	11	11	11	11	11	00	11	11
10	01	11	01	11	01	11	01	11	01	11	01	11	11	11	10
11	10	11	10	11	10	11	11	11	10	11	11	11	00	11	10
12	10	11	10	11	10	11	00	11	10	11	00	11	01	11	01
13	00	11	00	11	00	11	11	11	00	11	11	11	00	11	00
14	00	11	00	11	00	11	11	11	00	11	11	11	10	11	01

Table 12: Pilot bit patterns for downlink DPCCH with  $N_{pilot}$  = 2, 4, 8 and 16

NOTE \*1: This pattern is used except slot formats 2B and 3B.

NOTE \*2: This pattern is used except slot formats 0B, 1B, 4B, 5B, 8B, and 9B.

NOTE \*3: This pattern is used except slot formats 6B, 7B, 10B, 11B, 12B, and 13B.

NOTE: For slot format *n*B where n = 0, ..., 15, the pilot bit pattern corresponding to N<sub>pilot</sub>/2 is to be used and symbol repetition shall be applied.

The relationship between the TPC symbol and the transmitter power control command is presented in table 13.

	TPC Bit Pattern							
$N_{TPC} = 2$	$N_{TPC} = 4$	N <sub>TPC</sub> = 8	control command					
11	1111	11111111	1					
00	0000	00000000	0					

#### Table 13: TPC Bit Pattern

Multicode transmission may be employed in the downlink, i.e. the CCTrCH (see [3]) is mapped onto several parallel downlink DPCHs using the same spreading factor. In this case, the Layer 1 control information is transmitted only on the first downlink DPCH. DTX bits are transmitted during the corresponding time period for the additional downlink DPCHs, see figure 10.

In case there are several CCTrCHs mapped to different DPCHs transmitted to the same UE different spreading factors can be used on DPCHs to which different CCTrCHs are mapped. Also in this case, Layer 1 control information is only transmitted on the first DPCH while DTX bits are transmitted during the corresponding time period for the additional DPCHs.

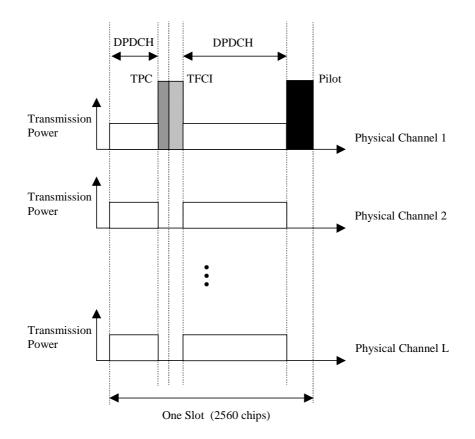


Figure 10: Downlink slot format in case of multi-code transmission

A power control preamble may be used for initialisation of a DCH. The DL DPCH shall take the same slot format in the power control preamble as afterwards, as given in Table 11, with the restriction that DTX shall be used in the DL DPDCH fields in the power control preamble. The length of the power control preamble is a UE-specific higher-layer parameter,  $N_{pcp}$  (see [5], section 5.1.2.47.7), signalled by the network. When  $N_{pcp} > 0$ , the pilot patterns from slot #(15 –  $N_{pcp}$ ) to slot #14 of table 12 shall be used. The TFCI field is filled with "1" bits.

#### 5.3.2.1 STTD for DPCH

The pilot bit pattern for the DPCH channel transmitted on antenna 2 is given in table 14.

- For N<sub>pilot</sub> = 8, 16 the shadowed part indicates pilot bits that are obtained by STTD encoding the corresponding (shadowed) bits in Table 12. The non-shadowed pilot bit pattern is orthogonal to the corresponding (non-shadowed) pilot bit pattern in table 12.
- For  $N_{pilot} = 4$ , the diversity antenna pilot bit pattern is obtained by STTD encoding both the shadowed and non-shadowed pilot bits in table 12.
- For  $N_{pilot} = 2$ , the diversity antenna pilot pattern is obtained by STTD encoding the two pilot bits in table 12 with the last two bits (data or DTX) of the second data field (data2) of the slot. Thus for  $N_{pilot} = 2$  case, the last two bits of the second data field (data 2) after STTD encoding, follow the diversity antenna pilot bits in Table 14.

STTD encoding for the DPDCH, TPC, and TFCI fields is done as described in subclause 5.3.1.1.1. For the SF=512 DPCH, the first two bits in each slot, i.e. TPC bits, are not STTD encoded and the same bits are transmitted with equal power from the two antennas. The remaining four bits are STTD encoded.

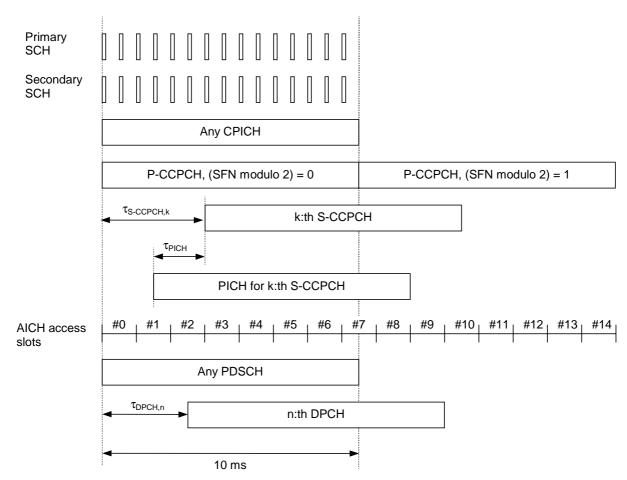
For compressed mode through spreading factor reduction and for  $N_{pilot} > 4$ , symbol repetition shall be applied to the pilot bit patterns of table 14, in the same manner as described in 5.3.2. For slot formats 2B and 3B, i.e. compressed mode through spreading factor reduction and  $N_{pilot} = 4$ , the pilot bits on antenna 1 are STTD encoded, and thus the pilot bit pattern is as shown in the most right set of table 14.

# 7 Timing relationship between physical channels

# 7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 28 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Transmission timing for uplink physical channels is given by the received timing of downlink physical channels, as described in the following subclauses.



#### Figure 28: Frame timing and access slot timing of downlink physical channels

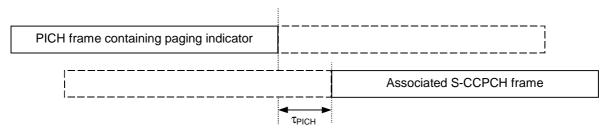
The following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e.  $\tau_{S-CCPCH,k} = T_k \times 256$  chip,  $T_k \in \{0, 1, ..., 149\}$ .
- The PICH timing is  $\tau_{\text{PICH}} = 7680$  chips prior to its corresponding S-CCPCH frame timing, i.e. the timing of the S-CCPCH carrying the PCH transport channel with the corresponding paging information, see also subclause 7.2.
- AICH access slots #0 starts the same time as P-CCPCH frames with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in subclauses 7.3 and 7.4 respectively.

- The relative timing of associated PDSCH and DPCH is described in subclause 7.5.
- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e.  $\tau_{DPCH,n} = T_n \times 256$  chip,  $T_n \in \{0, 1, ..., 149\}$ . The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in subclause 7.6.

# 7.2 PICH/S-CCPCH timing relation

Figure 29 illustrates the timing between a PICH frame and its associated S-CCPCH frame, i.e. the S-CCPCH frame that carries the paging information related to the paging indicators in the PICH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting  $\tau_{PICH}$  chips after the transmitted PICH frame.  $\tau_{PICH}$  is defined in subclause 7.1.





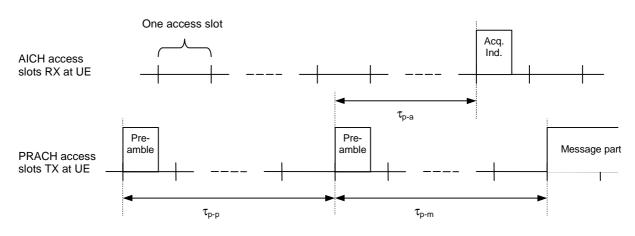
# 7.3 PRACH/AICH timing relation

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in subclause 7.1.

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number *n* is transmitted from the UE  $\tau_{p-a}$  chips prior to the reception of downlink access slot number *n*, *n* = 0, 1, ..., 14.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure 30.





The preamble-to-preamble distance  $\tau_{p\text{-}p}$  shall be larger than or equal to the minimum preamble-to-preamble distance  $\tau_{p\text{-}p,min}$ , i.e.  $\tau_{p\text{-}p} \ge \tau_{p\text{-}p,min}$ .

In addition to  $\tau_{p-p,min}$ , the preamble-to-AI distance  $\tau_{p-a}$  and preamble-to-message distance  $\tau_{p-m}$  are defined as follows:

- when AICH\_Transmission\_Timing is set to 0, then

 $\tau_{p-p,min} = 15360$  chips (3 access slots)

 $\tau_{p-a} = 7680$  chips

 $\tau_{p-m} = 15360$  chips (3 access slots)

- when AICH\_Transmission\_Timing is set to 1, then

 $\tau_{p-p,min} = 20480$  chips (4 access slots)

 $\tau_{p-a} = 12800$  chips

 $\tau_{p-m} = 20480$  chips (4 access slots)

The parameter AICH\_Transmission\_Timing is signalled by higher layers.

# 7.4 PCPCH/AICH timing relation

The uplink PCPCH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE  $\tau_{p-a1}$  chips prior to the reception of downlink access slot number n, n =0, 1, ...,14.

The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-ICH is identical to RACH Preamble and AICH. The timing relationship between CD-ICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The  $T_{cpch}$  timing parameter is identical to the PRACH/AICH transmission timing parameter. When  $T_{cpch}$  is set to zero or one, the following PCPCH/AICH timing values apply.

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-ICH.

 $\tau_{p-p}$  = Time to next available access slot, between Access Preambles.

Minimum time = 15360 chips + 5120 chips X Tcpch

Maximum time = 5120 chips X 12 = 61440 chips

- Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.
- $\tau_{p-a1} =$  Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T<sub>cpch</sub>
- $\tau_{a1-cdp} =$  Time between receipt of AP-AICH and transmission of the CD Preamble  $\tau_{a1-cdp}$  has a minimum value of  $\tau_{a1-cdp, min} = 7680$  chips.
- $\tau_{p-cdp} = Time between the last AP and CD Preamble. <math>\tau_{p-cdp}$  has a minimum value of  $\tau_{p-cdp-min}$  which is either 3 or 4 access slots, depending on  $T_{cpch}$
- $\tau_{cdp-a2}$  = Time between the CD Preamble and the CD-ICH has two alternative values: 7680 chips or 12800 chips, depending on  $T_{cpch}$
- $\tau_{cdp-pcp}$  = Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on  $T_{cpch}$ .

The message transmission shall start 0 or 8 slots after the start of the power control preamble depending on the length of the power control preamble.

Figure 31 illustrates the PCPCH/AICH timing relationship when  $T_{cpch}$  is set to 0 and all access slot subchannels are available for PCPCH.

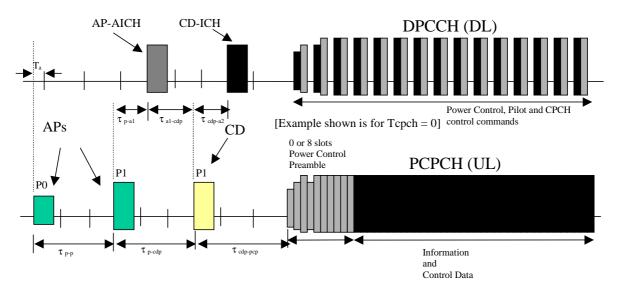
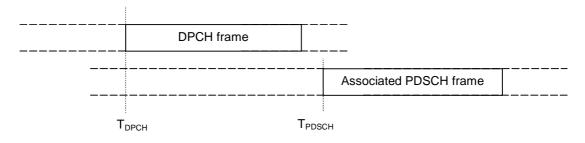


Figure 31: Timing of PCPCH and AICH transmission as seen by the UE, with  $T_{cpch}=0$ 

# 7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 32.



#### Figure 32: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted  $T_{DPCH}$  and the start of the associated PDSCH frame is denoted  $T_{PDSCH}$ . Any DPCH frame is associated to one PDSCH frame through the relation 46080 chips  $\leq T_{PDSCH} - T_{DPCH} < 84480$  chips, i.e. the associated PDSCH frame starts anywhere between three slot after the end of the DPCH frame up to 18 slots behind the end of the DPCH frame.

# 7.6 DPCCH/DPDCH timing relations

### 7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

### 7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

# 7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately  $T_0$  chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame.  $T_0$  is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of  $T_0$  can be found in [5].

# 7.7 Timing relations for initialisation of channels

Figure 33 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be  $T_{B-min} = 38400$  chips (i.e.15 slots).

The downlink DPCCH shall commence at a time  $T_B$  after the end of the relevant FACH frame, where  $T_B \ge T_{B-min}$  according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset_{-1}} \times 38400 \text{ chips , where:}$$

 $N_{pcp}$  is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], subclause 5.1.2.4).

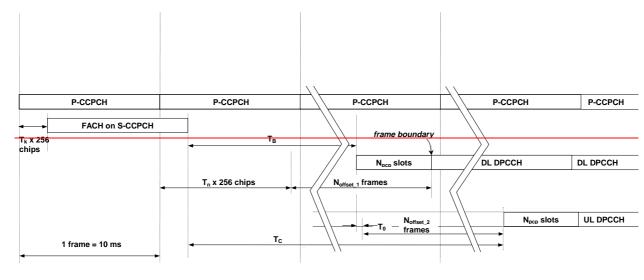
 $N_{offset_1}$  is a parameter set by higher layers and derived from the activation time if one is specified. In order that  $T_B \ge T_{B_-}$ min,  $N_{offset_1}$  shall be an integer number of frames such that:

$$N_{offset_1} \ge \begin{cases} 1 \text{ when } T_n - T_k \ge \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 2 \text{ when } \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \le T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 3 \text{ when } T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

 $T_{h}$  and  $T_{k}$  are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see subclause 7.1). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T<sub>C</sub> after the end of the relevant FACH frame, where

 $T_C = T_B + T_0 + N_{offset_2} \times 38400$  chips, where  $T_0$  is as in subclause 7.6.3. If an activation time for the uplink DPCCH is specified, then  $N_{offset_2}$  shall be set to zero. Otherwise the stating time of the uplink DPCCH shall be determined by higher layers according to the procedure in TS 25.214 sub clause 4.3.2, subject to the constraint that  $N_{offset_2}$  shall be an integer number of frames greater than or equal to zero.



#### Figure 33: Timing for initialisation of DCH.

The data channels shall not commence before the end of the power control preamble.

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#### 4.1.1.1 DCH - Dedicated Channel

The Dedicated Channel (DCH) is a downlink or uplink transport channel. The DCH is transmitted over the entire cell or over only a part of the cell using e.g. beam-forming antennas.

### 4.1.2 Common transport channels

There are six types of common transport channels: BCH, FACH, PCH, RACH, CPCH and DSCH.

#### 4.1.2.1 BCH - Broadcast Channel

The Broadcast Channel (BCH) is a downlink transport channel that is used to broadcast system- and cell-specific information. The BCH is always transmitted over the entire cell and has a single transport format.

### 4.1.2.2 FACH - Forward Access Channel

The Forward Access Channel (FACH) is a downlink transport channel. The FACH is transmitted over the entire cell or over only a part of the cell using e.g. beam-forming antennas. The FACH can be transmitted using slow power control.

#### 4.1.2.3 PCH - Paging Channel

The Paging Channel (PCH) is a downlink transport channel. The PCH is always transmitted over the entire cell. The transmission of the PCH is associated with the transmission of physical-layer generated Paging Indicators, to support efficient sleep-mode procedures.

#### 4.1.2.4 RACH - Random Access Channel

The Random Access Channel (RACH) is an uplink transport channel. The RACH is always received from the entire cell. The RACH is characterized by a collision risk and by being transmitted using open loop power control.

#### 4.1.2.5 CPCH - Common Packet Channel

The Common Packet Channel (CPCH) is an uplink transport channel. CPCH is associated with a dedicated channel on the downlink which provides power control and CPCH Control Commands (e.g. Emergency Stop) for the uplink CPCH. The CPCH is characterised by initial collision risk and by being transmitted using inner loop power control.

#### 4.1.2.6 DSCH - Downlink Shared Channel

The Downlink Shared Channel (DSCH) is a downlink transport channel shared by several UEs The DSCH is associated with one or several downlink DCH. The DSCH is transmitted over the entire cell or over only a part of the cell using e.g. beam-forming antennas.

# 4.2 Indicators

Indicators are means of fast low-level signalling entities which are transmitted without using information blocks sent over transport channels. The meaning of indicators is <u>implicit to the receiverspecific to the type of indicator</u>.

The indicators defined in the current version of the specifications are: Acquisition Indicator (AI), Access Preamble Indicator (API), Channel Assignment Indicator (CAI), Collision Detection Indicator (CDI), Page Indicator (PI) and Status Indicator (SI).

Indicators may be either boolean (two-valued) or three-valued. Their mapping to indicator channels is channel specific.

Indicators are transmitted on those physical channels that are indicator channels (ICH).

In case of TFCI based signalling, the TFCI informs the UE of the instantaneous transport format parameters related to the PDSCH as well as the channelisation code of the PDSCH.

In the other case, the information is given by higher layer signalling.

The channel bit rates and symbol rates for PDSCH are given in table 19.

For PDSCH the allowed spreading factors may vary from 256 to 4.

Slot format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	Ndata
0	30	15	256	300	20	20
1	60	30	128	600	40	40
2	120	60	64	1200	80	80
3	240	120	32	2400	160	160
4	480	240	16	4800	320	320
5	960	480	8	9600	640	640
6	1920	960	4	19200	1280	1280

#### Table 19: PDSCH fields

When open loop transmit diversity is employed for the PDSCH, STTD encoding is used on the data bits as described in subclause 5.3.1.1.1.

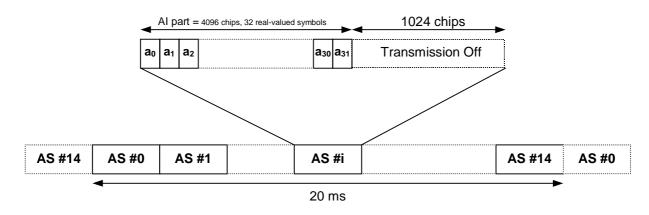
#### 5.3.3.6 Acquisition Indicator Channel (AICH)

The Acquisition Indicator channel (AICH) is a fixed rate (SF=256) physical channel used to carry Acquisition Indicators (AI). Acquisition Indicator  $AI_s$  corresponds to signature s on the PRACH.

Figure 21 illustrates the structure of the AICH. The AICH consists of a repeated sequence of 15 consecutive *access slots* (AS), each of length 5120 chips. Each access slot consists of two parts, an *Acquisition-Indicator* (AI) part consisting of 32 real-valued symbols  $a_0, ..., a_{31}$  and a part of duration 1024 chips with no transmission that is not formally part of the AICH. The part of the slot with no transmission is reserved for possible use by CSICH or possible future use by other physical channels.

The spreading factor (SF) used for channeliszation of the AICH is 256.

The phase reference for the AICH is the Primary CPICH.



#### Figure 21: Structure of Acquisition Indicator Channel (AICH)

The real-valued symbols  $a_0, a_1, \ldots, a_{31}$  in figure 21 are given by

$$a_{j} = \sum_{s=0}^{15} AI_{s}b_{s,j}$$

where AI<sub>s</sub>, taking the values +1, -1, and 0, is the acquisition indicator corresponding to signature s and the sequence  $b_{s,0}$ , ...,  $b_{s,31}$  is given by table 20. If the signature s is not a member of the set of available signatures for all the Access Service Class (ASC) for the corresponding PRACH (cf [5]), then AI<sub>s</sub> shall be set to 0.

The use of acquisition indicators is described in [5]. If an Acquisition Indicator is set to +1, it represents a positive acknowledgement. If an Acquisition Indicator is set to -1, it represents a negative acknowledgement.

The real-valued symbols,  $a_i$ , are spread and modulated in the same fashion as bits when represented in  $\{+1, -1\}$  form.

In case STTD-based open-loop transmit diversity is applied to AICH, STTD encoding according to subclause 5.3.1.1.1 is applied to each sequence  $b_{s,0}$ ,  $b_{s,1}$ , ...,  $b_{s,31}$  separately before the sequences are combined into AICH symbols  $a_0$ , ...,  $a_{31}$ .

S														l	<b>0</b> s,0,	b <sub>s,1</sub>	ı,	b <sub>s,3</sub>	81													
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1
2	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1
3	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1
4	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1
5	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1
6	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1
7	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
9	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
10	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
11	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1
12	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
13	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1
14	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1
15	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1

Table 20: AICH signature patterns

### 5.3.3.7 CPCH Access Preamble Acquisition Indicator Channel (AP-AICH)

The Access Preamble Acquisition Indicator channel (AP-AICH) is a fixed rate (SF=256) physical channel used to carry AP acquisition indicators (API) of CPCH. AP acquisition indicator API<sub>s</sub> corresponds to AP signature *s* transmitted by UE.

AP-AICH and AICH may use the same or different channelisation codes. The phase reference for the AP-AICH is the Primary CPICH. Figure 22 illustrates the structure of AP-AICH. The AP-AICH has a part of duration 4096 chips where the AP acquisition indicator (API) is transmitted, followed by a part of duration 1024chips with no transmission that is not formally part of the AP-AICH. The part of the slot with no transmission is reserved for possible use by CSICH or possible future use by other physical channels.

The spreading factor (SF) used for channeliszation of the AP-AICH is 256.

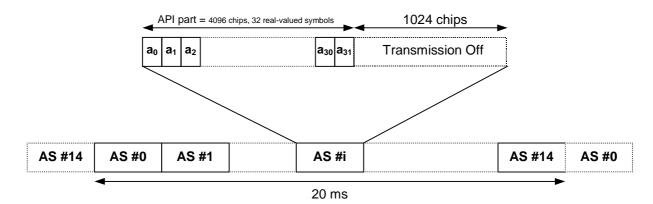


Figure 22: Structure of AP Acquisition Indicator Channel (AP-AICH)

The real-valued symbols  $a_0, a_1, ..., a_{31}$  in figure 22 are given by

$$\mathbf{a}_{j} = \sum_{s=0}^{15} \mathbf{API}_{s} \times \mathbf{b}_{s,j}$$

where API<sub>s</sub>, taking the values +1, -1, and 0, is the AP acquisition indicator corresponding to Access Preamble signature s transmitted by UE and the sequence  $b_{s,0}, ..., b_{s,31}$  is given in Table 20. If the signature s is not a member of the set of UL Access Preamble signatures for the corresponding PCPCH (cf [5] then API<sub>s</sub> shall be set to 0.

The use of acquisition indicators is described in [5]. If an AP acquisition indicator is set to +1, it represents a positive acknowledgement. If an AP acquisition indicator is set to -1, it represents a negative acknowledgement.

The real-valued symbols,  $a_i$ , are spread and modulated in the same fashion as bits when represented in  $\{+1, -1\}$  form.

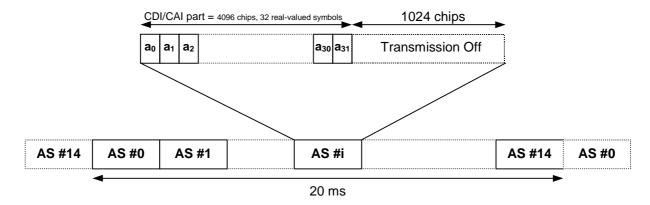
In case STTD-based open-loop transmit diversity is applied to AP-AICH, STTD encoding according to subclause 5.3.1.1.1 is applied to each sequence  $b_{s,0}$ ,  $b_{s,1}$ , ...,  $b_{s,31}$  separately before the sequences are combined into AP-AICH symbols  $a_0$ , ...,  $a_{31}$ .

#### 5.3.3.8 CPCH Collision Detection/Channel Assignment Indicator Channel (CD/CA-ICH)

The Collision Detection Channel Assignment Indicator channel (CD/CA-ICH) is a fixed rate (SF=256) physical channel used to carry CD Indicator (CDI) only if the CA is not active, or CD Indicator/CA Indicator (CDI/CAI) at the same time if the CA is active. The structure of CD/CA-ICH is shown in figure 23. CD/CA-ICH and AP-AICH may use the same or different channelisation codes.

The CD/CA-ICH has a part of duration of 4096chips where the CDI/CAI is transmitted, followed by a part of duration 1024chips with no transmission that is not formally part of the CD/CA-ICH. The part of the slot with no transmission is reserved for possible use by CSICH or possible future use by other physical channels.

The spreading factor (SF) used for channeliszation of the CD/CA-ICH is 256.



#### Figure 23: Structure of CD/CA Indicator Channel (CD/CA-ICH)

In case STTD-based open-loop transmit diversity is applied to CD/CA-ICH, STTD encoding according to subclause 5.3.1.1.1 is applied to each sequence  $b_{s,0}$ ,  $b_{s,1}$ , ...,  $b_{s,31}$  separately before the sequences are combined into CD/CA-ICH symbols  $a_0$ , ...,  $a_{31}$ .

In case CA is not active, the real-valued symbols a<sub>0</sub>, a<sub>1</sub>, ..., a<sub>31</sub> in figure 23 are given by

$$a_{j} = \sum_{s=0}^{15} CDI_{s} \times b_{s,j}$$

where  $CDI_s$ , taking the values +1, and 0, is the CD indicator corresponding to CD preamble signature *s* transmitted by UE and the sequence  $b_{s,0}, ..., b_{s,31}$  is given in table 20. If the signature *s* is not a member of the set of CD Preamble signatures for the corresponding PCPCH (cf [5]), then CDI<sub>s</sub> shall be set to 0.

1

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The real-valued symbols,  $a_i$ , are spread and modulated in the same fashion as bits when represented in  $\{+1, -1\}$  form.

In case CA is active, the real-valued symbols  $a_0, a_1, \ldots, a_{31}$  in figure 23 are given by

$$a_{j} = \sum_{i=0}^{15} CDI_{i} \times b_{s_{i},j} + \sum_{k=0}^{15} CAI_{k} \times b_{s_{k},j}$$

where the subscript  $s_i$ ,  $s_k$  depend on the indexes *i*, *k* according to table 21, respectively, and indicate the signature number *s* in table 20. The sequence  $b_{s,0}$ , ...,  $b_{s,31}$  is given in table 20. CDI<sub>i</sub>, taking the values +1/0 or -1/0, is the CD indicator corresponding to the CD preamble *i* transmitted by the UE, and CAI<sub>k</sub>, taking the values +1/0 or -1/0, is the CA indicator corresponding to the assigned channel index *k* as given in table 21. If the signature  $s_i$  is not a member of the set of CD Preamble signatures for the corresponding PCPCH (cf [5]), then CDI<sub>s</sub> shall be set to 0. Similarly, if the signature  $s_k$  is not a member of the set of CD Preamble signatures for the corresponding PCPCH (cf [5]), then CDI<sub>s</sub> shall be set to 0.

UE transmitted CD Preamble /	CDIi	signature <i>s</i> i	Channel Assignment Index <i>k</i>	CAIk	Signature <i>s</i> k
0	+1/0	1	0	+1/0	0
1	-1/0	I	1	-1/0	0
2	+1/0	3	2	+1/0	8
3	-1/0	3	3	-1/0	0
4	+1/0	5	4	+1/0	4
5	-1/0	5	5	-1/0	4
6	+1/0	7	6	+1/0	12
7	-1/0	1	7	-1/0	12
8	+1/0	9	8	+1/0	2
9	-1/0	9	9	-1/0	2
10	+1/0	11	10	+1/0	106
11	-1/0	11	11	-1/0	<u>10</u> 6
12	+1/0	13	12	+1/0	610
13	-1/0	13	13	-1/0	<u>6</u> 10
14	+1/0	15	14	+1/0	14
15	-1/0	15	15	-1/0	14

Table 21	Generation of	CDI <sub>i</sub> /CAI <sub>k</sub>
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#### 5.3.2.1 STTD for DPCH

The pilot bit pattern for the DPCH channel transmitted on antenna 2 is given in table 14.

- For  $N_{pilot} = 8$ , 16 the shadowed part indicates pilot bits that are obtained by STTD encoding the corresponding (shadowed) bits in Table 12. The non-shadowed pilot bit pattern is orthogonal to the corresponding (non-shadowed) pilot bit pattern in table 12.
- For  $N_{pilot} = 4$ , the diversity antenna pilot bit pattern is obtained by STTD encoding both the shadowed and non-shadowed pilot bits in table 12.
- For  $N_{pilot} = 2$ , the diversity antenna pilot pattern is obtained by STTD encoding the two pilot bits in table 12 with the last two bits (data or DTX) of the second data field (data2) of the slot. Thus for  $N_{pilot} = 2$  case, the last two bits of the second data field (data 2) after STTD encoding, follow the diversity antenna pilot bits in Table 14.

STTD encoding for the DPDCH, TPC, and TFCI fields is done as described in subclause 5.3.1.1.1. For the SF=512 DPCH, the first two bits in each slot, i.e. TPC bits, are not STTD encoded and the same bits are transmitted with equal power from the two antennas. The remaining four bits are STTD encoded.

For compressed mode through spreading factor reduction and for  $N_{pilot} > 4$ , symbol repetition shall be applied to the pilot bit patterns of table 14, in the same manner as described in 5.3.2. For slot formats 2B and 3B, i.e. compressed mode through spreading factor reduction and  $N_{pilot} = 4$ , the pilot bits <u>transmitted</u> on antenna <u>1-2</u> are STTD encoded, and thus the pilot bit pattern is as shown in the most right set of table 14.

	N <sub>pilot</sub> = 2 (*1)	N <sub>pilo</sub> (*:	t <b>= 4</b> 2)		N <sub>pilot</sub> = 8 N <sub>pilot</sub> = 16 (*3) (*4)							N <sub>pilot</sub> = 4 (*5)					
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7	0	1
Slot #0	01	01	10	11	00	00	10	11	00	00	10	11	00	00	10	01	10
1	10	10	10	11	00	00	01	11	00	00	01	11	10	00	10	10	01
2	11	11	10	11	11	00	00	11	11	00	00	11	10	00	11	11	00
3	10	10	10	11	10	00	01	11	10	00	01	11	00	00	00	10	01
4	00	00	10	11	11	00	11	11	11	00	11	11	01	00	10	00	11
5	01	01	10	11	00	00	10	11	00	00	10	11	11	00	00	01	10
6	01	01	10	11	10	00	10	11	10	00	10	11	01	00	11	01	10
7	00	00	10	11	10	00	11	11	10	00	11	11	10	00	11	00	11
8	11	11	10	11	00	00	00	11	00	00	00	11	01	00	01	11	00
9	01	01	10	11	01	00	10	11	01	00	10	11	01	00	01	01	10
-	11	11	10	11	11	00	00	11	11	00	00	11	00	00	10	11	00
10	00	00	10	11	01	00	11	11	01	00	11	11	00	00	01	00	11
11	00	00	10	11	10	00	11	11	10	00	11	11	11	00	00	00	11
12	10	10	10	11	01	00	01	11	01	00	01	11	10	00	01	10	01
13	10	10	10	11	01	00	01	11	01	00	01	11	11	00	11	10	01
14																	

Table 14: Pilot bit patterns of downlink DPCCH for antenna 2 using STTD

NOTE \*1: The pilot bits precede the last two bits of the data2 field.

NOTE \*2: This pattern is used except slot formats 2B and 3B.

NOTE \*3: This pattern is used except slot formats 0B, 1B, 4B, 5B, 8B, and 9B.

NOTE \*4: This pattern is used except slot formats 6B, 7B, 10B, 11B, 12B, and 13B.

NOTE \*5: This pattern is used for slot formats 2B and 3B.

NOTE: For slot format *n*B where n = 0, 1, 4, 5, 6, ..., 15, the pilot bit pattern corresponding to N<sub>pilot</sub>/2 is to be used and symbol repetition shall be applied.

#### 3G TS 25.211 V3.3.0 (2000-06)

#### Release 1999

### 3GPP TSG RAN Meeting #9

**Document** R1-00-1049

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# 2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- [1] 3G TS 25.201: "Physical layer general description".
- [2] 3G TS 25.211: "Physical channels and mapping of transport channels onto physical channels (FDD)".
- [3] 3G TS 25.212: "Multiplexing and channel coding (FDD)".
- [4] 3G TS 25.213: "Spreading and modulation (FDD)".
- [5] 3G TS 25.214: "Physical layer procedures (FDD)".
- [6] 3G TS 25.221: "Transport channels and physical channels (TDD)".
- [7] 3G TS 25.222: "Multiplexing and channel coding (TDD)".
- [8] 3G TS 25.223: "Spreading and modulation (TDD)".
- [9] 3G TS 25.224: "Physical layer procedures (TDD)".
- [10] 3G TS 25.231: "Measurements".
- [11] 3G TS 25.301: "Radio Interface Protocol Architecture".
- [12] 3G TS 25.302: "Services Provided by the Physical Layer".
- [13] 3G TS 25.401: "UTRAN Overall Description".
- [14] 3G TS 25.133: "Requirements for Support of Radio Resource Management (FDD)".

# 7.6 DPCCH/DPDCH timing relations

### 7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

### 7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

# 7.6.3 Uplink/downlink timing at UE

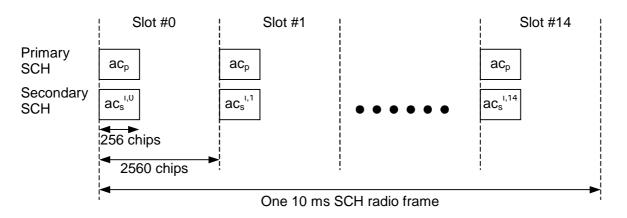
At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately  $T_0$  chips after the reception of the first significant detected path (in time) of the corresponding downlink DPCCH/DPDCH frame.  $T_0$  is a constant defined to be 1024 chips. The first detected path (in time) is defined implicitly by the relevant tests in [14]. More information about the uplink/downlink timing relation and meaning of  $T_0$  can be found in [5].

<b>25.211</b> CR 076 Current Version: 3.3.0	_
GSM (AA.BB) or 3G (AA.BBB) specification number ↑ ↑ CR number as allocated by MCC support team	
For submission to:       RAN #9       for approval       X       strategic       (for SN list expected approval meeting # here for information       for information       Non-strategic       (for SN list expected approval	
Form: CR cover sheet, version 2 for 3GPP and SMG The latest version of this form is available from: <a href="http://ftp.3gpp.org/Information/CR-Fc">http://ftp.3gpp.org/Information/CR-Fc</a>	orm- doc
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Source:         TSG RAN WG1         Date:         2000-08-18	
Subject: Clarification of SCH transmitted by TSTD	
Work item:	
Category:FCorrectionRelease:Phase 2(only one category shall be marked with an X)A Corresponds to a correction in an earlier releaseImage: CRelease 96DEditorial modification of feature DEditorial modificationImage: CRelease 97Release 99Release 99Release 99Release 90Release 99	X
Reason for       In case of SCH transmitted by TSTD, SCH is not transmitted in Antenna 2 of slot #0         change:       Antenna 1 of slot #1 Antenna 2 of slot #14. Describing not transmitting SCH can avoid misunderstand.	,
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#### 5.3.3.4 Synchronisation Channel (SCH)

The Synchronisation Channel (SCH) is a downlink signal used for cell search. The SCH consists of two sub channels, the Primary and Secondary SCH. The 10 ms radio frames of the Primary and Secondary SCH are divided into 15 slots, each of length 2560 chips. Figure 18 illustrates the structure of the SCH radio frame.



#### Figure 18: Structure of Synchronisation Channel (SCH)

The Primary SCH consists of a modulated code of length 256 chips, the Primary Synchronisation Code (PSC) denoted  $c_p$  in figure 18, transmitted once every slot. The PSC is the same for every cell in the system.

The Secondary SCH consists of repeatedly transmitting a length 15 sequence of modulated codes of length 256 chips, the Secondary Synchronisation Codes (SSC), transmitted in parallel with the Primary SCH. The SSC is denoted  $c_s^{i,k}$  in figure 18, where i = 0, 1, ..., 63 is the number of the scrambling code group, and k = 0, 1, ..., 14 is the slot number. Each SSC is chosen from a set of 16 different codes of length 256. This sequence on the Secondary SCH indicates which of the code groups the cell's downlink scrambling code belongs to.

The primary and secondary synchronization codes are modulated by the symbol *a* shown in figure 18, which indicates the presence/ absence of STTD encoding on the P-CCPCH and is given by the following table:

P-CCPCH STTD encoded	a = +1
P-CCPCH not STTD encoded	a = -1

#### 5.3.3.4.1 SCH transmitted by TSTD

Figure 19 illustrates the structure of the SCH transmitted by the TSTD scheme. In even numbered slots both PSC and SSC are transmitted on antenna 1, and in odd numbered slots both PSC and SSC are transmitted on antenna 2.

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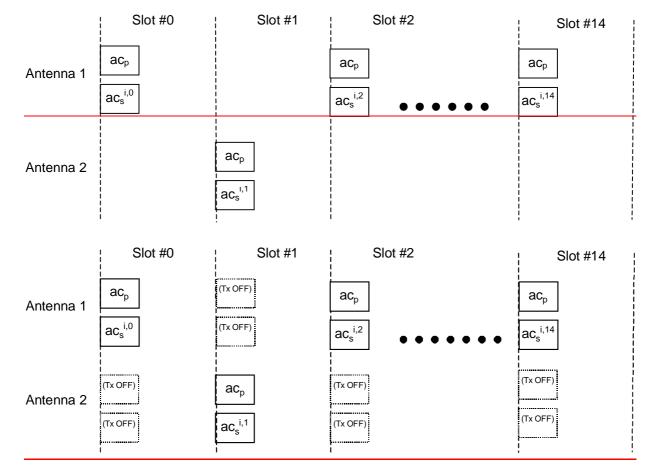


Figure 19: Structure of SCH transmitted by TSTD scheme

e.g. for 3GPP use the format TP-99xxx or for SMG, use the format P-99-xxx

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# 5.2 Uplink physical channels

### 5.2.1 Dedicated uplink physical channels

There are two types of uplink dedicated physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH).

The DPDCH and the DPCCH are I/Q code multiplexed within each radio frame (see [4]).

The uplink DPDCH is used to carry the DCH transport channel. There may be zero, one, or several uplink DPDCHs on each radio link.

The uplink DPCCH is used to carry control information generated at Layer 1. The Layer 1 control information consists of known pilot bits to support channel estimation for coherent detection, transmit power-control (TPC) commands, feedback information (FBI), and an optional transport-format combination indicator (TFCI). The transport-format combination indicator informs the receiver about the instantaneous transport format combination of the transport channels mapped to the simultaneously transmitted uplink DPDCH radio frame. There is one and only one uplink DPCCH on each radio link.

Figure 1 shows the frame structure of the uplink dedicated physical channels. Each radio frame of length 10 ms is split into 15 slots, each of length  $T_{slot} = 2560$  chips, corresponding to one power-control period.

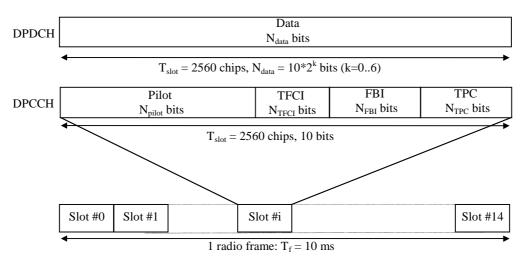


Figure 1: Frame structure for uplink DPDCH/DPCCH

The parameter k in figure 1 determines the number of bits per uplink DPDCH slot. It is related to the spreading factor SF of the DPDCH as  $SF = 256/2^k$ . The DPDCH spreading factor may range from 256 down to 4. The spreading factor of the uplink DPCCH is always equal to 256, i.e. there are 10 bits per uplink DPCCH slot.

The exact number of bits of the uplink DPDCH and the different uplink DPCCH fields ( $N_{pilot}$ ,  $N_{TFCI}$ ,  $N_{FBI}$ , and  $N_{TPC}$ ) is given by table 1 and table 2. What slot format to use is configured by higher layers and can also be reconfigured by higher layers.

The channel bit and symbol rates given in table 1 and table 2 are the rates immediately before spreading. The pilot patterns are given in table 3 and table 4, the TPC bit pattern is given in table 5.

The FBI bits are used to support techniques requiring feedback from the UE to the UTRAN Access Point, including closed loop mode transmit diversity and site selection diversity transmission (SSDT). The structure of the FBI field is shown in figure 2 and described below.

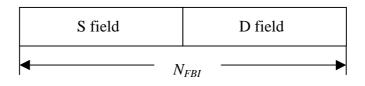


Figure 2: Details of FBI field

The S field is used for SSDT signalling, while the D field is used for closed loop mode transmit diversity signalling. The S field consists of 0, 1 or 2 bits. The D field consists of 0 or 1 bit. The total FBI field size  $N_{FBI}$  is given by table 2. If total FBI field is not filled with S field or D field, FBI field shall be filled with "1". When  $N_{FBI}$  is 2bits, S field is 0bit and D field is 1bit, left side field shall be filled with "1" and right side field shall be D field. Simultaneous use of SSDT power control and closed loop mode transmit diversity requires that the S field consists of 1 bit. The use of the FBI fields is described in detail in [5].

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N <sub>data</sub>
0	15	15	256	150	10	10
1	30	30	128	300	20	20
2	60	60	64	600	40	40
3	120	120	32	1200	80	80
4	240	240	16	2400	160	160
5	480	480	8	4800	320	320
6	960	960	4	9600	640	640

#### **Table 1: DPDCH fields**

There are two types of uplink dedicated physical channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI (e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 2. It is the UTRAN that determines if a TFCI should be transmitted and it is mandatory for all UEs to support the use of TFCI in the uplink. The mapping of TFCI bits onto slots is described in [3].

In compressed mode, DPCCH slot formats with TFCI fields are changed. There are two possible compressed slot formats for each normal slot format. They are labelled A and B and the selection between them is dependent on the number of slots that are transmitted in each frame in compressed mode.

Slot Form at #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N <sub>pilot</sub>	N <sub>TPC</sub>	N <sub>tfCi</sub>	N <sub>FBI</sub>	Transmitted slots per radio frame
0	15	15	256	150	10	6	2	2	0	15
0A	15	15	256	150	10	5	2	3	0	10-14
0B	15	15	256	150	10	4	2	4	0	8-9
1	15	15	256	150	10	8	2	0	0	8-15
2	15	15	256	150	10	5	2	2	1	15
2A	15	15	256	150	10	4	2	3	1	10-14
2B	15	15	256	150	10	3	2	4	1	8-9
3	15	15	256	150	10	7	2	0	1	8-15
4	15	15	256	150	10	6	2	0	2	8-15
5	15	15	256	150	10	5	1	2	2	15
5A	15	15	256	150	10	4	1	3	2	10-14
5B	15	15	256	150	10	3	1	4	2	8-9

#### Table 2: DPCCH fields

The pilot bit patterns are described in table 3 and table 4. The shadowed column part of pilot bit pattern is defined as FSW and FSWs can be used to confirm frame synchronization. (The value of the pilot bit pattern other than FSWs shall be "1".)

	N <sub>pilot</sub> = 3			N <sub>pilot</sub> = 4				N <sub>pilot</sub> = 5				N <sub>pilot</sub> = 6						
Bit #	0	1	2	0	1	2	3	0	1	2	3	4	0	1	2	3	4	5
Slot #0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
1	0	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1	1	0
2	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
3	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0
4	1	0	1	1	1	0	1	1	0	1	0	1	1	1	0	1	0	1
5	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0
6	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0
7	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
8	0	1	1	1	0	1	1	0	1	1	1	0	1	0	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
11	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1
12	1	0	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0	0
13	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1
14	0	0	1	1	0	0	1	0	0	1	1	1	1	0	0	1	1	1

Table 3: Pilot bit patterns for uplink DPCCH with  $N_{pilot} = 3, 4, 5$  and 6

Table 4: Pilot bit patterns for upline	COPCCH with N <sub>pilot</sub> = 7 and 8
--	--

			N	pilot =	7						Npilo	<sub>t</sub> = 8			
Bit #	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7
Slot #0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
1	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0
2	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
3	1	0	0	1	0	0	1	1	0	1	0	1	0	1	0
4	1	1	0	1	0	1	1	1	1	1	0	1	0	1	1
5	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0
6	1	1	1	1	0	0	1	1	1	1	1	1	0	1	0
7	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
8	1	0	1	1	1	0	1	1	0	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1
11	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	1	0	0	1	1	1	1	0	1	0	1	0
13	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1
14	1	0	0	1	1	1	1	1	0	1	0	1	1	1	1

The relationship between the TPC bit pattern and transmitter power control command is presented in table 5.

Table 5:	TPC Bit	Pattern
----------	---------	---------

TPC Bit	Pattern	Transmitter power				
N <sub>TPC</sub> = 1	N <sub>TPC</sub> = 2	control command				
1	11	1				
0	00	0				

Multi-code operation is possible for the uplink dedicated physical channels. When multi-code transmission is used, several parallel DPDCH are transmitted using different channelization codes, see [4]. However, there is only one DPCCH per radio link.

A power control preamble may be used for initialisation of a DCH. Both the UL and DL DPCCHs shall be transmitted during the power control preamble. The length of the power control preamble is a UE-specific higher layer parameter,  $N_{pcp}$  (see [5], section 5.1.2.4), signalled by the network. The UL DPCCH shall take the same slot format in the power control preamble as afterwards, as given in table 2. When,  $N_{pcp} > 0$  the pilot patterns from slot #(15-  $N_{pcp}$ ) to slot #14 of table 3 and table 4 shall be used. The timing of the power control preamble is shown in Figure 33 in subclause 7.7. The TFCI field is filled with "1" bits.