Düsseldorf, Germany, 21-23 June 2000
Title: $\quad$ Agreed CRs to TS 25.213
Source: TSG-RAN WG1
Agenda item: 5.1.3

| No. | Doc \# | Spec | CR | Rev | Subject | Cat | Current_v | New_v |
| :---: | :---: | :---: | :---: | :---: | :--- | :---: | :---: | :---: |
| 1 | R1-000559 | 25.213 | 033 | - | Clarifications to power control preamble sections | F | 3.2 .0 | 3.3 .0 |
| 2 | R1-000711 | 25.213 | 034 | 2 | Numbering of the PCPCH access preamble and | D | 3.2 .0 | 3.3 .0 |
| 3 | R1-000549 | 25.213 | 035 | - | DPDCH/DPCCH gain factors | F | 3.2 .0 | 3.3 .0 |

## CHANGE REQUEST

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### 25.213 CR 033

Current Version: 3.2.0
GSM (AA.BB) or $3 G(A A . B B B)$ specification number $\uparrow$
$\uparrow$ CR number as allocated by MCC support team

For submission to: TSG-RAN \#8 list expected approval meeting \# here

| for approval |  |
| ---: | ---: |
| for information | $\mathbf{X}$ |
|  |  |
|  |  |



Form: CR cover sheet, version 2 for 3GPP and SMG The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc
Proposed change affects:
(at least one should be marked with an X)

Source:
TSG RAN WG1

ME $\mathbf{X}$
UTRAN / Radio $\qquad$ X Core Network $\square$

$\square$


Date: 2000-04-05
Subject: Clarifications to power control preamble sections

## Work item:

| Category: | F | Correction | X | Release: | Phase 2 |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | A | Corresponds to a correction in an earlier release |  |  | Release 96 |
| (only one category | B | Addition of feature |  |  | Release 97 |
| shall be marked | C | Functional modification of feature |  |  | Release 98 |
| with an $X$ ) | D | Editorial modification |  |  | Release 99 |
|  |  |  |  |  | Release 00 |

Reason for Clarification of channelisation and scrambling codes for power control preambles in change: DCH.

Clauses affected: $\quad$ 4.3.1.2,4.3.2.4

| Other specs | Other 3G core specifications <br> Other GSM core <br> affected: <br> specifications | $\square$ |
| :--- | :--- | :--- |
|  | $\rightarrow$ List of CRs: |  |
|  | $\rightarrow$ List of CRs: |  |
|  | MS test specifications <br> BSS test specifications <br> O\&M specifications | $\rightarrow$ List of CRs: |
|  | $\rightarrow$ List of CRs: |  |
|  | $\rightarrow$ List of CRs: |  |

## Other comments:

### 4.3 Code generation and allocation

### 4.3.1 Channelization codes

### 4.3.1.1 Code definition

The channelization codes of figure 1 are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between a user's different physical channels. The OVSF codes can be defined using the code tree of figure 4.


Figure 4: Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes
In figure 4, the channelization codes are uniquely described as $\mathrm{C}_{\mathrm{ch}, \mathrm{SF}, \mathrm{k}}$, where SF is the spreading factor of the code and $k$ is the code number, $0 \leq k \leq \mathrm{SF}-1$.

Each level in the code tree defines channelization codes of length SF, corresponding to a spreading factor of SF in figure 4.

The generation method for the channelization code is defined as:

$$
\begin{gathered}
\mathrm{C}_{\mathrm{ch}, 1,0}=1, \\
{\left[\begin{array}{c}
C_{c h, 2,0} \\
C_{c h, 2,1}
\end{array}\right]=\left[\begin{array}{cc}
C_{c h, 1,0} & C_{c h, 1,0} \\
C_{c h, 1,0} & -C_{c h, 1,0}
\end{array}\right]=\left[\begin{array}{cc}
1 & 1 \\
1 & -1
\end{array}\right]} \\
{\left[\begin{array}{c}
C_{c h, 2(n+1), 0} \\
C_{c h, 2}(n+1), 1 \\
C_{c h, 2}(n+1), 2 \\
C_{c h, 2}(n+1), 3 \\
\vdots \\
C_{c h, 2}(n+1),(n+1) l_{2} \\
C_{c h, 2}(n+1), 2(n+1)-1
\end{array}\right]=\left[\begin{array}{cc}
C_{c h, 2^{n}, 0} & C_{c h, 2^{n}, 0} \\
C_{c h, 2^{2}, 0} & -C_{c h, 2^{n}, 0} \\
C_{c h, 2^{n}, 1} & C_{c h, 2^{2}, 1} \\
C_{c h, 2^{n}, 1} & -C_{c h, 2^{n}, 1} \\
\vdots & \vdots \\
C_{c h, 2^{n}, 2^{n}-1} & C_{c h, 2^{n}, 2^{n}-1} \\
C_{c h, 2^{n}, 2^{n}-1} & -C_{c h, 2^{n}, 2^{n}-1}
\end{array}\right]}
\end{gathered}
$$

The leftmost value in each channelization code word corresponds to the chip transmitted first in time.

### 4.3.1.2 Code allocation for DPCCH/DPDCH

For the DPCCH and DPDCHs the following applies:

- The DPCCH is always spread by code $\mathrm{c}_{\mathrm{c}}=\mathrm{C}_{\mathrm{ch}, 256,0}$.
- When only one DPDCH is to be transmitted, $\mathrm{DPDCH}_{1}$ is spread by code $\mathrm{c}_{\mathrm{d}, 1}=\mathrm{C}_{\mathrm{ch}, \mathrm{SF}, \mathrm{k}}$ where SF is the spreading factor of $\mathrm{DPDCH}_{1}$ and $\mathrm{k}=\mathrm{SF} / 4$.
- When more than one DPDCH is to be transmitted, all DPDCHs have spreading factors equal to $4 . \mathrm{DPDCH}_{n}$ is spread by the the code $\mathrm{c}_{\mathrm{d}, \mathrm{n}}=\mathrm{C}_{\mathrm{ch}, 4, \mathrm{k}}$, where $k=1$ if $n \in\{1,2\}, k=3$ if $n \in\{3,4\}$, and $k=2$ if $n \in\{5,6\}$.

If a power control preamble is used to initialise a DCH, the channelisation code for the DPCCH during the power control preamble shall be the same as that to be used afterwards.

### 4.3.1.3 Code allocation for PRACH message part

The preamble signature $s, 0 \leq s \leq 15$, points to one of the 16 nodes in the code-tree that corresponds to channelization codes of length 16. The sub-tree below the specified node is used for spreading of the message part. The control part is spread with the channelization code $\mathrm{c}_{\mathrm{c}}$ (as shown in section 4.2.2.2) of spreading factor 256 in the lowest branch of the sub-tree, i.e. $\mathrm{c}_{\mathrm{c}}=\mathrm{C}_{\mathrm{ch}, 256, \mathrm{~m}}$ where $\mathrm{m}=16 \times \mathrm{s}+15$. The data part uses any of the channelization codes from spreading factor 32 to 256 in the upper-most branch of the sub-tree. To be exact, the data part is spread by channelization code $\mathrm{c}_{\mathrm{d}}=\mathrm{C}_{\mathrm{ch}, \mathrm{SF}, \mathrm{m}}$ and SF is the spreading factor used for the data part and $\mathrm{m}=\mathrm{SF} \times \mathrm{s} / 16$.

### 4.3.1.4 Code allocation for PCPCH message part

For the control part and data part the following applies:

- The control part is always spread by code $\mathrm{c}_{\mathrm{c}}=\mathrm{C}_{\mathrm{ch}, 256,0}$.
- The data part is spread by code $\mathrm{c}_{\mathrm{d}}=\mathrm{C}_{\mathrm{ch}, \mathrm{SF}, \mathrm{k}}$ where SF is the spreading factor of the data part and $\mathrm{k}=\mathrm{SF} / 4$.

The data part may use the code from spreading factor 4 to 256 . A UE is allowed to increase SF during the message transmission on a frame by frame basis.

### 4.3.1.5 Channelisation code for PCPCH power control preamble

The channelisation code for the PCPCH power control preamble is the same as that used for the control part of the message part, as described in section 4.3.1.4 above.

### 4.3.2 Scrambling codes

### 4.3.2.1 General

All uplink physical channels are subjected to scrambling with a complex-valued scrambling code. The DPCCH/DPDCH may be scrambled by either long or short scrambling codes, defined in section 4.3.2.4. The PRACH message part is scrambled with a long scrambling code, defined in section 4.3.2.5. Also the PCPCH message part is scrambled with a long scrambling code, defined in section 4.3.2.6.
There are $2^{24}$ long and $2^{24}$ short uplink scrambling codes. Uplink scrambling codes are assigned by higher layers.
The long scrambling code is built from constituent long sequences defined in section 4.3.2.2, while the constituent short sequences used to build the short scrambling code are defined in section 4.3.2.3.

### 4.3.2.2 Long scrambling sequence

The long scrambling sequences $\mathrm{c}_{\text {long, }, \mathrm{n}, \mathrm{n}}$ and $\mathrm{c}_{\text {long }, 2, \mathrm{n}}$ are constructed from position wise modulo 2 sum of 38400 chip segments of two binary $m$-sequences generated by means of two generator polynomials of degree 25 . Let $x$, and $y$ be the two $m$-sequences respectively. The $x$ sequence is constructed using the primitive (over $\mathrm{GF}(2)$ ) polynomial $X^{25}+X^{3}+1$. The $y$ sequence is constructed using the polynomial $X^{25}+X^{3}+X^{2}+X+1$. The resulting sequences thus constitute segments of a set of Gold sequences.

The sequence $c_{\text {long } 2, n}$ is a 16777232 chip shifted version of the sequence $c_{\text {long }, 1, n}$.
Let $n_{23} \ldots n_{0}$ be the 24 bit binary representation of the scrambling sequence number $n$ with $n_{0}$ being the least significant bit. The $x$ sequence depends on the chosen scrambling sequence number $n$ and is denoted $x_{n}$, in the sequel. Furthermore, let $x_{n}(i)$ and $y(i)$ denote the $i$ :th symbol of the sequence $x_{n}$ and $y$, respectively.

The $m$-sequences $x_{n}$ and $y$ are constructed as:
Initial conditions:
$-\quad x_{n}(0)=n_{0}, x_{n}(1)=n_{1}, \ldots=x_{n}(22)=n_{22}, x_{n}(23)=n_{23}, x_{n}(24)=1$.

- $y(0)=y(1)=\ldots=y(23)=y(24)=1$.

Recursive definition of subsequent symbols:

- $\quad x_{n}(i+25)=x_{n}(i+3)+x_{n}(i)$ modulo 2, $i=0, \ldots, 2^{25}-27$.
- $y(i+25)=y(i+3)+y(i+2)+y(i+1)+y(i)$ modulo $2, i=0, \ldots, 2^{25}-27$.

Define the binary Gold sequence $z_{n}$ by:

- $\quad z_{n}(i)=x_{n}(i)+y(i)$ modulo $2, i=0,1,2, \ldots, 2^{25}-2$.

The real valued Gold sequence $Z_{n}$ is defined by:

$$
Z_{n}(i)=\left\{\begin{array}{ll}
+1 & \text { if } z_{n}(i)=0 \\
-1 & \text { if } z_{n}(i)=1
\end{array} \text { for } i=0,1, \ldots, 2^{25}-2\right.
$$

Now, the real-valued long scrambling sequences $c_{\text {long, } 1, \mathrm{n}}$ and $\mathrm{c}_{\text {long, } 2, \mathrm{n}}$ are defined as follows:

$$
\begin{gathered}
\mathrm{c}_{\text {long }, 1, \mathrm{n}}(i)=Z_{n}(i), i=0,1,2, \ldots, 2^{25}-2 \text { and } \\
\mathrm{c}_{\text {long }, 2, \mathrm{n}}(i)=Z_{n}\left((i+16777232) \text { modulo }\left(2^{25}-1\right)\right), i=0,1,2, \ldots, 2^{25}-2 .
\end{gathered}
$$

Finally, the complex-valued long scrambling sequence $\mathrm{C}_{\text {long, } \mathrm{n}}$, is defined as:

$$
C_{\text {long }, n}(i)=c_{\text {long }, 1, n}(i)\left(1+j(-1)^{i} c_{\text {long }, 2, n}(2\lfloor i / 2\rfloor)\right)
$$

where $i=0,1, \ldots, 2^{25}-2$ and $\rfloor$ denotes rounding to nearest lower integer.


Figure 5: Configuration of uplink scrambling sequence generator

### 4.3.2.3 Short scrambling sequence

The short scrambling sequences $c_{\text {short } 1, n, n}(i)$ and $c_{\text {short } 2, n}(i)$ are defined from a sequence from the family of periodically extended $S(2)$ codes.

Let $n_{23} n_{22} \ldots n_{0}$ be the 24 bit binary representation of the code number $n$.
The $n$ :th quaternary $\mathrm{S}(2)$ sequence $z_{n}(i), 0 \leq n \leq 16777215$, is obtained by modulo 4 addition of three sequences, a quaternary sequence $a(i)$ and two binary sequences $b(i)$ and $d(i)$, where the initial loading of the three sequences is determined from the code number $n$. The sequence $z_{n}(i)$ of length 255 is generated according to the following relation:

$$
-\quad z_{n}(i)=a(i)+2 b(i)+2 d(i) \text { modulo } 4, i=0,1, \ldots, 254
$$

where the quaternary sequence $a(i)$ is generated recursively by the polynomial $g_{0}(x)=x^{8}+x^{5}+3 x^{3}+x^{2}+2 x+1$ as:

- $a(0)=2 n_{0}+1$ modulo $4 ;$
- $a(i)=2 n_{i}$ modulo $4, i=1,2, \ldots, 7$;
- $a(i)=3 a(i-3)+a(i-5)+3 a(i-6)+2 a(i-7)+3 a(i-8)$ modulo $4, i=8,9, \ldots, 254$;
and the binary sequence $b(i)$ is generated recursively by the polynomial $g_{1}(x)=x^{8}+x^{7}+x^{5}+x+1$ as

$$
\begin{aligned}
& b(i)=n_{8+i} \text { modulo } 2, i=0,1, \ldots, 7, \\
& b(i)=b(i-1)+b(i-3)+b(i-7)+b(i-8) \text { modulo } 2, i=8,9, \ldots, 254,
\end{aligned}
$$

and the binary sequence $d(i)$ is generated recursively by the polynomial $g_{2}(x)=x^{8}+x^{7}+x^{5}+x^{4}+1$ as:

$$
\begin{aligned}
d(i) & =n_{16+i} \text { modulo } 2, i=0,1, \ldots, 7 \\
d(i) & =d(i-1)+d(i-3)+d(i-4)+d(i-8) \text { modulo } 2, i=8,9, \ldots, 254 .
\end{aligned}
$$

The sequence $z_{n}(i)$ is extended to length 256 chips by setting $z_{n}(255)=z_{n}(0)$.
The mapping from $z_{n}(i)$ to the real-valued binary sequences $c_{\text {short }, 1, n}(i)$ and $c_{\text {short } 2, n}(i), i=0,1, \ldots, 255$ is defined in Table 2.

Table 2: Mapping from $z_{n}(I)$ to $c_{\text {short, } 1, n}(I)$ and $c_{\text {short }, 2, n}(I), i=0,1, \ldots, 255$

| $z_{n}(I)$ | $C_{\text {short }, 1, n}(I)$ | $C_{\text {short }, 2, n}(I)$ |
| :---: | :---: | :---: |
| 0 | +1 | +1 |
| 1 | -1 | +1 |
| 2 | -1 | -1 |
| 3 | +1 | -1 |

Finally, the complex-valued short scrambling sequence $\mathrm{C}_{\text {short, } \mathrm{n}}$, is defined as:

$$
C_{\text {short }, n}(i)=c_{\text {shorr }, 1, n}(i \bmod 256)\left(1+j(-1)^{i} c_{\text {short }, 2, n}(2\lfloor(i \bmod 256) / 2\rfloor)\right)
$$

where $i=0,1,2, \ldots$ and $\rfloor$ denotes rounding to nearest lower integer.
An implementation of the short scrambling sequence generator for the 255 chip sequence to be extended by one chip is shown in Figure 6.


Figure 6: Uplink short scrambling sequence generator for 255 chip sequence

### 4.3.2.4 DPCCH/DPDCH scrambling code

The code used for scrambling of the uplink DPCCH/DPDCH may be of either long or short type. When the scrambling code is formed, different consituent codes are used for the long and short type as defined below.

The $n$ :th uplink scrambling code for DPCCH/DPDCH, denoted $\mathrm{S}_{\mathrm{dpch}, \mathrm{n}}$, is defined as:

$$
\mathrm{S}_{\mathrm{dpch}, \mathrm{n}}(i)=\mathrm{C}_{\mathrm{long}, \mathrm{n}}(i), i=0,1, \ldots, 38399, \text { when using long scrambling codes; }
$$

where the lowest index corresponds to the chip transmitted first in time and $\mathrm{C}_{\mathrm{long}, \mathrm{n}}$ is defined in section 4.3.2.2.
The $n$ :th uplink scrambling code for DPCCH/DPDCH, denoted $\mathrm{S}_{\mathrm{dpch}, \mathrm{n}}$, is defined as:

$$
\mathrm{S}_{\mathrm{dpch}, \mathrm{n}}(i)=\mathrm{C}_{\mathrm{short,n}}(i), i=0,1, \ldots, 38399, \text { when using short scrambling codes; }
$$

where the lowest index corresponds to the chip transmitted first in time and $\mathrm{C}_{\text {short, } n}$ is defined in section 4.3.2.3.
If a power control preamble is used to initialise a DCH , the scrambling code for the DPCCH during the power control preamble shall be the same as that to be used afterwards. The phase of the scrambling code shall be such that the end of the code is aligned with the frame boundary at the end of the power control preamble.

3GPP TSG RAN Meeting \#8
Document R1-00711
Düsseldorf, Germany, 21-23 June 2000
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format $P-99-x x x$

## CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

### 25.213 CR 034r2 Current Version: 3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number $\uparrow \quad \uparrow C R$ number as allocated by MCC support team
For submission to: TSG RAN\#8 list expected approval meeting \# here

Form: CR cover sheet, version 2 for 3GPP and SMG

| for approval |  |
| ---: | ---: |
|  | $\mathbf{X}$ |
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The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects:
(U)SIM $\square$ ME $\mathbf{X}$
UTRAN / Radio $\square$ X

Core Network $\square$
(at least one should be marked with an X)

## Source:

TSG RAN WG1
Date:
Subject: $\quad$ Numbering of the PCPCH access preamble and collision detection preamble scrambling codes

Work item: TS 25.213

| Category: | F | Correction |  |
| :--- | :--- | :--- | :--- |
|  | A | Corresponds to a correction in an earlier release |  |
| (only one category | B | Addition of feature |  |
| shall be marked | C | Functional modification of feature |  |
| with an $X$ ) | D | Editorial modification | $\mathbf{X}$ |

Release: Phase 2
Release 96
Release 97
Release 98
Release 99
Release 00


## Reason for

change:

## Clauses affected:

| Other specs affected: | Other 3G core specifications Other GSM core specifications | $\rightarrow$ List of CRs: <br> $\rightarrow$ List of CRs: |
| :---: | :---: | :---: |
|  |  |  |
|  |  |  |
|  |  | $\rightarrow$ List of CRs: |
|  | BSS test specifications | $\rightarrow$ List of CRs: |
|  | O\&M specifications | $\rightarrow$ List of CRs |

## Other

comments:

### 4.3.4 PCPCH preamble codes

### 4.3.4.1 Access preamble

### 4.3.4.1.1 Access preamble code construction

Similar to PRACH access preamble codes, the PCPCH access preamble codes $\mathrm{C}_{\mathrm{c}-\mathrm{acc}, \mathrm{n}, \mathrm{s}}$, are complex valued sequences. The PCPCH access preamble codes are built from the preamble scrambling codes $\mathrm{S}_{\mathrm{c}-\mathrm{acc}, \mathrm{n}}$ and a preamble signature $\mathrm{C}_{\mathrm{sig}, \mathrm{s}}$ as follows:
$-\quad \mathrm{C}_{\mathrm{c}-\mathrm{acc}, \mathrm{n}, \mathrm{s}}(\mathrm{k})=\mathrm{S}_{\mathrm{c}-\mathrm{ac}, \mathrm{n}}(\mathrm{k}) \times \mathrm{C}_{\mathrm{sig}, \mathrm{s}}(\mathrm{k}) \times e^{j\left(\frac{\pi}{4}+\frac{\pi}{2} k\right)}, \mathrm{k}=0,1,2,3, \ldots, 4095 ;$

- where $\mathrm{S}_{\mathrm{c}-\mathrm{acc}, \mathrm{n}}$ and $\mathrm{C}_{\mathrm{sig}, \mathrm{s}}$ are defined in section 4.3.4.1.2 and 4.3.4.1.3 below respectively.


### 4.3.4.1.2 Access preamble scrambling code

The access preamble serambling code generation is done in a way similar to that of PRACH. There are 32768 PCPCH scrambling codes in total.

The scrambling code for the PCPCH preamble part is constructed from the long scrambling sequences. There are 40960 PCPCH access preamble scrambling codes in total.

The $n$ :th PCPCH access preamble scrambling code, where $n=\underline{0} \ldots, 8192,8193, \ldots, 40959$ is defined as:

$$
-\quad S_{c-a c, n}(i)=\mathrm{c}_{\text {long }, 1 \mathrm{n}}(i), i=0,1, \ldots, 4095 ;
$$

where the sequence $c_{\text {long, } 1, \mathrm{n}}$ is defined in section 4.3.2.2.
In the case when the access resources are shared between the PRACH and PCPCH , the scrambling codes used in the PRACH preamble are used for the PCPCH preamble as well.

The 4096032768 PCPCH access preamble scrambling codes are divided into 512 groups with 8064 codes in each group. There is a one-to-one correspondence between the group of PCPCH access preamble scrambling codes in a cell and the primary scrambling code used in the downlink of the cell. The $k$ :th PCPCH scrambling code within the cell with downlink primary scrambling code $m$, for $k=\underline{0} \ldots 16,17, \ldots, 79$ and $m=0,1,2, \ldots, 511$, is $\mathrm{S}_{\mathrm{c}-\mathrm{acc}, \mathrm{n}}$ as defined above with $\mathrm{n}=16 \times \mathrm{m}+\mathrm{k}$ for $\mathrm{k}=0, \ldots, 15$ and $n=64 \times m+(k-16)+81 \underline{9276} \underline{\text { for } \mathrm{k}=16, \ldots, 79}$.

The index $\mathrm{k}=0, \ldots, 15$ may only be used as a PCPCH access preamble part scrambling code if the same code is also used for a PRACH.

The index $\mathrm{k}=16, \ldots, 79$ correspond to PCPCH access preamble scrambling codes which are not shared together with a PRACH. This leads to 32768 PCPCH specific preamble scrambling codes divided into 512 groups with 64 elements. In ease scrambling code resource is shared between PCPCH and PRACH, the index $k$ is less than 16 and the corresponding PRACH formulae shall be used. Otherwise, if the index $k$ is greater than or equal to 16 , the formula in this section shall be used.

### 4.3.4.1.3 Access preamble signature

The access preamble part of the CPCH -access burst carries one of the sixteen different orthogonal complex signatures identical to the ones used by the preamble part of the random-access burst.

### 4.3.4.2 CD preamble

### 4.3.4.2.1 CD preamble code construction

Similar to PRACH access preamble codes, the PCPCH CD preamble codes $\mathrm{C}_{\mathrm{c}-\mathrm{cd}, \mathrm{n}, \mathrm{s}}$ are complex valued sequences. The PCPCH CD preamble codes are built from the preamble scrambling codes $\mathrm{Sc}-\mathrm{cd}, \mathrm{n}$ and a preamble signature $\mathrm{C}_{\text {sig,s }}$ as follows:

- $\quad \mathrm{C}_{\mathrm{c}-\mathrm{cd}, \mathrm{n}, \mathrm{s}}(\mathrm{k})=\mathrm{S}_{\mathrm{c}-\mathrm{cd}, \mathrm{n}}(\mathrm{k}) \times \mathrm{C}_{\mathrm{sig}, s}(\mathrm{k}) \times e^{j\left(\frac{\pi}{4}+\frac{\pi}{2} k\right)}, \mathrm{k}=0,1,2,3, \ldots, 4095 ;$
where $\mathrm{S}_{\mathrm{c}-\mathrm{cd}, \mathrm{n}}$ and $\mathrm{C}_{\text {sig,s }}$ are defined in sections 4.3.4.2.2 and 4.3.4.2.3 below respectively.


### 4.3.4.2.2 CD preamble scrambling code

The PCPCH CD preamble scrambling code is derived from the same serambling code used in the CPCH aceess preamble. There are .40960 PCPCH-CD preamble scrambling codes in total.

There are 32768 PCPCH scrambling codes in total.
The $n$ :th PCPCH CD access preamble scrambling code, where $n=\underline{0}, \ldots, 8192,8193, \ldots, 40959$, is defined as:

- $\quad S_{c-c d, n}(i)=\mathrm{c}_{\text {long }, 1, \mathrm{n}}(i), i=0,1, \ldots, 4095 ;$
where the sequence $c_{\text {long, }, \mathrm{n}}$ is defined in section 4.3.2.2.
In the case when the access resources are shared between the RACH and CPCH, the serambling codes used in the RACH preamble will be used for the CPCH CD preamble as well.

The 3276840960 PCPCH scrambling codes are divided into 512 groups with 8064 codes in each group. There is a one-to-one correspondence between the group of PCPCH CD preamble scrambling codes in a cell and the primary scrambling code used in the downlink of the cell. The $k$ :th PCPCH scrambling code within the cell with downlink primary scrambling code $m, k=\underline{0,1,16,17, \ldots, 79}$ and $m=0,1,2, \ldots, 511$, is $\mathrm{S}_{\mathrm{c}-\mathrm{cd}, \mathrm{n}}$ as defined above with $\underline{\mathrm{n}=16 \times \mathrm{m}+\mathrm{k}}$


In case serambling code resource is shared between PCPCH and PRACH, the index $k$ is less than 16 and the eorrespending PRACH formulae shall be used. Otherwise, if the index $k$ is greater than or equal to 16 , the formula in this section shall be used.

The index $\mathrm{k}=0, \ldots, 15$ may only be used as a PCPCH CD preamble part scrambling code if the same code is also used for a PRACH.

The index $\mathrm{k}=16, \ldots, 79$ correspond to PCPCH CD preamble scrambling codes which are not shared together with a PRACH. This leads to 32768 PCPCH specific preamble scrambling codes divided into 512 groups with 64 elements.

### 4.3.4.2.3 CD preamble signature

The CD-preamble part of the CPCH-access burst carries one of sixteen different orthogonal complex signatures identical to the ones used by the preamble part of the random-access burst.

### 4.4 Modulation

### 4.4.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps .

### 4.4.2 Modulation

In the uplink, the complex-valued chip sequence generated by the spreading process is QPSK modulated as shown in Figure 7 below: page for instructions on how to fill in this form correctly.

### 25.213 CR 035

Current Version: 3.2.0
GSM (AA.BB) or 3G (AA.BBB) specification number $\uparrow$
$\uparrow$ CR number as allocated by MCC support team

| For submission to: TSG RAN\#8 <br> List expected approval meeting \# here <br> $\uparrow$for approval <br> for information |
| :--- |


Source: TSG RAN WG1 Date: 8.4.2000

Subject: $\quad$ DPDCH/DPCCH gain factors

## Work item:

Category:
(only one category
shall be marked
with an X)

F Correction
A Corresponds to a correction in an earlier release
B Addition of feature
C Functional modification of feature
D Editorial modification

| $\mathbf{X}$ |
| :--- |
|  |
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|  |
|  |

Release: Phase 2 Release 96 Release 97 Release 98 Release 99 Release 00


Reason for Quantization values of the gain parameters in Table 1 are proposed to be specified as fraction change: values instead of decimal values to avoid possible rounding errors in the case when gain factors are computed.

Clauses affected: $\quad$ 4.2.1

| Other specs | Other 3G core specifications | $\rightarrow$ List of CRs: |
| :---: | :---: | :---: |
| affected: | Other GSM core specifications | $\rightarrow$ List of CRs: |
|  | MS test specifications | $\rightarrow$ List of CRs: |
|  | BSS test specifications | $\rightarrow$ List of CRs: |
|  | O\&M specifications | List of CR |

## Other

comments:
<-------- double-click here for help and instructions on how to create a CR.

### 4.2 Spreading

### 4.2.1 DPCCH/DPDCH

Figure 1 illustrates the principle of the uplink spreading of DPCCH and DPDCHs. The binary DPCCH and DPDCHs to be spread are represented by real-valued sequences, i.e. the binary value " 0 " is mapped to the real value +1 , while the binary value " 1 " is mapped to the real value -1 . The DPCCH is spread to the chip rate by the channelization code $c_{c}$, while the $n$ :th DPDCH called DPDCH $_{n}$ is spread to the chip rate by the channelization code $c_{d, n}$. One DPCCH and up to six parallel DPDCHs can be transmitted simultaneously, i.e. $1 \leq n \leq 6$.


Figure 1: Spreading for uplink DPCCH and DPDCHs
After channelization, the real-valued spread signals are weighted by gain factors, $\beta_{\mathrm{c}}$ for DPCCH and $\beta_{\mathrm{d}}$ for all DPDCHs.

At every instant in time, at least one of the values $\beta_{c}$ and $\beta_{d}$ has the amplitude 1.0. The $\beta$-values are quantized into 4 bit words. The quantization steps are given in table 1 .

Table 1: The quantization of the gain parameters

| Signalling values for <br> $\beta_{\mathrm{c}}$ and $\beta_{\mathrm{d}}$ | Quantized amplitude ratios <br> $\beta_{\mathrm{c}}$ and $\beta_{\mathrm{d}}$ |
| :--- | :--- |
| 15 | 1.0 |
| 14 | $0.933314 / 15$ |
| 13 | $0.866613 / 15$ |
| 12 | $0.800012 / 15$ |
| 11 | $0.733311 / 15$ |
| 10 | $0.666710 / 15$ |
| 9 | $0.60009 / 15$ |
| 8 | $0.53338 / 15$ |
| 7 | $0.4667 \overline{7 / 15}$ |
| 6 | $0.40006 / 15$ |
| 5 | $0.33335 / 15$ |
| 4 | $0.26674 / 15$ |
| 3 | $0.20003 / 15$ |
| 2 | $0.13332 / 15$ |
| 1 | $0.06671 / 15$ |
| 0 | Switch off |

After the weighting, the stream of real-valued chips on the I- and Q-branches are then summed and treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $\mathrm{S}_{\mathrm{dpch}, \mathrm{n}}$. The scrambling code is applied aligned with the radio frames, i.e. the first scrambling chip corresponds to the beginning of a radio frame.

