TSG-RAN Meeting #7 Madrid, Spain, 13 – 15 March 2000

Title: Agreed CRs to TS 25.222

Source: TSG-RAN WG1

Agenda item: 6.1.3

No.	Doc #	Spec	CR	Rev	Subject	Cat	Versio	Versio
1	R1-000082	25.222	017	-	Corrections to TS 25.222	F	3.1.1	3.2.0
2	R1-000081	25.222	018	-	Refinements of Physical Channel Mapping	F	3.1.1	3.2.0
3	R1-000193	25.222	019	1	TFCI coding specification in TDD	F	3.1.1	3.2.0
4	R1-000160	25.222	021	-	Modification of Turbo code internal interleaver	В	3.1.1	3.2.0
5	R1-000226	25.222	023	-	Update of TS 25.222 – clarification of BTFD for	F	3.1.1	3.2.0
6	R1-000237	25.222	025	-	Change of TFCI basis for TDD	F	3.1.1	3.2.0
7	R1-000255	25.222	026	-	Padding Function for Turbo coding of small blocks	В	3.1.1	3.2.0
8	R1-000282	25.222	027	-	Editorial modification of shifting parameter	D	3.1.1	3.2.0
9	R1-000437	25.222	029	1	Editorial changes of channel coding section	D	3.1.1	3.2.0

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<u>Reason for</u> <u>change:</u>	FDD: - Ir - M - C - H - C	 This CR includes the following corrections, mainly due to harmonisation reasons with FDD: Inclusion of flexible coding schemes for the FACH Modification of the chapter describing convolutional coding Clarification of the alignment of TrCHs with different TTI Handling of zero length transport blocks Clarification of the indices for timeslot related 2nd interleaving Furthermore, some minor editorial changes have been added. 							<i>i</i> ith
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3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

<acronym></acronym>	<explanation></explanation>
ARQ	Automatic Repeat on Request
BCH	Broadcast Channel
BER	Bit Error Rate
BS	Base Station
BSS	Base Station Subsystem
CBR	Constant Bit Rate
СССН	Common Control Channel
CCTrCH	Coded Composite Transport Channel
CDMA	Code Division Multiple Access
CFN	Connection Frame Number
CRC	Cyclic Redundancy Check
DCA	Dynamic Channel Allocation
DCCH	Dedicated Control Channel
DCH	Dedicated Channel
DL	Downlink
DRX	Discontinuous Reception
DSCH	Downlink Shared Channel
DTX	Discontinuous Transmission
FACH	Forward Access Channel
FDD	Frequency Division Duplex
FDMA	Frequency Division Multiple Access
FEC	Forward Error Control
	Frame Error Rate
FER GF	Galois Field
JD	Joint Detection
JD L1	
LI L2	Layer 1
	Layer 2
LLC	Logical Link Control
MA	Multiple Access
MAC	Medium Access Control
MS	Mobile Station
MT	Mobile Terminated Non-Real Time
NRT	
OVSF	Orthogonal Variable Spreading Factor
PC	Power Control
PCCC	Parallel Concatenated Convolutional Code
PCH	Paging Channel
PhCH	Physical Channel
PI	Paging Indicator
QoS	Quality of Service
QPSK	Quaternary Phase Shift Keying
RACH	Random Access Channel
RF	Radio Frequency
RLC	Radio Link Control
RRC	Radio Resource Control
RRM	Radio Resource Management
RSC	Recursive Systematic Convolutional Coder
RT	Real Time
RU	Resource Unit
SCCC	Serial Concatenated Convolutional Code
SCH	Synchronization Channel
SNR	Signal to Noise Ratio
TCH	Traffic channel
TDD	Time Division Duplex
TDMA	Time Division Multiple Access

Transport Format Combination
Transport Format Combination Indicator
Transmit Power Control
Transport Block
Transport Channel
Transmission Time Interval
User Equipment
Uplink
Universal Mobile Telecommunications System
Uplink Shared Channel
UMTS Terrestrial Radio Access
Variable Bit Rate

4.2 Transport channel coding/multiplexing

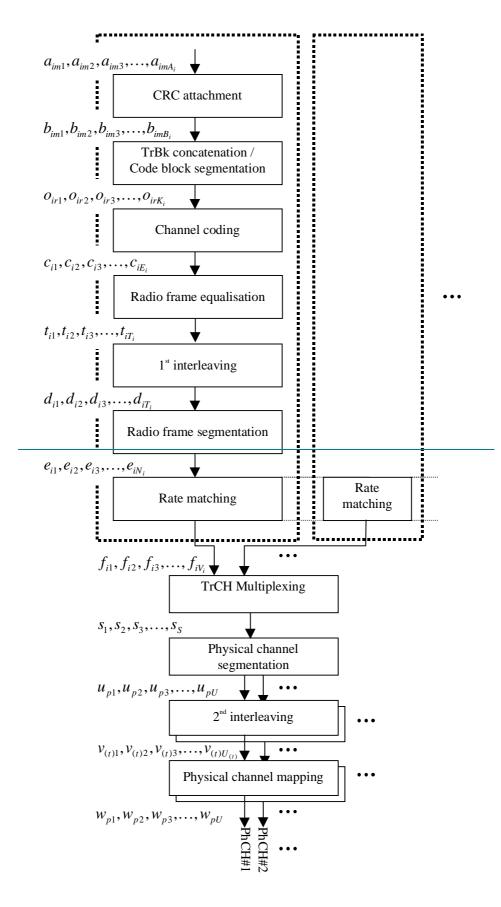
Figure 4-1 illustrates the overall concept of transport-channel coding and multiplexing. Data arrives to the coding/multiplexing unit in form of transport block sets, once every transmission time interval. The transmission time interval is transport-channel specific from the set {10 ms, 20 ms, 40 ms, 80 ms}.

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The following coding/multiplexing steps can be identified:

- Add CRC to each transport block (see section 4.2.1)
- TrBk concatenation / Code block segmentation (see section 4.2.2)
- Channel coding (see section 4.2.3)
- Radio frame size equalization (see section 4.2.4)
- Interleaving (two steps, see sections 4.2.5 and 4.2.10)
- Radio frame segmentation (4.2.6)
- Rate matching (see section 4.2.7)
- Multiplexing of transport channels (see section 4.2.8)
- Physical channel segmentation (see section 4.2.9)
- Mapping to physical channels (see section 4.2.11)

The coding/multiplexing steps for uplink and downlink are shown in figure 4-1.



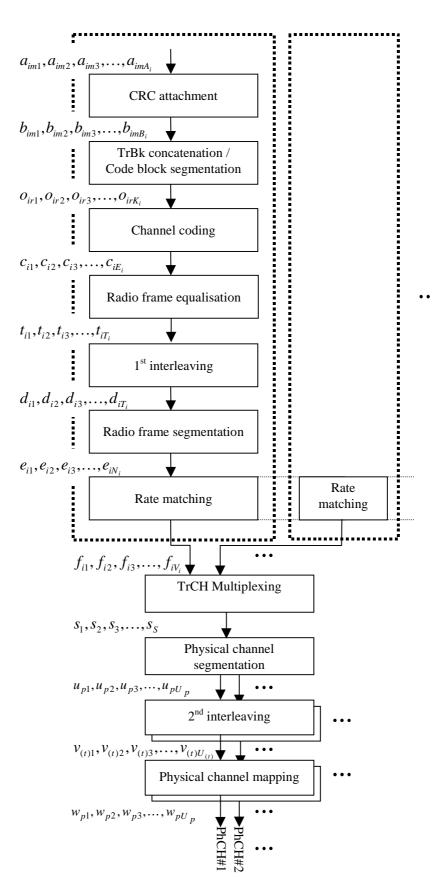


Figure 4–1: Transport channel multiplexing structure for uplink and downlink

CRC calculation 4.2.1.1

The entire transport block is used to calculate the CRC parity bits for each transport block. The parity bits are generated by one of the following cyclic generator polynomials:

$$g_{CRC24}(D) = D^{24} + D^{23} + D^6 + D^5 + D + 1$$
$$g_{CRC16}(D) = D^{16} + D^{12} + D^5 + 1$$
$$g_{CRC12}(D) = D^{12} + D^{11} + D^3 + D^2 + D + 1$$
$$g_{CRC8}(D) = D^8 + D^7 + D^4 + D^3 + D + 1$$

~

Denote the bits in a transport block delivered to layer 1 by $a_{im1}, a_{im2}, a_{im3}, \dots, a_{imA_i}$, and the parity bits by

 $p_{im1}, p_{im2}, p_{im3}, \dots, p_{imL_i}$. A_i is the length of a transport block of TrCH *i*, *m* is the transport block number, and L_i is 24, 16, <u>12</u>, <u>8</u>, or 0 depending on what is signalled from higher layers.

The encoding is performed in a systematic form, which means that in GF(2), the polynomial

$$a_{im1}D^{A_i+23} + a_{im2}D^{A_i+22} + \dots + a_{imA_i}D^{24} + p_{im1}D^{23} + p_{im2}D^{22} + \dots + p_{im23}D^1 + p_{im24}D^{24}$$

yields a remainder equal to 0 when divided by $g_{CRC24}(D)$, polynomial

$$a_{im1}D^{A_i+15} + a_{im2}D^{A_i+14} + \dots + a_{imA_i}D^{16} + p_{im1}D^{15} + p_{im2}D^{14} + \dots + p_{im15}D^1 + p_{im16}D^1$$

yields a remainder equal to 0 when divided by $g_{CRC16}(D)$, polynomial

$$a_{im1}D^{A_i+11} + a_{im2}D^{A_i+10} + \dots + a_{imA_i}D^{12} + p_{im1}D^{11} + p_{im2}D^{10} + \dots + p_{im7}D^1 + p_{im12}$$

$$a_{im1}D^{A_i+11} + a_{im2}D^{A_i+10} + \dots + a_{imA_i}D^{12} + p_{im1}D^{11} + p_{im2}D^{10} + \dots + p_{im11}D^1 + p_{im12}$$

yields a remainder equal to 0 when divided by g_{CRC12}(D) and the polynomial

$$a_{im1}D^{A_i+7} + a_{im2}D^{A_i+6} + \dots + a_{imA_i}D^8 + p_{im1}D^7 + p_{im2}D^6 + \dots + p_{im7}D^1 + p_{im8}$$

yields a remainder equal to 0 when divided by $g_{CRC8}(D)$.

If no transport blocks are input to the CRC calculation ($M_i = 0$), no CRC attachment shall be done.

4.2.2.2 Code block segmentation

NOTE: It is assumed that filler bits are set to 0.

Segmentation of the bit sequence from transport block concatenation is performed if $X_i > Z$. The code blocks after segmentation are of the same size. The number of code blocks on TrCH *i* is denoted by C_i . If the number of bits input to the segmentation, X_i , is not a multiple of C_i , filler bits are added to the last block. The filler bits are transmitted and they are always set to 0. The maximum code block sizes are:

convolutional coding: Z = 504

turbo coding: Z = 5114

no channel coding: Z = unlimited

The bits output from code block segmentation are denoted by $o_{ir1}, o_{ir2}, o_{ir3}, \dots, o_{irK_i}$, where *i* is the TrCH number, *r* is the code block number, and K_i is the number of bits.

Number of code blocks: $C_i = [X_i / Z]$

Number of bits in each code block: $K_i = [X_i / C_i]$

Number of filler bits: $Y_i = C_i K_i - X_i$

If $X_i \leq Z$, then $O_{i1k} = x_{ik}$, and $K_i = X_i$.

If $X_i \ge Z$, then

 $o_{i1k} = x_{ik} \qquad k = 1, 2, ..., K_i$ $o_{i2k} = x_{i,(k+K_i)} \qquad k = 1, 2, ..., K_i$ $o_{i3k} = x_{i,(k+2K_i)} \qquad k = 1, 2, ..., K_i$... $o_{iC_ik} = x_{i(k+(C_i-1)K_i)} \qquad k = 1, 2, ..., K_i - Y_i$ $o_{iC_ik} = 0 \qquad k = (K_i - Y_i) + 1, (K_i - Y_i) + 2, ..., K_i$

4.2.3 Channel coding

Code blocks are delivered to the channel coding block. They are denoted by $O_{ir1}, O_{ir2}, O_{ir3}, \dots, O_{irK_i}$, where *i* is the TrCH number, *r* is the code block number, and K_i is the number of bits in each code block. The number of code blocks on TrCH *i* is denoted by C_i . After encoding the bits are denoted by $y_{ir1}, y_{ir2}, y_{ir3}, \dots, y_{irY_i}$. The encoded blocks are serially multiplexed so that the block with lowest index *r* is output first from the channel coding block. The bits output are denoted by $C_{i1}, C_{i2}, C_{i3}, \dots, C_{iE_i}$, where *i* is the TrCH number and $E_i = C_i Y_i$. The output bits are defined by the following relations:

$$c_{ik} = y_{i1k} \quad k = 1, 2, ..., Y_i$$

$$c_{ik} = y_{i,2,(k-Y_i)} \quad k = Y_i + 1, Y_i + 2, ..., 2Y_i$$

$$c_{ik} = y_{i,3,(k-2Y_i)} \quad k = 2Y_i + 1, 2Y_i + 2, ..., 3Y_i$$
...

 $c_{ik} = y_{i,C_i,(k-(C_i-1)Y_i)}$ $k = (C_i-1)Y_i + 1, (C_i-1)Y_i + 2, ..., C_iY_i$

The relation between O_{irk} and Y_{irk} and between K_i and Y_i is dependent on the channel coding scheme.

The following channel coding schemes can be applied to transport channels:

- Convolutional coding
- Turbo coding
- No channel coding

The values of Y_i in connection with each coding scheme:

- Convolutional coding, $\frac{1}{2}$ rate: $Y_i = 2*K_i + 16$; $\frac{1}{3}$ rate: $Y_i = 3*K_i + 24$
- Turbo coding, 1/3 rate: $Y_i = 3*K_i + 12$
- No channel coding, $Y_i = K_i$

Table 4.2.3-1: Error Correction Coding Parameters

Transport channel type	Coding scheme	Coding rate
BCH		1/0
PCH	Convolutional code	<u>1/2</u>
RACH		
		<u>1/3, 1/2</u>
DCH, DSCH, USCH, FACH	Turbo code	<u>1/3</u>
	No coding	

Table 4.2.3-1: Error Correction Coding Parameters

Transport channel type	Coding scheme	Coding rate
BCH		
PCH	Convolutional and	1/2
FACH	Convolutional code	
RACH		
		1/3, 1/2
DCH, DSCH, USCH	Turbo code	1/3
	No coding	

If no code blocks are input to the channel coding ($C_i = 0$), no bits shall be output from the channel coding, i.e. $E_i = 0$.

4.2.3.1 Convolutional Coding

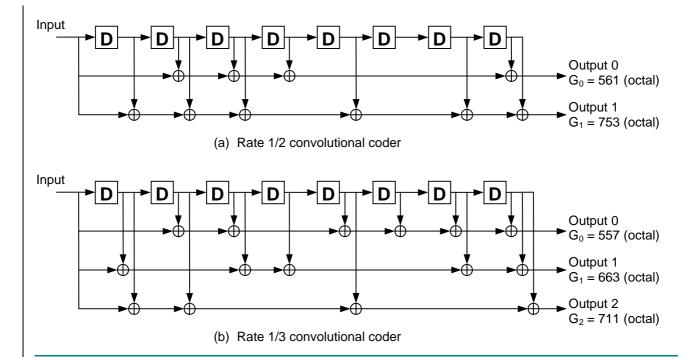
Convolutional codes with constraint length 9 and coding rates 1/3 and 1/2 are defined.

The configuration of the convolutional coder is presented in figure 3.

<u>Output from the rate 1/3 convolutional coder shall be done in the order output0, output1, output2, output0, output1, output2, output2. Output from the rate 1/2 convolutional coder shall be done in the order output 0, output 1, output 0, ..., output 1.</u>

8 tail bits with binary value 0 shall be added to the end of the code block before encoding.

The initial value of the shift register of the coder shall be "all 0" when starting to encode the input bits.



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Figure 3: Rate 1/2 and rate 1/3 convolutional coders

- Constraint length K=9. Coding rates 1/2 and 1/3.
- The configuration of the convolutional coder is presented in figure 4-2.
- The output from the convolutional coder shall be done in the order output0, output1,output2, output0, output1,..., output2. (When coding rate is 1/2, output is done up to output 1).
- The initial value of the shift register of the coder shall be "all 0".
- K 1 tail bits (value 0) shall be added to the end of the code block before encoding.

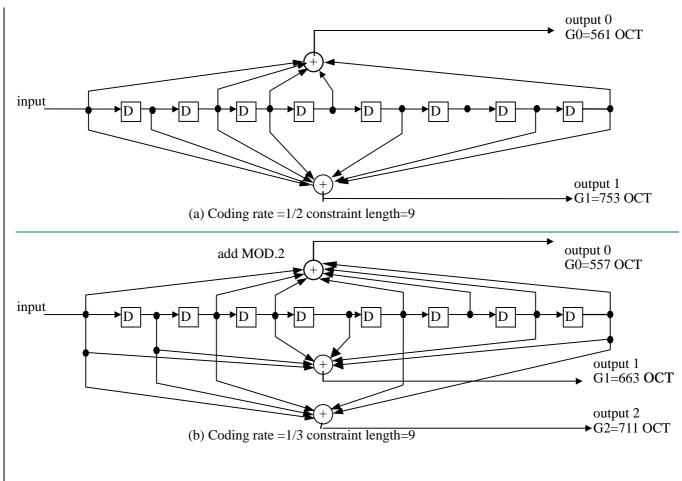


Figure 4-2: Convolutional Coder

4.2.3.2 Turbo coding

4.2.3.2.1 Turbo coder

The turbo coding scheme is a parallel concatenated convolutional code (PCCC) with 8-state constituent encoders.

For data services requiring quality of service between 10⁻³ and 10⁻⁶ BER inclusive, parallel concatenated convolutional code (PCCC) with 8 state constituent encoders is used.

The transfer function of the 8-state constituent code for PCCC is

$$\mathbf{G}(\mathbf{D}) = \left[1, \frac{n(D)}{d(D)}\right]$$

where,

$$d(D)=1+D^2+D^3$$

 $n(D)=1+D+D^3$.

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4.2.7 Rate matching

Rate matching means that bits on a TrCH are repeated or punctured. Higher layers assign a rate-matching attribute for each TrCH. This attribute is semi-static and can only be changed through higher layer signalling. The rate-matching attribute is used when the number of bits to be repeated or punctured is calculated.

The number of bits on a TrCH can vary between different transmission time intervals. When the number of bits between different transmission time intervals is changed, bits are repeated to ensure that the total bit rate after TrCH multiplexing is identical to the total channel bit rate of the allocated physical channels.

If no bits are input to the rate matching for all TrCHs within a CCTrCH, the rate matching shall output no bits for all TrCHs within the CCTrCH.

Notation used in section 4.2.7 and subsections:

 N_{ij} :_____Number of bits in a radio frame before rate matching on TrCH *i* with transport format combination *j*.

 ΔN_{ij} : If positive – number of bits to be repeated in each radio frame on TrCH *i* with transport format combination *j*.

If negative – number of bits to be punctured in each radio frame on TrCH i with transport format combination j.

- *RM_i*: ____Semi-static rate matching attribute for TrCH *i*. Signalled from higher layers.
- *PL:* ____Puncturing limit. This value limits the amount of puncturing that can be applied in order to minimise the _____number of physical channels. Signalled from higher layers.
- $N_{data,j}$: Total number of bits that are available for a CCTrCH in a radio frame with transport format combination j.
- P: number of physical channels used in the current frame
- P_{max} : maximum number of physical channels <u>allocated</u> for a CCTrCH.
- <u> U_p </u>: Number of data bits in the physical channel p with p = 1...P
- *I:* ____Number of TrCHs in a CCTrCH.
- Z_{mij} : ____Intermediate calculation variable.
- *F_i*: ____Number of radio frames in the transmission time interval of TrCH *i*.
- *n_i*: _____Radio frame number in the transmission time interval of TrCH *i* ($0 \le n_i < F_i$).
- *q:* —Average puncturing or repetition distance(normalised to only show the remaining rate matching on top of an integer number of repetitions).
- $I_F(n_i)$: The inverse interleaving function of the 1st interleaver (note that the inverse interleaving function is identical to the interleaving function itself for the 1st interleaver).
- $S(n_i)$: The shift of the puncturing or repetition pattern for radio frame n_i .
- $TF_i(j)$: Transport format of TrCH i for the transport format combination j.
- TFS(i): The set of transport format indexes l for TrCH i.
- e_{ini}: Initial value of variable e in the rate matching pattern determination algorithm of section 4.2.7.3.
- e_{plus} Increment of variable *e* in the rate matching pattern determination algorithm of section 4.2.7.3.
- e_{minus} Decrement of variable *e* in the rate matching pattern determination algorithm of section 4.2.7.3.
- *b:* Indicates systematic and parity bits.

b=01: Systematic bit. X(t) in 4.2.3.2.1.

<u>Y:</u> $b=42: 1^{st}$ parity bit (from the upper Turbo constituent encoder). Y(t) in section 4.2.3.2.1.

<u>Y'</u>: $b=23: 2^{nd}$ parity bit (from the lower Turbo constituent encoder). Y'(t) in section 4.2.3.2.1.

4.2.7.1 Determination of rate matching parameters

The following relations, defined for all TFC *j*, -are used when calculating the rate matching pattern:

$$Z_{0,i} = 0$$

$$Z_{ij} = \begin{bmatrix} \sum_{m=1}^{i} RM_m \cdot N_{mj} \\ \sum_{m=1}^{l} RM_m \cdot N_{mj} \end{bmatrix} \text{ for all } i = 1 \dots I$$

$$\Delta N_{ij} = Z_{ij} - Z_{i-1,j} - N_{ij} \quad \text{for all } i = 1 \dots I$$

Puncturing can be used to minimise the required transmission capacity. The maximum amount of puncturing that can be applied is signalled from higher layers and denoted by PL. The possible values for N_{data} depend on the number of physical channels P_{max} , allocated to the respective CCTrCH, and on their characteristics (spreading factor, length of midamble and TFCI, usage of TPC and multiframe structure), which is given in [7].

Denote the number of data bits in each physical channel by $N\underline{U}_{pk,Skp}$, where kp refers to the sequence number $1 \le kp \le P_{max}$ of this physical channel in the allocation message, and the second index Skp indicates the spreading factor with the possible values $\{16, 8, 4, 2, 1\}$, respectively. For each physical channel an individual minimum spreading factor Skp_{min} is transmitted by means of the higher layer. Then, for N_{data} one of the following values in ascending order can be chosen: $-\{N_{1,16}, ..., N_{1,SImin}, N_{1,SImin} + N_{2,S2min}, ..., N_{1,SImin} + N_{2,S2min} + ... + N_{p,16}, ..., N_{1,SImin} + N_{2,S2min} + ... + N_{p,26}, ..., N_{1,SImin} + N_{2,S2min} + ... + N_{p,16}, ..., N_{1,SImin} + N_{2,S2min} + ... + N_{p,SPmin}$

$$\left\{U_{1,16},...,U_{1,S1_{\min}},U_{1,S1_{\min}}+U_{2,16},...,U_{1,S1_{\min}}+U_{2,S2_{\min}},...,U_{1,S1_{\min}}+U_{2,S2_{\min}}+...+U_{P_{\max},16},...,U_{1,S1_{\min}}+U_{2,S2_{\min}}+...+U_{P_{\max},(SP_{\max},M_{1,S1_{\min}})}\right\}$$

N_{data, i} for the transport format combination j is determined by executing the following algorithm:

SET1 = { N_{data} such that
$$N_{data} - PL \cdot \sum_{x=1}^{I} \frac{RM_x}{\min_{1 \le y \le I} \{RM_y\}} \cdot N_{x,j}$$
 is non negative }

 $N_{data, i} = min SET1$

The number of bits to be repeated or punctured, ΔN_{ij} , within one radio frame for each TrCH i is calculated with the relations given at the beginning of this section for all possible transport format combinations j and selected every radio frame.

If $\Delta N_{ij} = 0$ then the output data of the rate matching is the same as the input data and the rate matching algorithm of section 4.2.7.3 does not need to be executed.

Otherwise, the rate matching pattern is calculated with the algorithm described in section 4.2.7.3. For this algorithm the parameters e_{ini} , e_{plus} , e_{minus} , and X_i are needed, which are calculated according to the equations in section 4.2.7.1.1 and 4.2.7.1.2

4.2.7.3 Rate matching pattern determination

The bits input to the rate matching are denoted by $x_{i1}, x_{i2}, x_{i3}, \dots, x_{iX_i}$, where *i* is the TrCH and X_i is the parameter given in section 4.2.7.1.1 and 4.2.7.1.2. The bits output from the rate matching are denoted by $f_{i1}, f_{i2}, f_{13}, \dots, f_{iV_i}$, where *i* is the TrCH number and $V_i = N + \Delta N$.

Note that the transport format combination number j for simplicity has been left out in the bit numbering.

The rate matching rule is as follows:

if puncturing is to be performed

e = e_{ini} -- initial error between current and desired puncturing ratio

m = 1 -- index of current bit

do while $m \le X_i$

 $e = e - e_{minus}$ -- update error

if e <= 0 then -- check if bit number m should be punctured

set bit $x_{i,m}$ to δ where $\delta \notin \{0, 1\}$

 $e = e + e_{plus}$ -- update error

end if

m = m + 1 -- next bit

end do

```
else
```

e = e_{ini} -- initial error between current and desired puncturing ratio

m = 1 -- index of current bit

do while $m \ll X_i$

 $e = e - e_{minus}$ -- update error

do while e <= 0 -- check if bit number m should be repeated

repeat bit $x_{i,m}$

 $e = e + e_{plus}$ -- update error

end do

m = m + 1 -- next bit

```
end do
```

end if

A repeated bit is placed directly after the original one.

4.2.10 2nd interleaving

The 2nd interleaving can be applied jointly to all data bits transmitted during one frame, or separately within each timeslot, on which the CCTrCH is mapped. The selection of the 2nd interleaving scheme is controlled by higher layer.

4.2.10.1 Frame related 2nd interleaving

In case of frame related interleaving, the bits input to the 2nd interleaver are denoted $x_1, x_2, x_3, ..., x_U$, where *U* is the total number of bits after TrCH multiplexing transmitted during the respective radio frame with $S = U = \sum U_p$.

The relation between x_k and the bits u_{pk} in the respective physical channels is given below:

$$x_{k} = u_{1k} \quad k = 1, 2, ..., U_{1}$$
$$x_{(k+U_{1})} = u_{2k} \quad k = 1, 2, ..., U_{2}$$
$$...$$
$$x_{(k+U_{1}+...+U_{p-1})} = u_{Pk} \quad k = 1, 2, ..., U_{P}$$

The following steps have to be performed once for each CCTrCH:

- (1) Set the number of columns $C_2 = 30$. The columns are numbered 0, 1, 2, ..., C_2 -1 from left to right.
- (2) Determine the number of rows R_2 by finding minimum integer R_2 such that $U \le R_2C_2$.
- (3) The bits input to the 2^{nd} interleaving are written into the $R_2 \times C_2$ rectangular matrix row by row.

x_1	x_2	x_3	x ₃₀
<i>x</i> ₃₁	<i>x</i> ₃₂	<i>x</i> ₃₃	x ₆₀
	:	:	:
$x_{(R_2-1)30+1}$	$x_{(R_2-1)30+2}$	$X_{(R_2-1)30+3}$	$\dots x_{R_2 \cdot 30}$

(4) Perform the inter-column permutation based on the pattern $\{P_2(j)\}$ $(j = 0, 1, ..., C_2-1)$ that is shown in table 4.2.9-1, where $P_2(j)$ is the original column position of the j-th permuted column. After permutation of the columns, the bits are denoted by y_k .

 $\begin{bmatrix} y_1 & y_{R_2+1} & y_{2R_2+1} & \cdots & y_{29R_2+1} \\ y_2 & y_{R_2+2} & y_{2R_2+2} & \cdots & y_{29R_2+2} \\ \vdots & \vdots & \vdots & & \vdots \\ y_{R_2} & y_{2R_2} & y_{3R_2} & \cdots & y_{30R_2} \end{bmatrix}$

(5) The output of the 2nd interleaving is the bit sequence read out column by column from the inter-column permuted $R_2 \times C_2$ matrix. The output is pruned by deleting bits that were not present in the input bit sequence, i.e. bits y_k that corresponds to bits x_k with k>U are removed from the output. The bits after 2nd interleaving are denoted by v_1, v_2, \ldots, v_U , where v_1 corresponds to the bit y_k with smallest index k after pruning, v_2 to the bit y_k with second smallest index k after pruning, and so on.

4.2.10.2 Timeslot related 2nd interleaving

In case of timeslot related 2^{nd} interleaving, the bits input to the 2^{nd} interleaver are denoted $x_{t1}, x_{t2}, x_{t3}, \dots, x_{tU_t}$, where *t* refers to a certain timeslot, and U_t is the number of bits transmitted in this timeslot during the respective radio frame

In each timeslot *t* the relation between x_{tk} and u_{tpk} is given below with P_t referring to the number of physical channels within the respective timeslot:

The following steps have to be performed for each timeslot *t*, on which the respective CCTrCH is mapped:

- (1) Set the number of columns $C_2 = 30$. The columns are numbered 0, 1, 2, ..., C_2 -1 from left to right.
- (2) Determine the number of rows R_2 by finding minimum integer R_2 such that $U_t \leq R_2 C_2$.
- (3) The bits input to the 2^{nd} interleaving are written into the $R_2 \times C_2$ rectangular matrix row by row.

X_{t1}	x_{t2}	x_{t3}	x_{t30}
<i>x</i> _{t31}	x_{t32}	x_{t33}	X_{t60}
:	÷	÷	:
$X_{t,((R_2-1)30+1)}$	$x_{t,((R_2-1)30+2)}$	$x_{t,((R_2-1)30+3)}$	$\ldots X_{t,(R_230)}$

(4) Perform the inter-column permutation based on the pattern $\{P_2(j)\}$ $(j = 0, 1, ..., C_2-1)$ that is shown in table 4.2.9-1, where $P_2(j)$ is the original column position of the *j*-th permuted column. After permutation of the columns, the bits are denoted by y_{tk} .

y_{t1}	$\mathcal{Y}_{t,(R_2+1)}$	$\mathcal{Y}_{t,(2R_2+1)}$	$\cdots y_{t,(29R_2+1)}$
y_{t2}	$\mathcal{Y}_{t,(R_2+2)}$	$\mathcal{Y}_{t,(2R_2+2)}$	$\cdots \mathcal{Y}_{t,(29R_2+2)}$
:	÷	:	$\cdots \mathcal{Y}_{t,(29R_2+2)}$ $\cdots \qquad \vdots$
y_{tR_2}	$\mathcal{Y}_{t,(2R_2)}$	$y_{t,(3R_2)}$	

(5) The output of the 2nd interleaving is the bit sequence read out column by column from the inter-column permuted $R_2 \times C_2$ matrix. The output is pruned by deleting bits that were not present in the input bit sequence, i.e. bits y_{tk} that corresponds to bits x_{tk} with $k>U_t$ are removed from the output. The bits after 2nd interleaving are denoted by

4.2.12 Multiplexing of different transport channels onto one CCTrCH, and mapping of one CCTrCH onto physical channels

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Different transport channels can be encoded and multiplexed together into one Coded Composite Transport Channel (CCTrCH). The following rules shall apply to the different transport channels which are part of the same CCTrCH:

1) Transport channels multiplexed into one CCTrCh shouldall have co-ordinated timings in the sense that transport blocks arriving from higher layers on different transport channels of potentially different transmission time intervals shall have aligned transmission time instants as shown in figure 4-6. When the TFCS of a CCTrCH is changed because a transport channel *i* is added to the CCTrCH or reconfigured within the CCTrCH, the TTI of transport channel *i* may only start in radio frames with CFN fulfilling the relation

$\underline{CFN_i \mod F_{max} = 0}$,

where F_{max} denotes the maximum number of radio frames within the transmission time intervals of all transport channels which are multiplexed into the same CCTrCH, including transport channel *i* which is added or reconfigured, and CFN_i denotes the connection frame number of the first radio frame within the transmission time interval of transport channel *i*.

After addition or reconfiguration of a transport channel *i* within a CCTrCH, the TTI of transport channel *i* may only start in radio frames with CFN fulfilling the relation

 $\underline{CFN_i \mod F_i = 0}$.

2) Different CCTrCHs cannot be mapped onto the same physical channel.

3) One CCTrCH shall be mapped onto one or several physical channels.

								Poss	ble trar	ismissi	on time	instan	ts					
Transmission- time intervals	0 ms	10 m	ns 20 m	ns 30 m	ns 40	ms 50	ms 60	ms 70	ms 80	ms 9	0 ms 100	ms 110	ms 120) ms 130) ms 140	ms 150	ms160	ms
10 ms														<u>.</u>				
20 ms	Į	Ī		Ī					[
40 ms																		
80 ms														[
	T									T								•

•: Allowed transmission time instants

Figure 4-6: Possible transmission time instants regarding CCTrCH

- 4) Dedicated Transport channels and common transport channels cannot be multiplexed into the same CCTrCH.
- 5) For the common transport channels, only the FACH and PCH may belong to the same CCTrCH.
- 6) Each CCTrCH carrying a BCH shall carry only one BCH and shall not carry any other Transport Channel.
- 7) Each CCTrCH carrying a RACH shall carry only one RACH and shall not carry any other Transport Channel.

Hence, there are two types of CCTrCH

CCTrCH of dedicated type, corresponding to the result of coding and multiplexing of one or several DCH.

CCTrCH of common type, corresponding to the result of the coding and multiplexing of a common channel, i.e. RACH and USCH in the uplink and DSCH, BCH, FACH or PCH in the downlink, respectively.

Transmission of TFCI is possible for CCTrCH containing Transport Channels of:

- Dedicated type
- USCH type
- DSCH type
- FACH and/or PCH type

e.g. for 3GPP use the format TP-99xxx or for SMG, use the format P-99-xxx

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4.2.11 Physical channel mapping

The PhCH for both uplink and downlink is defined in [6]. The bits after physical channel mapping are denoted by $w_{p1}, w_{p2}, \dots, w_{pU_p}$, where p is the PhCH number and U_p is the number of bits in one radio frame for the respective

PhCH. The bits W_{pk} are mapped to the PhCHs so that the bits for each PhCH are transmitted over the air in ascending order with respect to k.

The mapping of the bits $v_{(t)1}, v_{(t)2}, ..., v_{(t)U_{(t)}}$ is performed like block interleaving, writing the bits into columns, but a PhCH with an odd number is filled in forward order, were as a PhCH with an even number is filled in reverse order.

The mapping scheme, as described in the following subsection, shall be applied individually for each timeslot t used in the current frame. Therefore, the bits $v_{t1}, v_{t2}, ..., v_{tU_t}$ are assigned to the bits of the physical channels

 $w_{t1,1...U_{t1}}, w_{t2,1...U_{t2}}, ..., w_{tP_t,1...U_{tP_t}}$ in each timeslot.

In uplink there are at most two codes allocated ($P\leq2$). If there is only one code, the same mapping as for downlink is applied. Denote SF1 and SF2 the spreading factors used for code 1 and 2, respectively. For the number of consecutive bits to assign per code bs_k the following rule is applied:

if

 $\frac{SF1 \ge SF2 \text{ then } bs_1 = 1 \text{ ; } bs_2 = SF1/SF2 \text{ ;}}{else}$ $\frac{SF2 \ge SF1 \text{ then } bs_1 = SF2/SF1 \text{ ; } bs_2 = 1 \text{ ;}}{end if}$

In the downlink case bs_p is 1 for all physical channels.

4.2.11.1 Mapping scheme

Notation used in this section:

<u>*P*</u>: number of physical channels for timeslot t, $P_t = 1..2$ for uplink; $P_t = 1...16$ for downlink

 U_{tp} : capacity in bits for the physical channel p in timeslot t

 U_t : total number of bits to be assigned for timeslot t

<u>bs_p:</u> number of consecutive bits to assign per code

for downlink all $bs_p = 1$

for uplink if SF1 >= SF2 then $bs_1 = 1$; $bs_2 = SF1/SF2$;

if SF2 > SF1 then $bs_1 = SF2/SF1$; $bs_2 = 1$;

<u>fbp</u>: number of already written bits for each code

pos: intermediate calculation variable

```
for p=1 to P<sub>t</sub> -- reset number of already written bits for every physical channel
```

 $\frac{fb_p = 0}{for}$

end for

<u>p = 1</u> -- start with PhCH #1

for k=1 to U_{t} .

```
do while (fb_p == U_{tp})-- physical channel filled up already ?p = ((p + 1) \mod (P_1 + 1)) + 1;end do
```

 $if (p \mod 2) == 0$

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$\underline{\text{pos} = U_{\underline{tp}} - \text{fb}_{\underline{p}}}$	reverse order
else	
$\underline{\qquad pos = fb_p + 1}$	forward order
endif	
$w_{tp,pos} = v_{t,k}$	assignment
	Increment number of already written bits
<u>if $(fb_p \mod bs_p) == 0$</u> <u>$p = ((p + 1) \mod (P_t + 1)) + 1;$</u> end if	Conditional change to the next physical channel
end for	
The mapping scheme depends on the 4.2.11.1 Mapping scheme after fran 4.2.11.1.1 Mapping scheme after fran	ne related 2 nd interleaving
In unlink there are at most two codes	allocated ($P\leq2$). If there is only one code, the same mapping as for downlink is
applied, see section 6.2.11.1.2. Denot	e SF1 and SF2 the spreading factors used for code 1 and 2, respectively. Then adding factors s1: $s2 = SF2$: SF1, where the smallest possible integers are used for
The following mapping rule is applied	1:
Bits are mapped on the first PhCH (ir	$\frac{1}{1} \text{ forward order) if } (k - 1) \mod (s1 + s2) = 0, \dots, s1 - 1;$
$-\mathcal{W}_{1,(k\operatorname{div}(s1+s2))\cdot s1+k\operatorname{mod}(s1+s2)} = \mathcal{V}_k$	
else bits are mapped on the second Pl	CH (in reverse order):
$\mathcal{W}_{2,U_2-(kdiv(s1+s2))\cdot s2+k\mathrm{mod}(s1+s2)-s1}=\mathcal{V}_k$	
	k=1 and increasing k until one of the PhCH is completely filled. From then on, the CH which has not been filled in the same order (forward or reverse depending on PhCH.
4.2.11.1.2 Mapping scheme after fram	me related 2nd interleaving in downlink
The mapping is equivalent to block ir forward order, were as a PhCH with a	nterleaving, writing in colomns, but a PhCH with an odd number is filled in an even number is filled in reverse order.
The following mapping rule is applied	1:
Bits are mapped on an odd numbered	PhCH (in forward order) according to the following rule, if (k mod P)+1 is odd:
$w_{k \bmod P+1, k \operatorname{div} P} = v_k$	
Bits are mapped on an even numbered	HPhCH (in reverse order) according to the following rule, if (k mod P)+1 is even:
$\frac{W_k \mod P + 1, U_P - 1 - k \operatorname{div} P}{V_k} = V_k$	
This formula is applied starting with From then on, the remaining bits are on the PhCH) as previously on these	k=1 and increasing k until all the PhCHs which carry TFCI are completely filled. mapped on the remaining PhCHs in the same order (forward or reverse depending PhCHs.

4.2.11.2 Mapping scheme after timeslot related 2nd interleaving

For each timeslot only those physical channels with $p = 1, 2, ..., P_t$ are considered respectively, which are transmitted in that timeslot, and the following mapping scheme is applied:

6.2.11.2.1 Mapping scheme after timeslot related 2nd interleaving in uplink

In uplink there are at most two codes allocated ($P\leq 2$). If there is only one code, the same mapping as for downlink is applied, see section 6.2.11.1.2. Denote SF1 and SF2 the spreading factors used for code 1 and 2, respectively. Then denote the inverse relation of the spreading factors s1: s2 = SF2: SF1, where the smallest possible integers are used for s1 and s2.

The following mapping rule is applied:

Bits are mapped on the first PhCH (in forward order) if $(k \ 1)mod(s1+s2) = 0, ..., s1 \ 1$:

 $-\frac{W_{1,(k\,div(s1+s2))\cdot s1+k\,\mathrm{mod}\,(s1+s2)}}{V_{tk}} = \frac{V_{tk}}{V_{tk}}$

else bits are mapped on the second PhCH (in reverse order):

 $-\mathcal{W}_{2,U_2-(k\,div(s1+s2))\cdot s2+k\,\mathrm{mod}\,(s1+s2)-s1} = \mathcal{V}_{tk}$

This formula is applied starting with k=1 and increasing k until one of the PhCH is completely filled. From then on, the remaining bits are mapped on the PhCH which has not been filled in the same order (forward or reverse depending on the PhCH) as used previously on that PhCH.

6.2.11.2.2 Mapping scheme after timeslot related 2nd interleaving in downlink

The mapping is equivalent to block interleaving, writing in colomns, but a PhCH with an odd number is filled in forward order, were as a PhCH with an even number is filled in reverse order.

The following mapping rule is applied:

Bits are mapped on an odd numbered PhCH (in forward order) according to the following rule, if (k mod P_t)+1 is odd:

 $W_{k \mod P_t+1, k \operatorname{div} P_t} = V_{tk}$

Bits are mapped on an even numbered PhCH (in reverse order) according to the following rule, if (k mod P_t)+1 is even:

 $\frac{W_{k \mod P_{t}+1, U_{P_{t}}-1-k \operatorname{div} P_{t}}}{W_{t}} = V_{tk}$

This formula is applied starting with k=1 and increasing k until all the PhCHs which carry TFCI are completely filled. From then on, the remaining bits are mapped on the remaining PhCHs in the same order (forward or reverse depending on the PhCH) as previously on these PhCHs.

e.g. for 3GPP use the format TP-99xxx or for SMG, use the format P-99-xxx

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	M _{i,0}	M _{i,1}	M _{i,2}	M _{i,3}	M _{I,4}	M _{i,5}	M _{i,6}	M _{i,7}	M _{i,8}	M _{i,9}
0	1	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0	0
2	1	1	1	0	0	0	0	0	0	1
3	1	0	0	1	0	0	1	0	1	1
3 4	1	1	0	1	0	0	0	0	0	1
			1	1	-		-	-		-
5	1	0			0	0	0	0	1	0
6	1	1	1	1	0	0	0	1	0	0
7	1	0	0	0	1	0	0	1	1	0
8	1	1	0	0	1	0	1	1	1	0
9	1	0	1	0	1	0	1	0	1	1
10	1	1	1	0	1	0	0	0	1	1
11	1	0	0	1	1	0	0	1	1	0
12	1	1	0	1	1	0	0	1	0	1
13	1	0	1	1	1	0	1	0	0	1
14	1	1	1	1	1	0	1	1	1	1
15	1	1	0	0	0	1	1	1	0	0
16	1	0	1	0	0	1	1	1	0	1
17	1	1	1	0	0	1	1	0	1	0
18	1	0	0	1	0	1	0	1	1	1
19	1	1	0	1	0	1	0	1	0	1
20	1	0	1	1	0	1	0	0	1	1
21	1	1	1	1	0	1	0	1	1	1
22	1	0	0	0	1	1	0	1	0	0
23	1	1	0	0	1	1	1	1	0	1
24	1	0	1	0	1	1	1	0	1	0
25	1	1	1	0	1	1	1	0	0	1
26	1	0	0	1	1	1	0	0	1	0
27	1	1	0	1	1	1	1	1	0	0
28	1	0	1	1	1	1	1	1	1	0
29	1	1	1	1	1	1	1	1	1	1
30	1	0	0	0	0	0	0	0	0	0
31	1	0	0	0	0	1	1	0	0	0

Table 4.3.1-1: Basis sequences for (32,10) TFCI code

Let's define the TFCI information bits as a_0 , a_1 , a_2 , a_3 , a_4 , a_5 , a_6 , a_7 , a_8 , a_9 (a_0 is LSB and a_9 is MSB). The TFCI information bits shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame.

The output code word bits b_i are given by:

$$b_i = \sum_{n=0}^{9} (a_n \times M_{i,n}) \mod 2$$

where i=0...31. N_{TFCI} =32.

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4.3.1.2 Coding of short TFCI lengths

4.3.1.2.1 Coding very short TFCIs by repetition

If the number of TFCI bits is 1 or 2, then repetition will be used for coding. In this case each bit is repeated to a total of 4 times giving 4-bit transmission ($N_{TFCI}=4$) for a single TFCI bit and 8-bit transmission ($N_{TFCI}=8$) for 2 TFCI bits. Let's define the TFCI information bit(s) as b_0 (or b_0 and b_1). The TFCI information bit(s) shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame. In the case of two TFCI bits denoted b_0 and b_1 the TFCI word shall be { b_0 , b_1 , b_0 , b_1 , b_0 , b_1 , b_0 , b_1 }}.

4.3.1.2.2 Coding short TFCIs using bi-orthogonal codes

If the number of TFCI bits is in the range 3 to 5 the TFCI bits are encoded using a (16, 5) bi-orthogonal (or first order Reed-Muller) code. The coding procedure is as shown in figure 4-8.

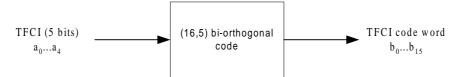


Figure 4-8: Channel coding of short length TFCI bits

The code words of the (16,5) bi-orthogonal code are linear combinations of 5 basis sequences as defined in table 4.3.1-2 below.

i	M _{i,0}	$M_{i,1}$	M _{i,2}	$M_{i,3}$	M _{i,4}
0	1	1	0	0	0
1	1	0	1	0	0
2	1	1	1	0	0
3	1	0	0	1	0
4	1	1	0	1	0
5	1	0	1	1	0
6	1	1	1	1	0
7	1	0	0	0	1
8	1	1	0	0	1
9	1	0	1	0	1
10	1	1	1	0	1
11	1	0	0	1	1
12	1	1	0	1	1
13	1	0	1	1	1
14	1	1	1	1	1
15	1	0	0	0	0

Table 4.3.1-2: Basis sequences for (16,5) TFCI code

Let's define the TFCI information bits as a_0 , a_1 , a_2 , a_3 , a_4 (a_0 is LSB and a_4 is MSB). The TFCI information bits shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame.

The output code word bits b_j are given by:

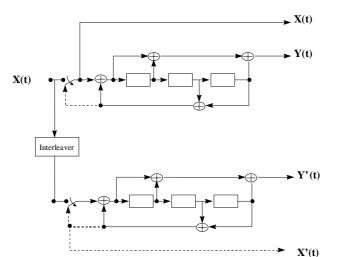
$$b_i = \sum_{n=0}^{4} (a_n \times M_{i,n}) \mod 2$$

where i=0...15. N_{TFCI} =16.

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Figure 4-3: Structure of the 8-state PCCC encoder (dotted lines effective for trellis termination only)

The initial value of the shift registers of the PCCC encoder shall be all zeros.

The output of the PCCC encoder is punctured to produce coded bits corresponding to the desired code rate. For rate 1/3, none of the systematic or parity bits are punctured, and the output sequence is X(0), Y(0), Y'(0), X(1), Y(1), Y'(1), etc.

4.2.3.2.2 Trellis termination in turbo code

Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are added after the encoding of information bits.

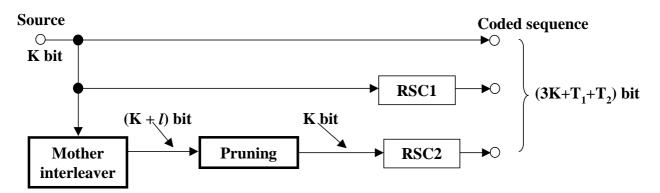
The first three tail bits shall be used to terminate the first constituent encoder (upper switch of figure 4-3 in lower position) while the second constituent encoder is disabled. The last three tail bits shall be used to terminate the second constituent encoder (lower switch of figure 4-3 in lower position) while the first constituent encoder is disabled.

The transmitted bits for trellis termination shall then be

X(t) Y(t) X(t+1) Y(t+1) X(t+2) Y(t+2) X'(t) Y'(t) X'(t+1) Y'(t+1) X'(t+2) Y'(t+2).

4.2.3.2.3 Turbo code internal interleaver

Figure 4-4 depicts the overall 8-State PCCC Turbo coding scheme including Turbo code internal interleaver. The Turbo code internal interleaver consists of mother interleaver generation and pruning. For arbitrary given block length K, one mother interleaver is selected from the 134-163 mother interleavers set. The generation scheme of mother interleaver is described in section 4.2.3.2.3.1. After the mother interleaver generation, *l*-bits are pruned in order to adjust the mother interleaver to the block length K. Tail bits T₁ and T₂ are added for constituent encoders RSC1 and RSC2, respectively. The definition of *l* is shown in section 4.2.3.2.3.2.





4.2.3.2.3.1 Mother interleaver generation

The interleaving consists of three stages. In first stage, the input sequence is written into the rectangular matrix row by row. The second stage is intra-row permutation. The third stage is inter-row permutation. The three-stage permutations are described as follows, the input block length is assumed to be K (320-40 to 5114 bits).

First Stage:

(1) Determine the number of rows R such that

$$R = 5 (K = 40 \text{ to } 159 \text{ bits})$$

R = 10 (K = 160 to 200 bits and 481 to 530 bits; Case 1)

- R = 20 (K = any other block lengths except 481 to 530 bits; Case 2)
- (2) Determine the number of columns C such that

<u>if K = 481 to 530 then</u>Case-1; C = p = 53

elseCase 2;

(i) find minimum prime p such that,

$$0 = <(p+1) - K/R$$

(ii) if $(0 = \langle p - K/R)$ then go to (iii)

else C = p + 1.

(iii) if (0 = then <math>C = p - 1.

else C = p.

(3) The input sequence of the interleaver is written into the $R \times C$ rectangular matrix row by row starting from row 0.

Second Stage:

A. If C = p

- (A-1) Select a primitive root g_0 from table 4.2.2-2.
- (A-2) Construct the base sequence c(i) for intra-row permutation as:

 $c(i) = [g_0 \times c(i-1)] \bmod p \ , \ i = 1,2,\ldots(p{\text -}2)., \ c(0) = 1.$

- (A-3) Select the minimum prime integer set $\{q_j\}$ (j = 1, 2, ..., R-1) such that
 - g.c.d{ q_i , p-1} = 1
 - $q_j > 6$

```
q_j > q_{(j-1)}
```

where g.c.d. is greatest common divider. And $q_0 = 1$.

(A-4) The set $\{q_i\}$ is permuted to make a new set $\{p_i\}$ such that

 $p_{P(j)} = q_j, \ j = 0, 1, \ \dots R-1,$

where P(j) is the inter-row permutation pattern defined in the third stage.

(A-5) Perform the *j*-th (j = 0, 1, 2, ..., C-1) intra-row permutation as:

 $c_i(i) = c([i \times p_i] \mod (p-1)), \quad i = 0, 1, 2, \dots, (p-2), \text{ and } c_i(p-1) = 0,$

where $c_j(i)$ is the input bit position of *i*-th output after the permutation of *j*-th row.

If C = p+1

- (B-1) Same as case A-1.
- (B-2) Same as case A-2.
- (B-3) Same as case A-3.
- (B-4) Same as case A-4.
- (B-5) Perform the *j*-th (j = 0, 1, 2, ..., R-1) intra-row permutation as:

 $c_i(i) = c([i \times p_i] \mod (p-1)), \quad i = 0, 1, 2, \dots, (p-2), c_j(p-1) = 0, \text{ and } c_j(p) = p,$

where $c_j(i)$ is the input bit position of *i*-th output after the permutation of *j*-th row.

(B-6) If (K = C × R) then exhange $c_{R-l}(p)$ with $c_{R-l}(0)$.

$$\underline{\text{If } C = p-1}$$

- (C-1) Same as case A-1.
- (C-2) Same as case A-2.
- (C-3) Same as case A-3.
- (C-4) Same as case A-4.
- (C-5) Perform the *j*-th (j = 0, 1, 2, ..., R-1) intra-row permutation as:

 $c_i(i) = c([i \times p_i] \mod (p-1)) - 1, i = 0, 1, 2, \dots, (p-2).,$

where $c_i(i)$ is the input bit position of *i*-th output after the permutation of *j*-th row.

Third Stage:

Perform the inter-row permutation based on the following P(j) (j = 0, 1, ..., R-1) patterns, where P(j) is the original row position of the *j*-th permuted row.

 P_A : {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11} for R = 20

 P_{B} : {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10} for R = 20

 P_{C} : {9, 8, 7, 6, 5, 4, 3, 2, 1, 0} for R = 10

 P_{D} : {4, 3, 2, 1, 0} for R = 5

The usage of these patterns is as follows:

Block length K: P(j)

40 to 159-bit: P_D

160 to 200-bit: P_C

201320 to 480-bit: P_A

- 481 to 530-bit: P_C
- 531 to 2280-bit: P_A
- 2281 to 2480-bit: P_B
- 2481 to 3160-bit: P_A
- 3161 to 3210-bit: P_B
- 3211 to 5114-bit: P_A

(2) The output of the mother interleaver is the sequence read out column by column from the permuted $R \times C$ matrix starting from column 0.

18

<u>p</u>	<u>g</u> _	<u>p</u>	<u>g</u> _	<u>p</u>	<u>g_</u>	<u>p</u>	<u>g_</u>	p	<u>g</u> _
<u>7</u>	<u>3</u>	<u>47</u>	<u>5</u>	<u>101</u>	<u>2</u>	<u>157</u>	<u>5</u>	<u>223</u>	<u>3</u>
<u>11</u>	<u>2</u>	<u>53</u>	<u>2</u>	<u>103</u>	<u>5</u>	<u>163</u>	<u>2</u>	<u>227</u>	<u>2</u>
<u>13</u>	2	<u>59</u>	2	<u>107</u>	2	<u>167</u>	5	<u>229</u>	<u>6</u>
<u>17</u>	<u>3</u>	<u>61</u>	<u>2</u>	<u>109</u>	<u>6</u>	<u>173</u>	<u>2</u>	<u>233</u>	<u>3</u>
<u>19</u>	<u>2</u>	<u>67</u>	<u>2</u>	<u>113</u>	<u>3</u>	<u>179</u>	<u>2</u>	<u>239</u>	<u>7</u>
<u>23</u>	<u>5</u>	<u>71</u>	7	<u>127</u>	<u>3</u>	<u>181</u>	<u>2</u>	<u>241</u>	<u>7</u>
<u>29</u>	<u>2</u>	<u>73</u>	<u>5</u>	<u>131</u>	<u>2</u>	<u>191</u>	<u>19</u>	<u>251</u>	<u>6</u>
<u>31</u>	<u>3</u>	<u>79</u>	<u>3</u>	<u>137</u>	<u>3</u>	<u>193</u>	<u>5</u>	<u>257</u>	<u>3</u>
<u>37</u>	<u>2</u>	<u>83</u>	2	<u>139</u>	<u>2</u>	<u>197</u>	<u>2</u>		
<u>41</u>	<u>6</u>	<u>89</u>	<u>3</u>	<u>149</u>	<u>2</u>	<u>199</u>	<u>3</u>		
<u>43</u>	<u>3</u>	<u>97</u>	<u>5</u>	<u>151</u>	<u>6</u>	<u>211</u>	<u>2</u>		

Table 4.2.3-2: Table of prime *p* and associated primitive root <u>*g*</u>₀

p	g₀	P	g₀	Ð	g ₀	P	G ₀	þ	g ₀
17	3	59	2	103	5	157	5	211	2
19	2	61	2	107	2	163	2	223	3
23	5	67	2	109	6	167	5	227	2
29	2	71	7	113	3	173	2	229	6
31	3	73	5	127	3	179	2	233	3
37	2	79	ት	131	2	181	2	239	7
41	6	83	2	137	3	191	19	241	7
43	3	89	3	139	2	193	5	251	6
47	5	97	5	149	2	197	2	257	3
53	2	101	2	151	6	199	3		

4.2.3.2.3.2 Definition of the number of pruning bits

The output of the mother interleaver is pruned by deleting the l-bits in order to adjust the mother interleaver to the block length K, where the deleted bits are non-existent bits in the input sequence. The pruning bits number l is defined as:

 $l = R \times C - K$,

where R is the row number and C is the column number defined in section 4.2.3.2.3.1.

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list expected approval meeting	^{# here} for info ↑	approval X prmation	non-st	rategic (for SMG rategic use only)
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Work item: TS 2	5.222			
(only one category shall be marked C Fund	ection esponds to a correction tion of feature ctional modification of fe orial modification		elease	Se: Phase 2 Release 96 Release 97 Release 98 Release 99 Release 00
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Definitions, symbols and abbreviations 3

Definitions 3.1

For the purposes of the present document, the [following] terms and definitions [given in ... and the following] apply.

TrCH number: Transport channel number represents a TrCH ID assigned to L1 by L2. Transport channels are multiplexed to the CCTrCH in the ascending order of these IDs.

3.2 **Symbols**

For the purposes of the present document, the following symbols apply:

$\lceil x \rceil$	round towards ∞ , i.e. integer such that $x \leq \sqrt{x} > x+1$
[x]	round towards $-\infty$, i.e. integer such that $x-1 < \lfloor x \rfloor \le x$
x	absolute value of <i>x</i>

Unless otherwise is explicitly stated when the symbol is used, the meaning of the following symbols are:

i	TrCH number
j	TFC number
k	Bit number
l	TF number
т	Transport block number
п	Radio frame number
р	PhCH number
r	Code block number
Ι	Number of TrCHs in a CCTrCH.
C_i	Number of code blocks in one TTI of TrCH <i>i</i> .
F_i	Number of radio frames in one TTI of TrCH <i>i</i> .
M_i	Number of transport blocks in one TTI of TrCH <i>i</i> .
Р	Number of PhCHs used for one CCTrCH.
PL	Puncturing Limit-for the uplink. Signalled from higher layers
RM_i	Rate Matching attribute for TrCH <i>i</i> . Signalled from higher layers.

Temporary variables, i.e. variables used in several (sub)sections with different meaning.

x, X

1

y, Y

z, Z

5

4.2.13 Transport format detection

Transport format detection can be performed both with and without Transport Format Combination Indicator (TFCI). If a TFCI is transmitted, the receiver detects the transport format combination from the TFCI. When no TFCI is transmitted, so called blind transport format detection may be used, i.e. the receiver side uses the possible transport format combinations as a priori information.

4.2.13.1 Blind transport format detection

Blind Transport Format Detection is optional both in the UE and the UTRAN. Therefore, for all CCTrCH a TFCI shall be transmitted, including the possibility of a TFCI length zero, if only one TFC is defined.

Blind transport format detection may be performed in the receiver by trying all possible combinations of the transport format.

4.2.13.2 Explicit transport format detection based on TFCI

4.2.13.2.1 Transport Format Combination Indicator (TFCI)

The Transport Format Combination Indicator (TFCI) informs the receiver of the transport format combination of the CCTrCHs. As soon as the TFCI is detected, the transport format combination, and hence the individual transport channels' transport formats are known, and decoding of the transport channels can be performed.

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Clauses affecte	<u>d:</u> 4.3.1.1	, 4.3.1.2.2						
<u>Other specs</u> <u>Affected:</u>	Other 3G corr Other GSM c specificat MS test spec BSS test spe O&M specific	ions ifications cifications	-	$\begin{array}{l} \rightarrow \text{ List of CI} \\ \rightarrow \text{ List of CI} \end{array}$	Rs: Rs: Rs:			
<u>Other</u> comments:								

4.3 Coding for layer 1 control

4.3.1 Coding of transport format combination indicator (TFCI)

Encoding of the TFCI bits depends on the number of them. If there are 6-10 bits of TFCI the channel encoding is done as described in section 4.3.1.1. Also specific coding of less than 6 bits is possible as explained in section 4.3.1.2.

4.3.1.1 Coding of long TFCI lengths

The TFCI bits are encoded using a (32, 10) sub-code of the second order Reed-Muller code. The coding procedure is as shown in figure 4.3.3.1-1.

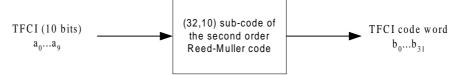


Figure 4.3.3.1-1: Channel coding of TFCI bits

TFCI is encoded by the (32,10) sub-code of second order Reed-Muller code. The code words of the (32,10) sub-code of second order Reed-Muller code are linear combination of some among 10 basis sequences. The basis sequences are as follows in table 4.3.1-1.

I	M _{i,0}	M _{i,1}	M _{i,2}	M _{i,3}	M _{I,4}	$M_{i,5}$	M _{i,6}	M _{i,7}	M _{i,8}	M i,9
0	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	0	0	0	0
1	<u>0</u> 4	<u>1</u> 0	<u>0</u> 4	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	1	0	0	0
2	<u>1</u> 4	<u>1</u> 4	<u>0</u> 4	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	0	0	0	1
3	<u>0</u> 4	<u>0</u> 0	<u>1</u> 0	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	1	0	1	1
4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	0	0	0	1
5	<u>0</u> 4	<u>1</u> 0	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	0	0	1	0
6	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	0	1	0	0
7	<u>0</u> 1	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	<u>0</u> 4	<u>1</u> 0	0	1	1	0
8	<u>1</u> 4	<u>0</u> 4	<u>0</u> 0	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0	1	1	1	0
9	<u>0</u> 1	<u>1</u> 0	<u>0</u> 4	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0	1	0	1	1
10	<u>1</u> 4	<u>1</u> 4	<u>0</u> 4	<u>1</u> 0	<u>0</u> 4	<u>1</u> 0	0	0	1	1
11	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	0	1	1	0
12	<u>1</u> 4	<u>0</u> 4	<u>1</u> 0	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	0	1	0	1
13	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	1	0	0	1
14	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	1	1	1	1
15	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	1	1	0	0
16	<u>0</u> 1	<u>1</u> 0	<u>0</u> 4	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	1	1	0	1
17	<u>1</u> 4	<u>1</u> 4	<u>0</u> 4	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	1	0	1	0
18	<u>0</u> 4	<u>0</u> 0	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	0	1	1	1
19	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	0	1	0	1
20	<u>0</u> 4	<u>1</u> 0	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	0	0	1	1
21	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	0	1	1	1
22	<u>0</u> 4	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4	0	1	0	0
23	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4	1	1	0	1
24	<u>0</u> 4	<u>1</u> 0	<u>0</u> 4	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4	1	0	1	0
25	<u>1</u> 4	<u>1</u> 4	<u>0</u> 4	<u>1</u> 0	<u>1</u> 1	<u>1</u> 4	1	0	0	1
26	<u>0</u> 4	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	<u>1</u> 1	<u>1</u> 4	0	0	1	0
27	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	<u>1</u> 1	<u>1</u> 4	1	1	0	0
28	<u>0</u> 4	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	1	1	1	0
29	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>1</u> 1	<u>1</u> 4	1	1	1	1
30	<u>0</u> 1	<u>0</u> 0	<u>0</u> 0	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	0	0	0	0
31	<u>0</u> 4	<u>0</u> 0	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	1	0	0	0

Table 4.3.1-1: Basis sequences for (32,10) TFCI code

For TFCI bits $a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9$ (a_0 is LSB and a_9 is MSB), the output code word bits b_i are given by: $b_i = \sum_{n=0}^{9} (a_n \times M_{i,n}) \mod 2$

where i=0...31. N_{TFCI} =32.

4.3.1.2 Coding of short TFCI lengths

4.3.1.2.1 Coding very short TFCIs by repetition

If the number of TFCI bits is 1 or 2, then repetition will be used for coding. In this case each bit is repeated to a total of 4 times giving 4-bit transmission (N_{TFCI} =4) for a single TFCI bit and 8-bit transmission (N_{TFCI} =8) for 2 TFCI bits. In the case of two TFCI bits denoted b_0 and b_1 the TFCI word shall be { $b_0, b_1, b_0, b_1, b_0, b_1$ }.

4.3.1.2.2 Coding short TFCIs using bi-orthogonal codes

If the number of TFCI bits is in the range 3 to 5 the TFCI bits are encoded using a (16, 5) bi-orthogonal (or first order Reed-Muller) code. The coding procedure is as shown in figure 4-8.

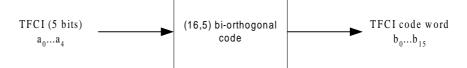


Figure 4-8: Channel coding of short length TFCI bits

The code words of the (16,5) bi-orthogonal code are linear combinations of 5 basis sequences as defined in table 4.3.1-2 below.

i	M _{i,0}	M _{i,1}	M _{i,2}	M _{i,3}	M _{i,4}
0	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0
1	<u>0</u> 1	<u>1</u> 0	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0
2	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0
3	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0
4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0
5	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0
6	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0
7	<u>0</u> 1	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4
8	<u>1</u> 4	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4
9	<u>0</u> 4	<u>1</u> 0	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4
10	<u>1</u> 4	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4
11	<u>0</u> 1	<u>0</u> 0	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4
12	<u>1</u> 4	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4
13	<u>0</u> 1	<u>1</u> 0	<u>1</u> 4	<u>1</u> 4	<u>1</u> 4
14	<u>1</u> 4				
15	<u>0</u> 4	<u>0</u> 0	<u>0</u> 0	<u>0</u> 0	<u>1</u> 0

Table 4.3.1-2: Basis sequences for (16,5) TFCI code

For TFCI information bits a_0 , a_1 , a_2 , a_3 , a_4 (a_0 is LSB and a_4 is MSB), the), the output code word bits b_j are given by: $b_i = \sum_{n=0}^{4} (a_n \times M_{i,n}) \mod 2$

where i=0...15. N_{TFCI} =16.

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4.2.2 Transport block concatenation and code block segmentation

All transport blocks in a TTI are serially concatenated. If the number of bits in a TTI is larger than Z, then code block segmentation is performed after the concatenation of the transport blocks. The maximum size of the code blocks depend on if convolutional or turbo coding is used for the TrCH.

4.2.2.1 Concatenation of transport blocks

The bits input to the transport block concatenation are denoted by $b_{im1}, b_{im2}, b_{im3}, \dots, b_{imB_i}$ where *i* is the TrCH number, *m* is the transport block number, and B_i is the number of bits in each block (including CRC). The number of transport blocks on TrCH *i* is denoted by M_i . The bits after concatenation are denoted by $x_{i1}, x_{i2}, x_{i3}, \dots, x_{iX_i}$, where *i* is the TrCH number and $X_i = M_i B_i$. They are defined by the following relations:

$$\begin{aligned} x_{ik} &= b_{i1k} \quad k = 1, 2, \dots, B_i \\ x_{ik} &= b_{i,2,(k-B_i)} \quad k = B_i + 1, B_i + 2, \dots, 2B_i \\ x_{ik} &= b_{i,3,(k-2B_i)} \quad k = 2B_i + 1, 2B_i + 2, \dots, 3B_i \\ \dots \\ x_{ik} &= b_{i,M_i,(k-(M_i-1)B_i)} \quad k = (M_i - 1)B_i + 1, (M_i - 1)B_i + 2, \dots, M_i B_i \end{aligned}$$

4.2.2.2 Code block segmentation

NOTE: It is assumed that filler bits are set to 0.

Segmentation of the bit sequence from transport block concatenation is performed if $X_i > Z$. The code blocks after segmentation are of the same size. The number of code blocks on TrCH *i* is denoted by C_i . If the number of bits input to the segmentation, X_i , is not a multiple of C_i , filler bits are added to the beginning of the first last block. The filler bits are transmitted and they are always set to 0. The maximum code block sizes are:

convolutional coding: Z = 504

turbo coding: Z = 5114

no channel coding: Z = unlimited

The bits output from code block segmentation are denoted by $o_{ir1}, o_{ir2}, o_{ir3}, \dots, o_{irK_i}$, where *i* is the TrCH number, *r* is the code block number, and K_i is the number of bits.

Number of code blocks: $C_i = [X_i / Z]$

Number of bits in each code block:

 $\frac{\text{if } X_i < 40 \text{ and Turbo coding is used, then}}{K_i = 40}$ $\frac{\text{else}}{K_i} = \int X_i / C_i$ $\frac{\text{end if}}{K_i}$ Number of filler bits: $Y_i = C_i K_i - X_i$

If $X_i \leq Z$, then

 $\underbrace{o_{i1k} = 0}_{k = 1, 2, \dots, Y_i} \\ o_{i1k} = x_{i,(k-Y_i)} \\ \underbrace{o_{i1k} = x_{i,k}}_{k = Y_i + 1, Y_i + 2, \dots, K_i}$

end if , and $K_i = X_i$. If $X_i \ge Z$, then $o_{i1k} = 0$ $k = 1, 2, ..., Y_i$ $o_{i1k} = x_{i,(k-Y_i)} + o_{i1k} = x_{ik}$ $k = Y_i \pm 1, Y_i \pm 2, ..., K_i$ $o_{i2k} = x_{i,(k+K_i-Y_i)} + o_{i2k} = x_{i,(k+K_i)}$ $k = 1, 2, ..., K_i$ $o_{i3k} = x_{i,(k+2K_i-Y_i)} + o_{i3k} = x_{i,(k+2K_i)}$ $k = 1, 2, ..., K_i$... $o_{iC_ik} = x_{i,(k+(C_i-1)K_i-Y_i)} + o_{iC_ik} = x_{i(k+(C_i-1)K_i)}$ $k = 1, 2, ..., K_i - Y_i$ $o_{iC_ik} = 0$ $k = (K_i - Y_i) + 1, (K_i - Y_i) + 2, ..., K_i$ end if

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4.2.7.1.2 Turbo encoded TrCHs

If repetition is to be performed on turbo encoded TrCHs, i.e. $\Delta N_{i,j} > 0$, the parameters in section 4.2.7.1.1 are used.

If puncturing is to be performed, the parameters below shall be used. Index b is used to indicate systematic (b=1), 1^{st} parity (b=2), and 2^{nd} parity bit (b=3).

a = 2 when b=2
a = 1 when b=3

$$\Delta N_i = \begin{cases} \left[\Delta N_{i,j} / 2 \right], & b = 2\\ \left[\Delta N_{i,j} / 2 \right], & b = 3 \end{cases}$$

If ΔN_i is calculated as 0 for b=2 or b=3, then the following procedure and the rate matching algorithm of section 4.2.7.3 don't need to be performed for the corresponding parity bit stream.

 $X_i = \lfloor N_{i,j}/3 \rfloor$,

 $q = \lfloor X_i / |\Delta N_i| \rfloor$

 $if(q \le 2)$

for x=0 to F_i-1

 $S[I_F[(3x+b-1) \mod F_i]] = x \mod 2$; end for

else

if q is even

then $q' = q - gcd(q, F_i)/F_i$ -- where $gcd(q, F_i)$ means greatest common divisor of q and F_i

-- note that q' is not an integer, but a multiple of 1/8

else q' = q

endif

for x=0 to $F_i - 1$

 $r = [x^{*}q^{'}] \mod F_{i};$

 $S[I_F[(3r+b-1) \mod F_i]] = [x*q'] \operatorname{div} F_i;$

endfor

endif

For each radio frame, the rate-matching pattern is calculated with the algorithm in section 4.2.7.3, where:

 X_i is as above,

 $e_{ini} = (a \cdot S(n_i) \cdot |\Delta N_i| + X_i) \text{ mod } (a \cdot X_i), \text{ if } e_{ini} = 0 \text{ then } e_{ini} = a \cdot X_i.$

 $e_{plus} = a \cdot X_i$

 $e_{\rm minus} = a \cdot |\Delta N_i|$

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$$o_{iC_ik} = x_{i(k+(C_i-1)K_i)}$$
 $k = 1, 2, ..., K_i - Y_i$

 $o_{iC_ik} = 0 \ k = (K_i - Y_i) + 1, (K_i - Y_i) + 2, \dots, K_i$

Channel coding 4.2.3

Code blocks are delivered to the channel coding block. They are denoted by $o_{ir1}, o_{ir2}, o_{ir3}, \dots, o_{irK_i}$, where *i* is the TrCH number, r is the code block number, and K_i is the number of bits in each code block. The number of code blocks on TrCH *i* is denoted by C_i . After encoding the bits are denoted by $y_{ir1}, y_{ir2}, y_{ir3}, \dots, y_{irY_i}$, where Y_i is the number of encoded bits. The encoded blocks are serially multiplexed so that the block with lowest index r is output first from the channel coding block. The bits output are denoted by $c_{i1}, c_{i2}, c_{i3}, \dots, c_{iE_i}$, where *i* is the TrCH number and E_i = $C_i Y_i$. The output bits are defined by the following relations:

 $c_{ik} = y_{i1k} - k = 1, 2, ..., Y_i$ $c_{ik} = y_{i,2,(k-Y_i)} - k = Y_i + 1, Y_i + 2, \dots, 2Y_i$ $c_{ik} = y_{i,3,(k-2Y_i)} - k = 2Y_i + 1, 2Y_i + 2, \dots, 3Y_i$

 $c_{ik} = y_{i,C_i,(k-(C_i-1)Y_i)} - k = (C_i - 1)Y_i + 1, (C_i - 1)Y_i + 2, \dots, C_iY_i$

The relation between O_{irk} and $Y_{\underline{y}irk}$ and between K_i and Y_i is dependent on the channel coding scheme.

The following channel coding schemes can be applied to transport channels:

- Convolutional coding
- Turbo coding
- No channel-coding

<u>Usage of coding scheme and coding rate for the different types of TrCH is shown in table 4.2.3-1.</u> The values of Y_i in connection with each coding scheme:

- Convolutional coding, $\frac{1}{2}$ with rate $\frac{1}{2}$: $Y_i = 2^*K_i + 16$; rate $\frac{1}{3}$ -rate: $Y_i = 3^*K_i + 24$
- Turbo coding, with rate 1/3-rate: $Y_i = 3*K_i + 12$
- No channel-coding: $Y_i = K_i$ -

Table 4.2.3-1: Usage of channel coding scheme and coding rate Error Correction Coding Parameters

<u>Type of TrCH</u>	Coding scheme	Coding rate
<u>BCH</u>		
<u>PCH</u>	<u>Convolutional coding</u>	<u>1/2</u>
<u>RACH</u>	<u>Convolutional coding</u>	
		<u>1/3, 1/2</u>
DCH, DSCH, FACH, USCH	Turbo coding	<u>1/3</u>
	No codi	ng

Transport channel type	Coding scheme	Coding rate
BCH		
PCH		1/2
FACH	Convolutional code	1/2
RACH		
		1/3, 1/2
DCH, DSCH, USCH	Turbo code	1/3
	No coding	

4.2.3.1 Convolutional <u>Cc</u>oding

----<u>Convolutional codes with C</u>constraint length K=9- and Ccoding rates 1/3 and 1/2 are defined and 1/3.

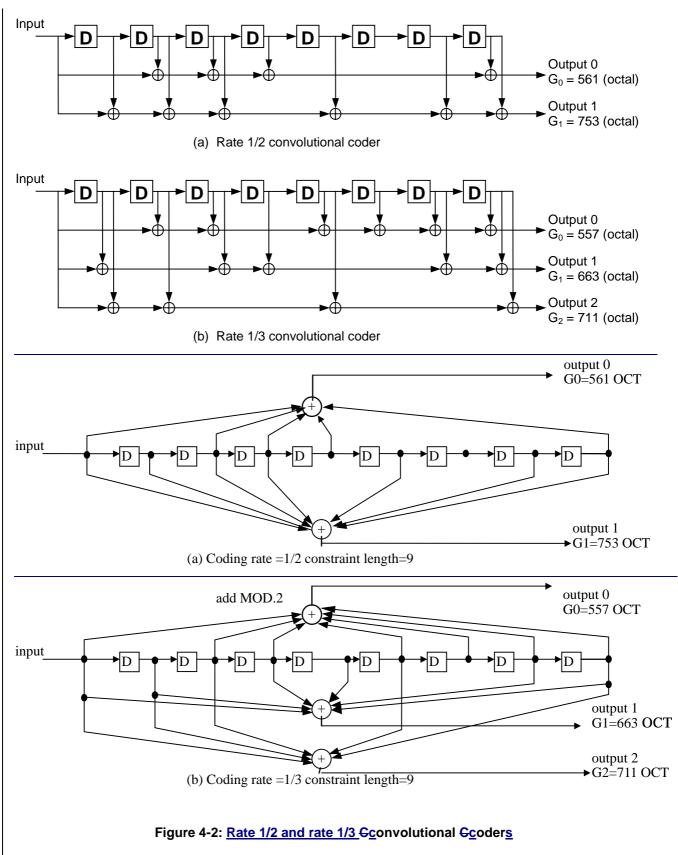
-----The configuration of the convolutional coder is presented in figure 4-2.

<u>The oO</u>utput from the <u>rate 1/3</u> convolutional coder shall be done in the order output0, output1, <u>output2</u>, <u>output3</u>, <u>output1</u>, <u>output1</u>,

8 tail bits with binary value 0 shall be added to the end of the code block before encoding.

----The initial value of the shift register of the coder shall be "all 0" when starting to encode the input bits.

- K-1 tail bits (value 0) shall be added to the end of the code block before encoding.



4.2.3.2 Turbo coding

4.2.3.2.1 Turbo coder

<u>The scheme of Turbo coder is a For data services requiring quality of service between 10^{-3} and 10^{-6} BER inclusive, <u>pP</u>arallel e<u>C</u>oncatenated e<u>C</u>onvolutional e<u>C</u>ode (PCCC) with <u>two</u> 8-state constituent encoders <u>and one Turbo code</u></u>

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internal interleaveris used. The coding rate of Turbo coder is 1/3. The structure of Turbo coder is illustrated in figure 4-3.

The transfer function of the 8-state constituent code for PCCC is

$$\underline{\qquad} G(D) = \underbrace{\left[1, n(D) \right]}_{d(D)} \left[1, \frac{g_1(D)}{g_0(D)} \right]$$

where,

$$d_{\underline{g_0}}(D) = 1 + D^2 + D^3$$
.

$$\underline{g_1}(D) = 1 + D + D^3.$$

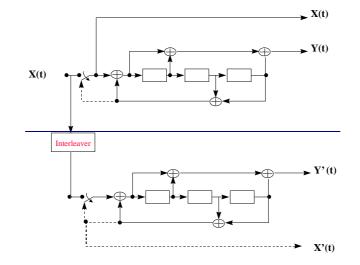


Figure 4-3: Structure of the 8-state PCCC encoder (dotted lines effective for trellis termination only)

The initial value of the shift registers of the <u>PCCC-8-state constituent</u> encoders shall be all zeros when starting to encode the input bits.

The o<u>O</u>utput of the PCCC encoder is punctured to produce coded bits corresponding to the desired code rate. For rate $\frac{1}{3}$, none of the systematic or parity bits are punctured, and the output sequence from the Turbo coder is $\frac{X(0)}{Y(0)}$, $\frac{Y'(0)}{X(1)}$, $\frac{Y(1)}{Y(1)}$, etc.

$x_{\underline{1}}, z_{\underline{1}}, z'_{\underline{1}}, x_{\underline{2}}, z_{\underline{2}}, z'_{\underline{2}}, \dots, x_{\underline{K}}, z_{\underline{K}}, z'_{\underline{K}},$

where $x_1, x_2, ..., x_K$ are the bits input to the Turbo coder i.e. both first 8-state constituent encoder and Turbo code internal interleaver, and *K* is the number of bits, and $z_1, z_2, ..., z_K$ and $z'_1, z'_2, ..., z'_K$ are the bits output from first and second 8-state constituent encoders, respectively.

The bits output from Turbo code internal interleaver are denoted by $x'_1, x'_2, ..., x'_K$, and these bits are to be input to the second 8-state constituent encoder.

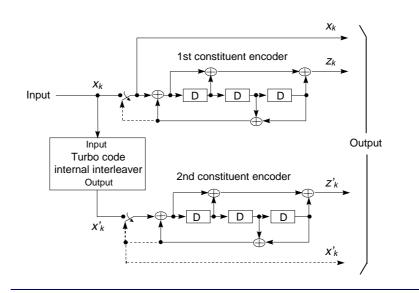


Figure 4-3: Structure of rate 1/3 Turbo coder (dotted lines apply for trellis termination only)

4.2.3.2.2 Trellis termination infor tTurbo coder

Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are <u>p</u>added after the encoding of information bits.

The first three tail bits shall be used to terminate the first constituent encoder (upper switch of figure 4-3 in lower position) while the second constituent encoder is disabled. The last three tail bits shall be used to terminate the second constituent encoder (lower switch of figure 4-3 in lower position) while the first constituent encoder is disabled.

The transmitted bits for trellis termination shall then be

 $\frac{X(t) Y(t) X(t+1) Y(t+1) X(t+2) Y(t+2) X'(t) Y'(t) X'(t+1) Y'(t+1) X'(t+2) Y'(t+2) x_{K+1}, z_{K+1}, x_{K+2}, z_{K+3}, z_{K+3}, x_{K+3}, x_{K+3}, z_{K+3}, z_{K+3$

4.2.3.2.3 Turbo code internal interleaver

Figure 4-4 depicts the overall 8 State PCCC Turbo coding scheme including Turbo code internal interleaver. The Turbo code internal interleaver consists of <u>bits-input to a rectangular matrix</u>, intra-row and inter-row permutations of the rectangular matrix, and bits-output from the rectangular matrix with pruning. mother interleaver generation and pruning. The bits input to the Turbo code internal interleaver are denoted by $x_1, x_2, x_3, \dots, x_K$, where K is the integer number of the bits and takes one value of $40 \le K \le 5114$. The relation between the bits input to the Turbo code internal interleaver and the bits input to the channel coding is defined by $x_k = o_{irk}$ and $K = K_{ir}$. For arbitrary given

block length K, one mother interleaver is selected from the 134 mother interleavers set. The generation scheme of mother interleaver is described in section 4.2.3.2.3.1. After the mother interleaver generation, *l* bits are pruned in order to adjust the mother interleaver to the block length K. Tail bits T_1 and T_2 are added for constituent encoders RSC1 and RSC2, respectively. The definition of *l* is shown in section 4.2.3.2.3.2.

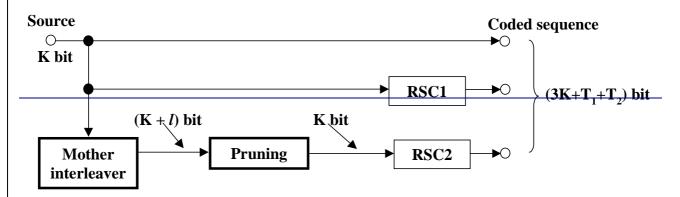


Figure 4-4: Overall 8 State PCCC Turbo Coding

The following section specific symbols are used in sections 4.2.3.2.3.1 – 4.2.3.4.3.3:

K	Number of bits input to Turbo code internal interleaver
R	Number of rows of rectangular matrix
С	Number of columns of rectangular matrix
р	Prime number
v	Primitive root
$\overline{s(i)}$	Base sequence for intra-row permutation
\underline{a}_i	Minimum prime integers
$\underline{r_i}$	Permuted prime integers
T(j)	Inter-row permutation pattern
$U_i(i)$	Intra-row permutation pattern
i	Index of matrix
j	Index of matrix
k	Index of bit sequence

4.2.3.2.3.1 Bits-input to rectangular matrix Mother interleaver generation

The bit sequence input to the Turbo code internal interleaver x_k The interleaving consists of three stages. In first stage,

the input sequence is written into the rectangular matrix <u>as follows:</u> row by row. The second stage is intra-row permutation. The third stage is inter row permutation. The three stage permutations are described as follows, the input block length is assumed to be K (320 to 5114 bits).

First Stage:

(1) Determine the number of rows R of the rectangular matrix such that

 $R = \begin{cases} 5, \text{if } (40 \le K \le 159) \\ 10, \text{if } ((160 \le K \le 200) \text{ or } (481 \le K \le 530)) \\ 20, \text{if } (K = \text{any other value}) \end{cases}$

R=20 (K = any other block length except 481 to 530 bits; Case 2)

where the rows of rectangular matrix are numbered 0, 1, 2, ..., R - 1 from top to bottom.

(2) Determine the number of columns $C \underline{of rectangular matrix}$ such that

```
\frac{\text{if } (481 \leq K \leq 530) \text{ then}}{p = 53 \text{ and } C = p.}
\frac{\text{else}}{\text{Case } 1; C = p = 53}
```

Case 2;

(i) -fFind minimum prime p such that,

$$\theta = \langle (p_+, 1) - K/R \ge 0$$
,
and determine C such that
(ii) if $-(0 = \langle p_- - K/R \ge 0)$ then go to (iii)
if $(p - 1 - K/R \ge 0)$ then
 $C = p - 1$.
else
 $C = p$.
end if
else
 $-C = p_+ + 1$.
end if
where the columns of rectangular matrix are numbered 0, 1, 2, ..., C - 1 from left to right.

<u>(iii) if (0 = then C=p 1.</u>

Else C = p.

(3) <u>Write</u> \underline{T}_{the} input <u>bit</u> sequence $\underline{x_k}$ of the interleaver is written into the $R \times \underline{x}C$ rectangular matrix row by row starting with bit $\underline{x_1}$ from in column 0 of row 0-:

x ₁	<i>x</i> ₂	<i>x</i> ₃	x _C	
<i>x</i> _(C+1)	$x_{(C+2)}$	$x_{(C+3)}$	x _{2C}	
	:	:	:	-
$x_{((R-1)C+1)}$	$x_{((R-1)C+2)}$	$x_{((R-1)C+3)}$	$\dots x_{RC}$	

Second Stage:

A. If C = p

4.2.3.2.3.2 Intra-row and inter-row permutations

After the bits-input to the $R \times C$ rectangular matrix, the intra-row and inter-row permutations are performed by using the following algorithm:

(1) (A-1) Select a primitive root $g_0 - v$ from table 4.2.23-2.

(2) (A-2)—Construct the base sequence $e_{\underline{s}}(i)$ for intra-row permutation as:

 $\frac{c(i) = [g_0 \times c(i-1)] \mod p \cdot \underline{s(i)} = [v \times \underline{s(i-1)}] \mod p}{i = 1, 2, \dots, (p-2), and es(0) = 1.$

(3) (A-3) Let $q_0 = 1$ be the first prime integer in $\{q_j\}$, and S select the consecutive minimum prime integers set $\{q_j\}$ ($j = 1, 2, ..., R_{j-1}$) such that

g.c.d{ q_j, p_{-1} } = 1,

 $q_j > 6$, and

 $q_j > q_{(j-1)}$

where g.c.d. is greatest common divider<u>divisor</u>. And $q_{\sigma} = 1$.

(4) (A 4) Permute The set $\{q_i\}$ is permuted to make a new set $\{p_{ij}\}$ such that

 $p_{\mathbf{P}(j)} \underline{r}_{\underline{T}(j)} = q_j, \ j = 0, 1, \dots, \underline{R}_{-1},$

where $P_{\underline{T}(j)}$ indicates the original row position of the *j*-th permuted row, and T(j) is the inter-row permutation pattern defined as the one of the following four kind of patterns: Pat_1 , Pat_2 , Pat_3 and Pat_4 depending on the number of input bits *K*. in the third stage.

	Pat ₄	$\mathrm{if}(40 \leq K \leq 159)$
	Pat ₃	$\mathrm{if}(160 \leq K \leq 200)$
	Pat ₁	$\mathrm{if}(201 \leq K \leq 480)$
	Pat ₃	$\mathrm{if}(481 \leq K \leq 530)$
$T(j) = \langle$	Pat ₁	if $(531 \le K \le 2280)$.
	Pat ₂	if $(2281 \le K \le 2480)$
	Pat ₁	if $(2481 \le K \le 3160)$
	Pat ₂	if $(3161 \le K \le 3210)$
	Pat ₁	if $(3211 \le K \le 5114)$

where *Pat*₁, *Pat*₂, *Pat*₃ and *Pat*₄ have the following patterns respectively.

 $\begin{array}{l} \underline{Pat_{1}: \{19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11\}} \\ \underline{Pat_{2}: \{19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10\}} \\ \underline{Pat_{3}: \{9, 8, 7, 6, 5, 4, 3, 2, 1, 0\}} \\ \underline{Pat_{4}: \{4, 3, 2, 1, 0\}} \end{array}$

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(5) (A-5) Perform the *j*-th ($j = 0, 1, 2, ..., -C\underline{R} - 1$) intra-row permutation as:

 $\frac{\text{if } (C = p) \text{ then}}{c_j(i) = c([i \times p_j] \mod(p-1)) \cdot \underline{U}_j(i) = s([i \times \underline{r}_j] \mod(p-1))}, \quad -i = 0, 1, 2, \dots, (p-2), \text{ and } \underline{eU}_j(p-1) = 0,$ where $\underline{eU}_j(i)$ is the input bit position of *i*-th output after the permutation of *j*-th row.
end if $\underline{Hif} (C = p_{+1}) \underline{hen}$ $\underline{(B - 1) \text{ Same as case A } 1.}$ (B - 2) Same as case A 3.

(B-4) Same as case A-4.

(B 5) Perform the *j* th (j = 0, 1, 2, ..., R 1) intra row permutation as:

 $\frac{c_j(i) = c([i \times p_j] \mod(p-1))}{U_j(i)} = s([i \times r_j] \mod(p-1)), \quad -i = 0, 1, 2, \dots, (p-2), \quad e\underline{U}_j(p-1) = 0, \text{ and } e\underline{U}_j(p) = p,$

where $eU_i(i)$ is the input bit position of *i*-th output after the permutation of *j*-th row-, and

 $\frac{(\mathbf{B} \cdot \mathbf{6}) - \mathbf{I}_{\underline{i}} \mathbf{f} (K = C \times \mathbf{x} R) \text{ then}}{\mathbf{e} \underline{E} \text{xhange } \mathbf{e} \underline{U}_{R-1}(p) \text{ with } \mathbf{e} \underline{U}_{R-1}(0).$ end if

end if

 $\operatorname{\underline{Hi}f}(C = p - 1) \operatorname{\underline{then}}$

(C 1) Same as case A 1.

(C 2) Same as case A 2.

(C 3) Same as case A 3.

(C-4) Same as case A 4.

(C-5) Perform the *j*-th (j = 0, 1, 2, ..., R-1) intra-row permutation as:

 $\frac{c_1(i) = c([i \times p_1] \mod (p-1))}{U_i(i) = s([i \times r_j] \mod (p-1))} - 1, \quad -i = 0, 1, 2, \dots, (p-2),$

where $e\underline{U}_j(i)$ is the input bit position of *i*-th output after the permutation of *j*-th row. end if

Third Stage:

— Perform the inter row permutation based on the following P(j) (*j*=0,1, ..., R 1) patterns, where P(j) is the original row position of the *j* th permuted row.

P_A: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11} for R=20

P_B: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10} for R=20

P_C: {9, 8, 7, 6, 5, 4, 3, 2, 1, 0} for R=10

The usage of these patterns is as follows:

Block length K: P(j)

320 to 480 bit: PA

481 to 530 bit: P_C

531 to 2280 bit: PA

2281 to 2480 bit: P_B

2481 to 3160 bit: P_A

3161 to 3210 bit: P_B

3211 to 5114-bit: PA

(2) The output of the mother interleaver is the sequence read out column by column from the permuted $R - \times C$ matrix starting from column 0.

p	<u>v</u>	<u>p</u>	<u>v</u>	p	<u>v</u>	<u>p</u>	<u>v</u>	<u>p</u>	<u>v</u>
<u>7</u>	<u>3</u>	<u>47</u>	<u>5</u>	<u>101</u>	<u>2</u>	<u>157</u>	<u>5</u>	<u>223</u>	<u>3</u>
<u>11</u>	<u>2</u>	<u>53</u>	<u>2</u>	<u>103</u>	<u>5</u>	<u>163</u>	2	<u>227</u>	2
<u>13</u>	<u>2</u>	<u>59</u>	<u>2</u>	<u>107</u>	<u>2</u>	<u>167</u>	<u>5</u>	<u>229</u>	<u>6</u>
<u>17</u>	<u>3</u>	<u>61</u>	<u>2</u>	<u>109</u>	<u>6</u>	<u>173</u>	2	<u>233</u>	<u>3</u>
<u>19</u>	<u>2</u>	<u>67</u>	<u>2</u>	<u>113</u>	3	<u>179</u>	2	<u>239</u>	<u>7</u>
<u>23</u>	<u>5</u>	<u>71</u>	<u>7</u>	<u>127</u>	<u>3</u>	<u>181</u>	<u>2</u>	<u>241</u>	<u>7</u>
<u>29</u>	<u>2</u>	<u>73</u>	<u>5</u>	<u>131</u>	<u>2</u>	<u>191</u>	<u>19</u>	<u>251</u>	<u>6</u>
<u>31</u>	<u>3</u>	<u>79</u>	<u>3</u>	<u>137</u>	3	<u>193</u>	5	<u>257</u>	<u>3</u>
<u>37</u>	<u>2</u>	<u>83</u>	<u>2</u>	<u>139</u>	<u>2</u>	<u>197</u>	2		
<u>41</u>	<u>6</u>	<u>89</u>	<u>3</u>	<u>149</u>	<u>2</u>	<u>199</u>	<u>3</u>		
<u>43</u>	<u>3</u>	<u>97</u>	<u>5</u>	<u>151</u>	<u>6</u>	<u>211</u>	2		

p	g₀	P	g ₀	p	g ₀	P	g ₀	þ	9 ₀
17	3	59	2	103	5	157	5	211	2
19	2	61	2	107	2	163	2	223	3
23	5	67	2	109	6	167	5	227	2
29	2	71	7	113	3	173	2	229	6
31	3	73	5	127	3	179	2	233	3
37	2	79	3	131	2	181	2	239	7
41	6	83	2	137	3	191	19	241	7
43	3	89	3	139	2	193	5	251	6
47	5	97	5	149	2	197	2	257	3
53	2	101	2	151	6	199	3		

4.2.3.2.3.322

Bits-output from rectangular matrix with Definition of the number of pruning-bits

After intra-row and inter-row permutations, the bits of the permuted rectangular matrix are denoted by y'k:

 $\begin{bmatrix} y'_1 & y'_{(R+1)} & y'_{(2R+1)} & \cdots & y'_{((C-1)R+1)} \\ y'_2 & y'_{(R+2)} & y'_{(2R+2)} & \cdots & y'_{((C-1)R+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y'_R & y'_{2R} & y'_{3R} & \cdots & y'_{CR} \end{bmatrix}$

The output of the Turbo code internal interleaver is the bit sequence read out column by column from the intra-row and inter-row permuted $R \times C$ matrix starting with bit y'_{1} in row 0 of column 0 and ending with bit y'_{CR} in row R - 1 of column C - 1. The output is pruned by deleting bits that were not present in the input bit sequence, i.e. bits y'_{k} that corresponds to bits x_{k} with k > K are removed from the output. The bits output from Turbo code internal interleaver are denoted by $x'_{1}, x'_{2}, ..., x'_{K}$, where x'_{1} corresponds to the bit y'_{k} with smallest index k after pruning, x'_{2} to the bit y'_{k} with second smallest index k after pruning, and so on. The output of the mother interleaver is pruned by deleting the l bits in order to adjust the mother interleaver to the block length K, where the deleted bits are non existent bits in the input sequence. The number of bits output from Turbo code internal interleaver is K and Tthe total number of pruneding bits number l is defined as:

$$-1 = R \times \stackrel{\longrightarrow}{\longrightarrow} C - K_{.,}$$

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where R is the row number and C is the column number defined in section 4.2.3.2.3.1.

4.2.3.3 Concatenation of encoded blocks

After the channel coding for each code block, if C_i is greater than 1, the encoded blocks are serially concatenated so that the block with lowest index *r* is output first from the channel coding block, otherwise the encoded block is output from channel coding block as it is. The bits output are denoted by $C_{i1}, C_{i2}, C_{i3}, \dots, C_{iE_i}$, where *i* is the TrCH number

and $E_i = C_i Y_i$. The output bits are defined by the following relations:

If no code blocks are input to the channel coding ($C_i = 0$), no bits shall be output from the channel coding, i.e. $E_i = 0$.