3GPP TSG GERAN SAIC Ad Hoc **GAHS-030030**
Chicago, U.S.A.
Oct. 28-30, 2003

Source: **Motorola**
Title: **SAIC Link Simulation Results**
Document for: **Discussion**

1. Introduction

Recently, some outstanding issues concerning the simulation assumptions of the "*Feasibility Study on Single Antenna Interference Cancellation (SAIC) for GSM Networks*" have been finalised. This paper outlines link-level simulation performance data consistent with the resulting GERAN-adopted interference models for both synchronous and asynchronous networks. Since the current GERAN work is focused on feasibility, results are presented for two exemplary approaches to advanced receiver design in GSM networks, including the cases a) GMSK desired signal and GMSK interfering signals, and b) GMSK desired signal and mixed GMSK/8-PSK interfering signals. A companion paper [8] reports network simulation results.

2. Simulation Assumptions

As determined by [3], the interferer models applicable to all of the system configurations assessed here comprised three discrete co-channel interferers, a single discrete adjacent channel interferer, a single residual co-channel interferer and two residual adjacent channel interferers (arranged symmetrically about the desired signal), where the residual interference was generated using an AWGN source shaped by the 8PSK pulse-shaping waveform specified in 3GPP TS 45.004.

Table 1 specifies the interferer configurations applicable to each reference system configuration in detail. As agreed at the 2nd SAIC *ad hoc* meeting (Seattle, March 2003), System Configurations 2/3 are merged to generate models corresponding to 40% and 70% loads. Configuration 4 is specified as the average (in dB) of the values offered in [6][7], while the parameters for System Configuration 1 are extracted from [7].

All of the results presented here used the receiver impairments model described in Table 2, which captures DC offset, I/Q gain and phase imbalance, and phase noise.[1] A random frequency offset (according to Table 3) was applied to each discrete interferer, where the generated frequency offsets were independently distributed over interferers and between bursts. Where frequency hopping was used, the realized multipath channel was independent between bursts for both the desired and interfering signals (i.e. 'ideal' frequency hopping was applied). Finally, DTX was enabled for the asynchronous models.

---

[1] *This model likely represents an upper bound on practically achievable impairments performance. It is used to potentially permit comparison of performance results (it is also recognised that companies are also free to used proprietary impairments models).*

Interferer Configuration		System Configuration			
Interferer	**TSC**	**1**	**2/3@40%**	**2/3@70%**	**4**
1st Co-Chan.	0	0	0	0	0
2nd Co-Chan.	U{1,..,7}[2]	-10.4	-6	-4	-9.7
3rd Co-Chan.	U{0,..,7}	-20.3	-10	-8	-17.0
Residual Co-Chan.	N/A	-	-9	-5	-20.6
1st Adj. Chan.[3]	U{0,..,7}	-15.3	-14	-14	-16.6
Residual Adj. Chan. (Upper)	N/A	-23.7	-18	-17	-24.9
Residual Adj. Chan. (Lower)	N/A	-23.7	-18	-17	-24.9

Table 1 – Interferer model definitions.

Impairment	Units	Value
DC Offset	dBc	-30
I/Q Gain Imbalance	dB	0.5
I/Q Phase Imbalance	degs	3
Phase Noise	degs RMS	1.0

Table 2 – Receiver impairments model.

Carrier Frequency (MHz)	Frequency Offset Standard Deviation (Hz)
900	16.7
1900	33

Table 3 – Interferer frequency offset model.

3. Receiver Types

There are a variety of feasible approaches to advanced receiver design for GSM, with each approach characterized by differing degrees of complexity and offering varying levels of performance depending on the interference environment. In order to make the broadest possible set of data available to the Feasibility Study, in what follows performance results are presented for two examples[4] of advanced receiver, denoted SAIC-A and SAIC-B. The SAIC-A receiver corresponds broadly to a quasi-linear processing approach, while SAIC-B has its roots in joint detection. Results are also presented for a reference 'conventional

[2] *U{a,b,...,c} denotes a uniform distribution over the argument list.*

[3] *Where the adjacent interference power levels at input to the receiver are 18dB great than listed.*

[4] *Other approaches are of course entirely feasible.*

receiver' whose performance is compliant with 3GPP TS 45.005 and (to our understanding) broadly indicative of contemporary GSM receiver performance.

4. 'Long-Term' Receiver Performance

Figure 5 (Appendix A) shows, for each system configuration, the long-term (i.e. mean FER vs. mean C/I) link-level performance of the reference conventional and SAIC-A receivers for both synchronous and asynchronous models for the Typical Urban (TU) channel model using Ideal Frequency Hopping (IFH). Note that the logical channel (i.e. either TCH/AFS12.2 or TCH/AFS5.9) is selected to correspond to the associated system configuration, and so AMR-12.2kbps results are reported for configurations 1 and 4, while AMR-5.9kps results are reported for configurations 2/3@40% and 2/3@70%.

Table 4 summarises the long-term performance improvement (dB) attributable to the SAIC-A receiver with respect to the conventional receiver at 1% FER. The performance of the SAIC-A receiver was generally superior to the conventional receiver, with the observed performance improvement ranging from 0.5-1.8dB for the synchronous case to 0.9-2.1dB for the asynchronous case.

System Configuration	SAIC-A Gain (dB) vs. System Synchronization Type	
	Synch.	Asynch.
1	1.8	2.0
2/3@40%	0.8	1.0
2/3@70%	0.5	0.9
4	1.7	2.1

Table 4 – SAIC-A long-term FER performance improvement by configuration – 1% FER.

The performance of the SAIC-B receiver under synchronous conditions is summarised in Figure 1, where again the FER data corresponds to the logical channel associated with each system configuration.

The long-term performance gains for the SAIC-B receiver relative to the conventional receiver are summarised in Table 5. It can be seen that the SAIC-B receiver has slightly better long-term performance than the SAIC-A receiver for the synchronous case, with gains lying in the range 0.7-2.8dB (compared to 0.5-1.8dB for SAIC-A).

System Configuration	SAIC-B Gain (dB) Synchronous Operation
1	2.8
2/3@40%	1.2
2/3@70%	0.7
4	2.5

Table 5 – SAIC-B mean FER performance improvement by configuration – 1% FER.

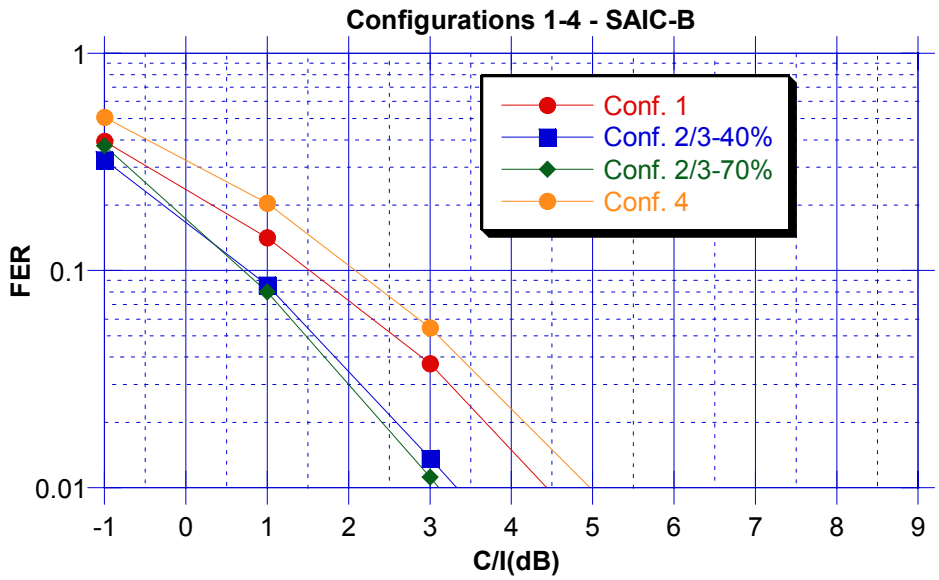

Figure 1 – SAIC-B receiver performance vs. system configuration.

Figure 2 compares the long-term performance of the conventional, SAIC-A and SAIC-B receivers for the asynchronous modes of system configurations 2/3@70% and 4.[5] In this case, as summarised in Table 6, the SAIC-A receiver generally out-performs the SAIC-B receiver by up to 1.5dB.

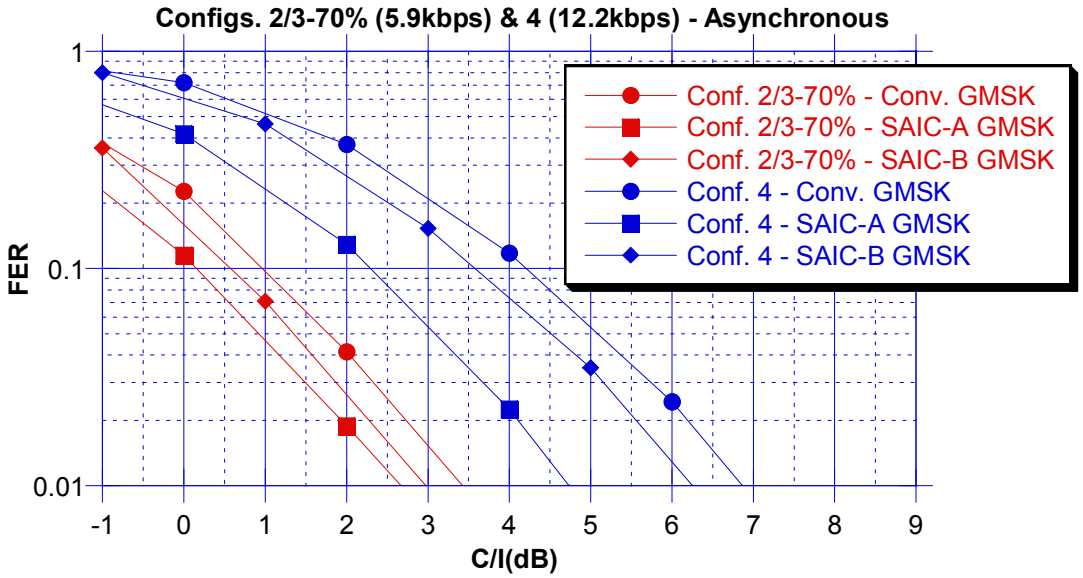

Figure 2 – Comparison of conventional, SAIC-A and SAIC-B long-tem receiver performance, asynchronous mode.

---

[5] *System configurations 1 and 2/3-40% showed similar behaviour and are omitted in the interest of simplicity.*

System Configuration	Gain (dB) rel. Conventional vs. Receiver Type	
	SAIC-A	SAIC-B
2/3@70%	0.8	0.5
4	2.1	0.6

Table 6 – SAIC-A and SAIC-B mean FER performance improvement by configuration at 1% FER - asynchronous.

5. GMSK-8PSK Performance

Although GMSK/8PSK interference scenarios were included in the original system definitions, they were not considered – either in circuit-switched or packet-switched form – as part of the work ([2][3][6][7]) which identified the interference configurations summarised in Table 1. Accordingly, Feasibility Study requirements for analysis of SAIC link-level performance for 8PSK desired or interfering signals are not fully defined.

Figure 3 presents some potentially illustrative data for the SAIC-A receiver, however, focused on reference system configuration 2 for two interfering scenarios:

a) where all of the discrete GMSK interferers are replaced with 8PSK interferers, and

b) where only the dominant discrete GMSK interferer is replaced with an 8PSK interferer,

Here, scenario b) is conceptually motivated (in simplistic fashion) by the desire to capture the effect a presumed lower 8PSK transmission probability in typical cell C/I distributions.

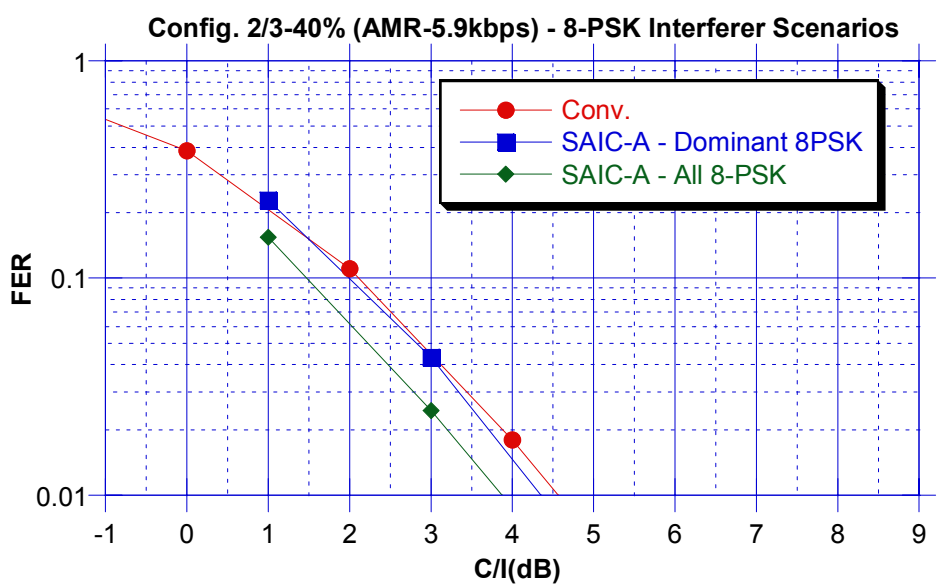

Figure 3 – SAIC-A receiver performance vs. GMSK/8PSK interferer mix Configuration 2/3-40%.

It can be seen from the figure that while the dominant 8PSK interferer appears to be the worst-case scenario, the overall receiver performance is still comparable to the conventional receiver, and accordingly the SAIC-A solution appears robust to 8PSK interference.

The structure of the SAIC-B receiver may lend itself, however, to the suppression of 8PSK interferers. This can be seen in Figure 4 which shows the raw bit error rate performance of the conventional and SAIC-B receivers in the presence of a single 8PSK interferer. Predictably, however, the performance differential degrades considerably when the GERAN interference models are applied (not shown), and the computational complexity of the SAIC-B receiver may be non-trivial in this mode of operation.

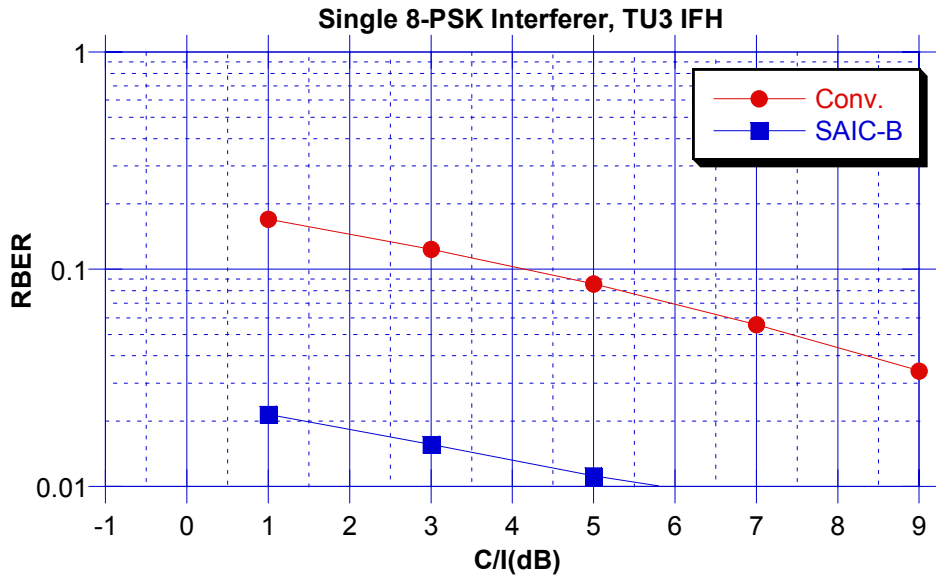

Figure 4 – SAIC-B performance, single 8-PSK interferer, TU3 IFH.

6. Link-System Mapping Performance

Examples of synchronous and asynchronous stage-1 (i.e. {C/I,DIR}->BEP) mappings for the SAIC-A receiver appear in Figure 6 and Figure 7 respectively. These mappings were used as the basis for the system simulation results presented in [8].

It can be seen that for the synchronous stage-1 mappings that the relationship between bit error probability (BEP) and C/I for a given DIR value was *broadly* independent of system configuration, although the SAIC-A receiver mappings tended to out-perform the conventional receiver by a larger margin for reference system configurations 1 and 4. The relative interferer power of configurations 1 and 4 also made it possible to more reliably report the BEP vs. C/I relationship for significantly larger DIR values.

The asynchronous mappings of Figure 7 include results for the conventional receiver under both synchronous and asynchronous conditions, and it can be seen that for configurations 1 and 4 the conventional receiver performed slightly better under asynchronous conditions than under synchronous conditions. A similar but smaller difference is observed for configuration 2/3-40% with the performance difference becoming largely negligible for configuration 2/3-70%.

Comparing the synchronous and asynchronous mappings, the performance of the conventional receiver was largely consistent, regardless of reference configuration and system synchronisation status. The

asynchronous system mappings did, however, show some overall performance improvement compared to the synchronous cases. Whether this effect is an artefact of the GERAN asynchronous interferer models, and would be encountered in practice is not completely clear.

Finally, Figure 8 shows examples of mappings for the SAIC-B receiver, in this case for configuration 2/3-40%. It can be seen that while the SAIC-B synchronous mapping shows some performance improvement over the corresponding SAIC-A mapping, the SAIC-B asynchronous mapping is degraded with respect to SAIC-A.

7. Observation and Conclusions

Both long-term and short-term (i.e. stage-1 mapping) results have been reported for a reference conventional receiver and two exemplary receivers. The following conclusions can be made.

a) ***Reference receiver performance*** – in determining the long-term performance gains of the advanced receivers, care must be taken in establishing the performance of the reference receiver. This can have a substantial impact on the apparent performance gains of the advanced receiver. The reference receiver performance for the GERAN asynchronous interference models was generally slightly better than for the synchronous models.

b) ***Long-term synchronous performance*** – under synchronous conditions, the SAIC-A receiver showed long-term performance gains at 1% FER of up to 2dB, while the SAIC-B approach showed gains of up to 3dB.

c) ***Long-term asynchronous performance*** – under asynchronous conditions the relative long-term performance of each receiver was reversed, with the SAIC-A approach sustaining gains of up to 2dB, while the SAIC-B receiver was restricted to gains of less than 1dB. Methods for improving the performance of the SAIC-B architecture under asynchronous conditions exist, but may be computationally non-trivial.

d) ***Rejection of 8PSK interference*** – the SAIC-A receiver appears robust to interference comprised of either a) uniform 8PSK-modulated signals, or b) a dominant 8PSK interferer with secondary GMSK interferers. Alternatively, the SAIC-B receiver can offer significant performance gains under single-interferer conditions (and to a lesser extent multiple interferer conditions), but again this may be at the expense of significantly increased receiver complexity.

8. References

[1] GAHS-0015, SAIC ad hoc Rapporteur, “Simulation parameters for GSM SAIC”, Atlanta, GA, USA, January 2003.

[2] GAHS-030023, Motorola, “Candidate exemplary interferer models”, SAIC Ad-Hoc#2, Seattle, U.S.A., March 4-5, 2003

[3] GAHS-030025, Rapporteur, “Exemplary link level assumptions, Configuration 2/3”, SAIC Ad-Hoc#2, Seattle, U.S.A., March 4-5, 2003

[4] Rapporteur, “Working assumptions for capacity estimation for SAIC in unsynchronised networks”, GERAN#16, New York, U.S.A., Aug. 25-29, 2003

[5] GP-031288, Motorola, “SAIC asynchronous link-level performance estimation”, Ft. Lauderdale, U.S.A., June 23-27

[6] GP-031289, Motorola, ”SAIC exemplary link model for Configuration 4”, Ft. Lauderdale, Florida, U.S.A., June 23-27, 2003

[7] GP-031203, Ericsson, “Single antenna interference cancellation – proposed interference levels for configurations 1 and 4”, Ft. Lauderdale, Florida, U.S.A., June 23-27, 2003

[8] GAHS-030029, Motorola, “SAIC system simulation results”, SAIC Ad-Hoc#3, Chicago, U.S.A., October 28-30, 2003

9. Appendix A

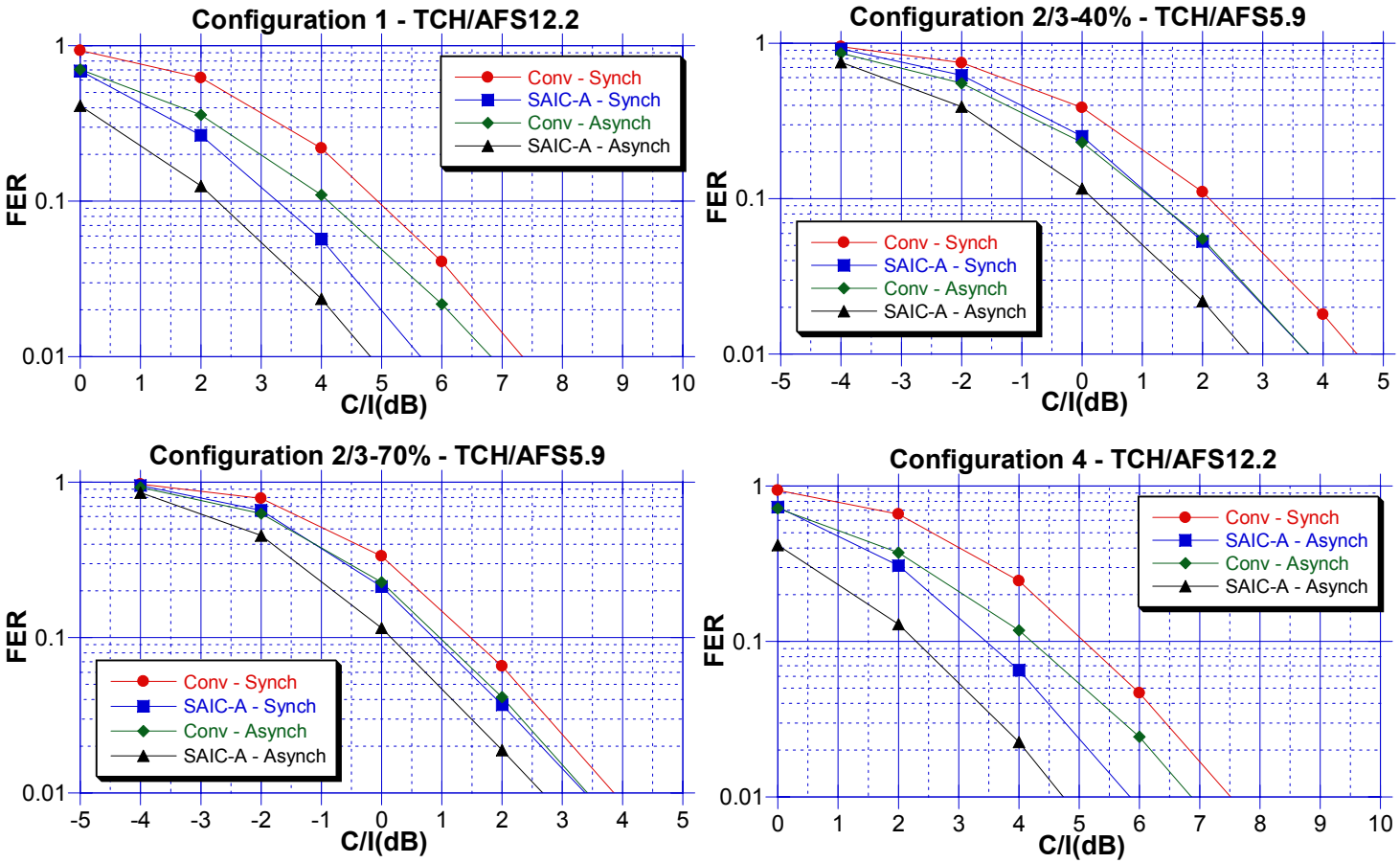

Figure 5 – Mean FER vs. C/I – AMR12.2kbps and AMR5.9kbps by configuration, TU3 IFH.

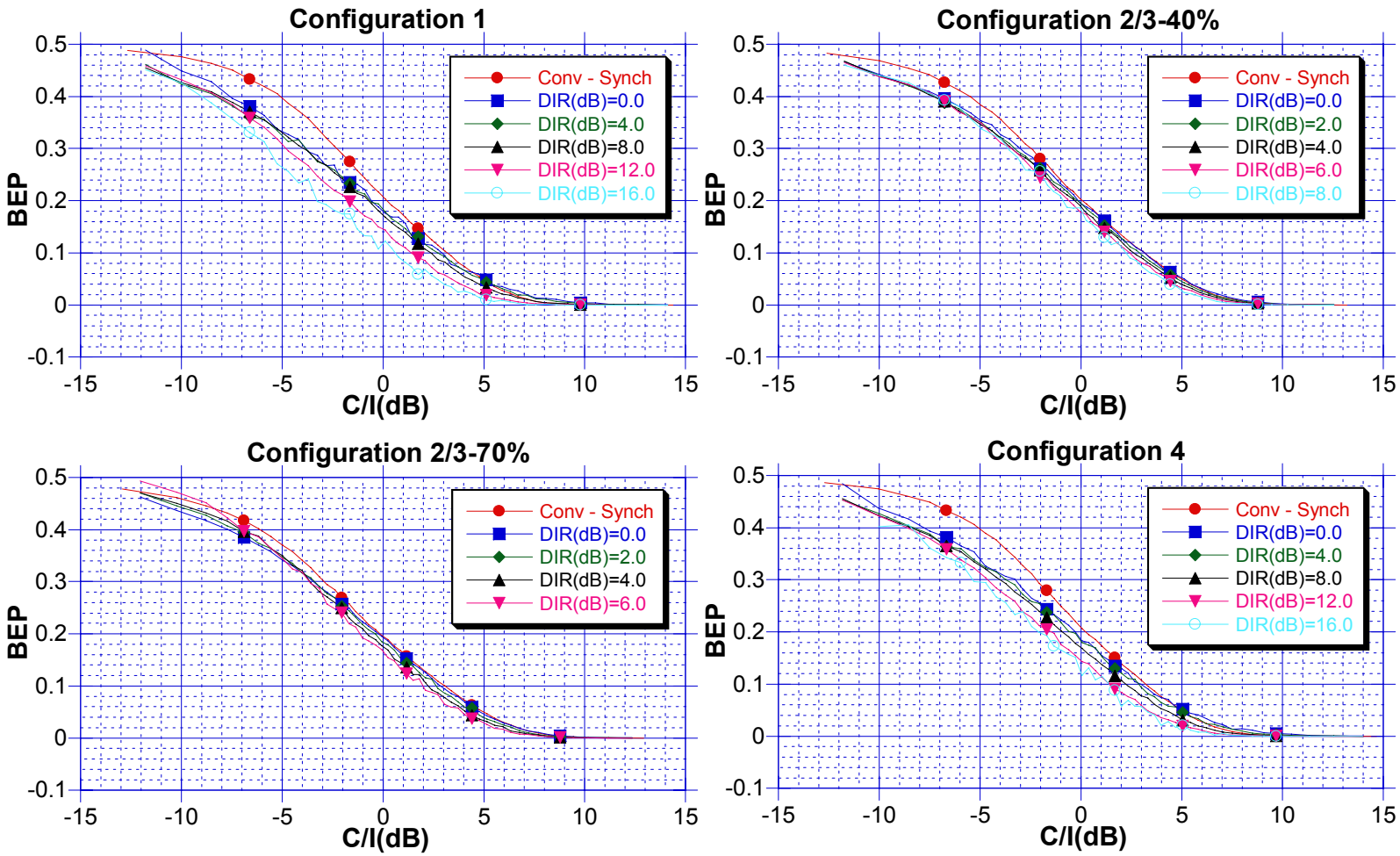

Figure 6 – Synchronous stage-1 mappings ({C/I,DIR}->BEP), configurations 1-4.

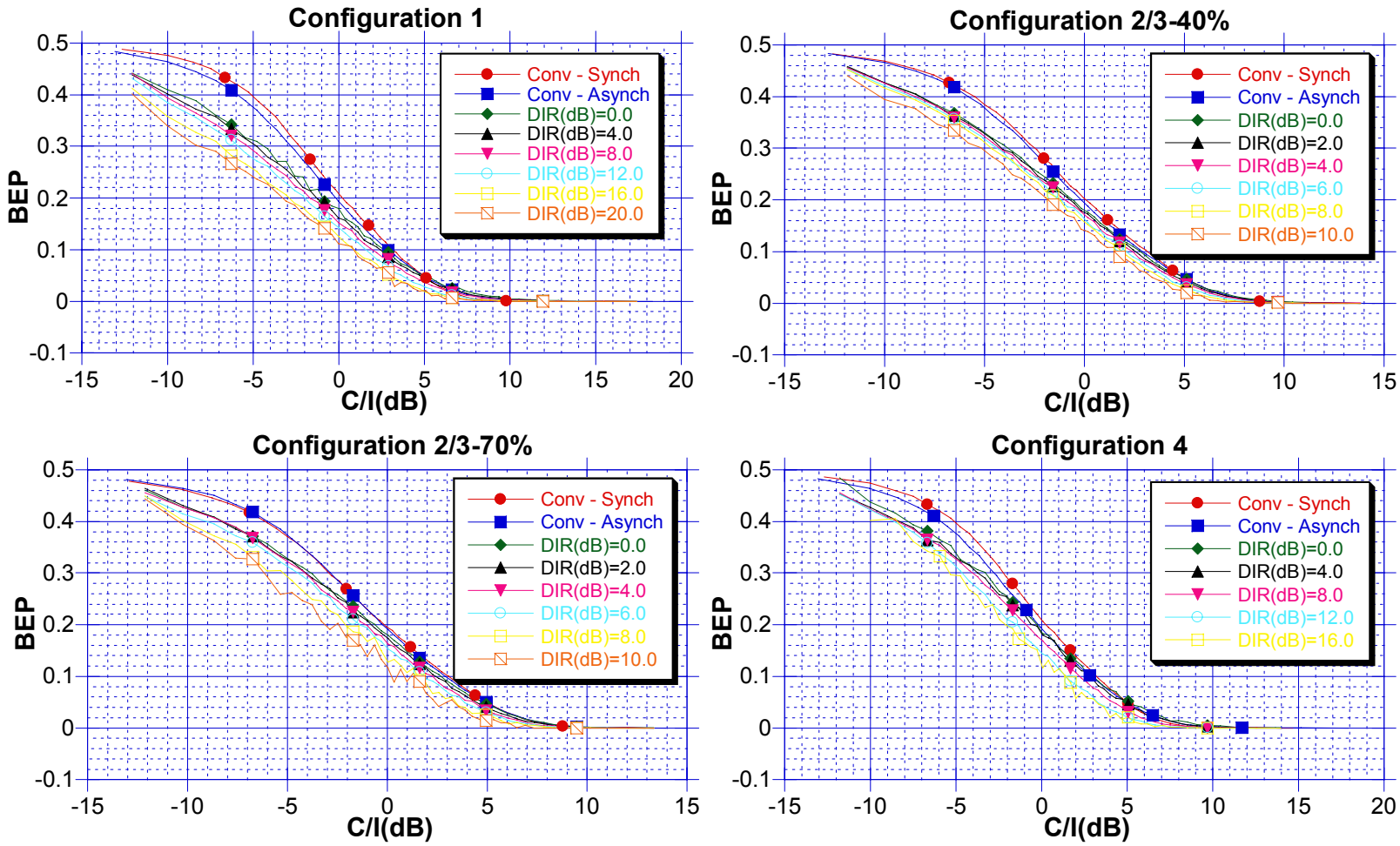

Figure 7 – Asynchronous stage-1 mappings ({C/I,DIR}->BEP), configurations 1-4.

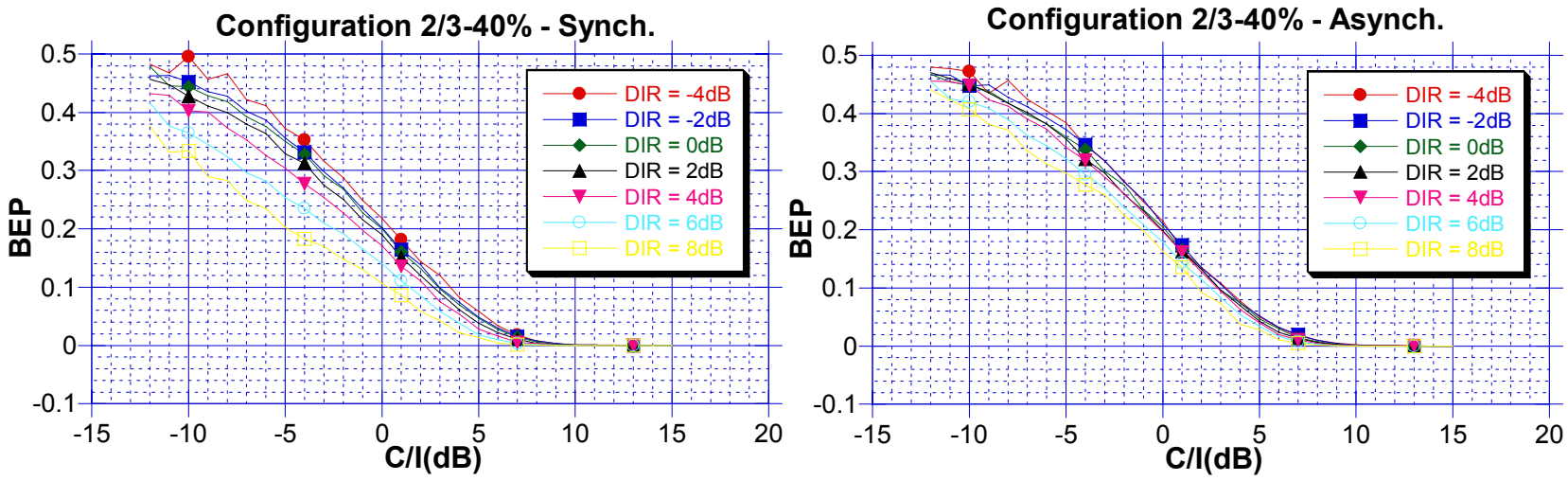

Figure 8 – Sample SAIC-B synchronous and asynchronous stage-1 mappings ({C/I,DIR}->BEP), configuration 2/3-40%.