**3GPP TSG-RAN WG1 Meeting #103-e** **R1-2009761**

**e-Meeting, October 26th – November 13th, 2020**

**Agenda item:** 8.1.2.1

**Source:** Moderator (Qualcomm)

**Title:** Summary #2 of email discussions [103-e-NR-feMIMO-02] for mTRP PDCCH enhancements

**Document for:** Discussion/Decision

# **Round 4 Discussions**

The following have been agreed:

**Agreement**

For PDCCH reliability enhancements, support SFN scheme + Alt 1-1.

* FFS: TCI state activation for CORESET, impact on default beam, BFD resource for BFR

**Agreement**

For PDCCH reliability enhancements with non-SFN schemes, support at least Option 2 + Case 1.

* Maximum number of linked PDCCH candidates is two
* FFS: Details including how the two PDCCH candidates are counted toward the BD limits and impact on overbooking, if any
* Down-select at least one Alt from Alts 1-2 / 1-3 / 2 / 3
* FFS: Linking options such as a fixed rule based on the same PDCCH candidate index, based on start CCE, based on configuration, etc.
  + FFS: additional restriction to facilitate soft combining
* FFS: implicit PUCCH resource determination for >8 PUCCH resources in the resource set, scheduling offset for “timeDurationForQCL”, Out-of-order / in-order definition for PDCCH-to-PDSCH and PDCCH-to-PUSCH, DAI for Type-2 codebook, Slot offset  for scheduling the same PDSCH/PUSCH/CSI-RS/SRS, rate matching PDSCH around the scheduling DCI.
* FFS: whether and how to support for DCI format 2\_x

**Working Assumption**

**For PDCCH reliability enhancements with non-SFN schemes and Option 2 + Case 1, support Alt3 (two SS sets associated with corresponding CORESETs).**

**Agreement**

***For PDCCH reliability enhancements with non-SFN schemes and Option 2 + Case 1, CCEs of the two PDCCH candidates are counted separately following Rel. 15/16 procedures. Further study the BD limit by considering the following***

* ***With respect to the complexity associated with RE de-mapping / demodulation, 2 units are required***
* ***With respect to the complexity associated with decoding, the following assumptions can be further discussed:***
  + ***Assumption 1: UE only decodes the combined candidate without decoding individual PDCCH candidates***
  + ***Assumption 2: UE decodes individual PDCCH candidates***
  + ***Assumption 3: UE decodes the first PDCCH candidate and the combined candidate***
  + ***Assumption 4: UE decodes each PDCCH candidate individually, and also decodes the combined candidate***
* ***Note 1: The Assumptions 1-4 are for discussion purpose only, and they may or may not have specification impact.***
  + ***FFS: The relationship between UE capability, RRC configuration, and the BD limit, and whether the Assumptions 1-4 are relevant for this purpose.***
* ***Note 2: the BD /CCE limit here is counted based on the configuration of PDCCH monitoring capability (e.g. per slot or per span).***

**Conclusion**

Group-common DCI formats (DCI formats 2\_x) are not precluded for multi-TRP PDCCH reliability enhancements and can be discussed with a lower priority compared to UE-specific DCI formats.

Note: Enhancements required for DCI formats 2\_x, if any, can be discussed case-by-case.

## **Intra-slot vs Inter-slot**

One topic that has been mentioned by multiple companies is the support of intra-slot versus inter-slot for PDCCH repetition. The decision may also have impact on linking option, BD limit (if an impact is identified), as well as SS set configurations. On the one hand, limiting the design to intra-slot repetition may simplify specification impact and/or UE implementation. On the other hand, excluding inter-slot may result in less flexibility for the network. Given URLLC use cases, it seems that at least intra-slot repetition should be supported to reduce the latency. Hence, the following proposal can be considered.

***FL Proposal 1: For PDCCH reliability enhancements with Option 2 + Case 1, at least support intra-slot repetition.***

* ***FFS: Whether inter-slot repetition in consecutive slots is supported additionally.***

Please indicate if you support the proposal. Also, please indicate if you have a concern if we agree to both intra-slot and inter-slot.

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| --- | --- |
| Company | Comments |
| Apple | Support intra-slot. We do not see good use case for inter-slot, which requires more spec impact. |
| NEC | We support both intra-slot and inter-slot repetition. |
| ZTE | We are fine to support intro-slot repetition first. But if we are going to support inter-slot repetition, it is better not to restrict consecutive slots for more flexibility.  ***Proposal 1: For PDCCH reliability enhancements with Option 2 + Case 1, at least support intra-slot repetition.***   * ***FFS: Whether inter-slot repetition is supported additionally.*** |
| CATT | Both inter-slot and intra-slot repetition are supported for Option 2+Case 1.  The following revision is suggested:  ***FL Proposal 1: For PDCCH reliability enhancements with Option 2 + Case 1, at least support intra-slot repetition.***   * ***FFS: Whether inter-slot repetition is supported additionally.*** * ***If inter-slot repetition is supported, FFS whether consecutive slots should be used.*** |
| MediaTek | We support both intra and inter slot repetition. We are fine with adding the consecutive slots. For use cases with less strict latency requirement, inter slot repetition can be useful. |
| Nokia/NSB | We are supportive of both intra-slot and inter-slot repetitions.  For edits suggested above by ZTE and CATT, for inter-slot repetitions, it not fully clear how the linking can work if consecutive slots are not assumed. |
| Convida Wireless | Support both intra- and inter-slot repetition. |
| Intel | We support both intra-slot and inter-slot  Inter-slot is beneficial to significantly improve PDCCH blocking probability by jointly scheduling PDCCH over 2 slots at a time as shown in R1-2008978 – yes it comes at a cost of latency (but in FR2 it may be acceptable latency). The reason for improvement is because a UE can be allocated a candidate in slot-1 and another candidate in slot-2 for soft-combining that can improve CCE utilization at the gNB. |
| QC | Support the proposal, and ok with CATT/ZTE edits. Inter-slot requires additional spec changes, e.g., possible changes to BD limit, and Slot offset for scheduling the same PDSCH/PUSCH/CSI-RS/SRS. We are open to study inter-slot further, but intra-slot should have higher priority. |
| Ericsson | We are fine with FL’s proposal. We can agree intra-slot repetition first and further study whether inter-slot repetition needs to be supported. |
| vivo | We support both intra-slot and inter-slot.  We tend to agree with Intel’s comment, and in FR2 due to larger SCS the overall latency shouldn’t be a big issue, for example, the latency of inter-slot repetition with SCS=120kHz is similar to intra-slot repetition with SCS=60kHz.  Comparing intra-slot repetition for PDCCH, the advantage of inter-slot repetition is that the number of BD in every PDCCH repetition is independent in every slot, in some cases PDCCH blocking is avoided, while BD limit per slot may exceed the limit in the case of intra-slot repetition.  We support  ***FL Proposal 1: For PDCCH reliability enhancements with Option 2 + Case 1, ~~at least~~ support intra-slot and inter-slot repetition.***   * ***~~FFS: Whether inter-slot repetition is supported additionally.~~*** * ***For inter-slot repetition, FFS whether consecutive slots should be used.*** |
| NTT Docomo | We support FL proposal. And we are also fine to support inter-slot repetition. |
| Xiaomi | We are fine with the FL proposal 1. We can support intra-slot first and then consider inter-slot. |
| Samsung | Support both intra- and inter-slot repetition due to a lack of available symbols for PDCCH based on the UE capability. Also, we support ZTE’s modification for the FFS point since considering slot format, we think that the restriction of consecutive slots only is not proper. |
| LG | We are fine with FL’s proposal. |
| OPPO | Support. We are open to inter-slot repetition. |
| Spreadtrum | Support. We are also fine for inter-slot repetition. |
| Lenovo&MotM | We support both intra-slot and inter-slot repetitions. |
| Huawei, HiSilicon | We are fine with FL’s proposal. The use case of intra-slot repetition is clear. We can further study the need of inter-slot repetition. |
| FL Summary | All companies support intra-slot.  For inter-slot, the situation is:   * Support: NEC, CATT, MediaTek, Nokia/NSB, Convida Wireless, Intel, vivo, NTT Docomo, Samsung, OPPO, Spreadtrum, Lenovo&MotM * Have concern: Apple, QC   Given some of the reasonings for inter-slot mentioned by companies, and the majority support, as FL, I suggest to agree to both intra-slot and inter-slot so that for the rest of the design (e.g. SS set configuration restrictions, linking options), we can have a unified approach. In that case, we can follow vivo’s suggestion:  ***Updated FL Proposal 1: For PDCCH reliability enhancements with Option 2 + Case 1, ~~at least~~ support intra-slot and inter-slot repetition.***   * ***~~FFS: Whether inter-slot repetition in consecutive slots is supported additionally.~~*** * ***For inter-slot repetition, FFS whether consecutive slots should be used.*** |
| Futurewei | Support the updated FL proposal or the latest in the email discussion.  We have a question of how the “consecutive slots” are defined. If two inter-slot PDCCH transmissions are separated by one or more UL slots, are they still be considered as consecutive? Or at least a maximum separation between the two inter-slot PDCCH transmissions should be defined. |
| FL Summary | @ Futurewei: The intention of consecutive slots here is strictly consecutive. If we conclude that due to TDD patterns, they can be separated by one UL symbol, then they are not consecutive. This is a valid point and requires more discussions as part of FFS when and if inter-slot is agreed.  Based on the latest Email discussions, we can choose between Proposal 1A and 1B:  ***FL Proposal 1A: For PDCCH reliability enhancements with Option 2 + Case 1, at least support intra-slot repetition.***   * ***FFS: Whether inter-slot repetition is supported additionally.***   + ***If inter-slot repetition is supported, FFS whether consecutive slots should be used.***   ***FL Proposal 1B: For PDCCH reliability enhancements with Option 2 + Case 1, support intra-slot and inter-slot repetition.***   * ***For inter-slot repetition, FFS whether consecutive slots should be used.*** |

## **PUCCH Resource determination**

Another issue mentioned by multiple companies is related to implicit PUCCH resource determination when start CCE and # of CCEs of the CORESET play a role in PUCCH resource determination in addition to PRI of the DL DCI. This rule is used when number of PUCCH resources in the PUCCH resource set is larger than 8, in which case the following formula is used [38.213, Section 9.2.3]:



In the case of PDCCH repetition, there are two start CCEs and two # of CCEs in the CORESETs. UE and gNB should unambiguously determine the PUCCH resource irrespective of which PDCCH candidate is actually decoded. Even if the start CCE of the two PDCCH candidates are the same (depending on the decision on linking options), it is possible that # of CCEs of the two CORESETs (in Alt3) are different. Multiple companies mentioned that a rule is needed for this case to resolve the ambiguity. This is also captured in the FFS in one of the agreement. Hence, the following proposal can be used as a starting point, and alternatives can be added based on the inputs (If alternatives are added, there will be no down-selection in this meeting).

***FL Proposal 2: When DL DCI is transmitted via PDCCH repetition (Option2 + Case 1), a fixed rule will be defined to determine the PUCCH resource for HARQ-Ack when the corresponding PUCCH resource set has a size larger than eight.***

* ***Alt 1: ..***
* ***Alt 2: ..***

Please indicate if you support the main part of the proposal, and also indicate if you would like to add Alts (please keep it high-level) for down-selection in the next meeting.

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| Company | Comments |
| Apple | We think one simply way is to make sure the starting CCE index for each PDCCH repetition and number of CCEs for two CORESETs to be the same. This can also be helpful to reduce number of BD for soft combining. |
| NEC | As we have already agreed explicit linkage between two PDCCH candidates, then the straightforward way is to use the starting CCE index and number of CCE based on only one of the two PDCCH candidates. In this way, there is no scheduling restriction for PDCCH.  So we propose one alternative to be:  Alt 1. Parameters (e.g. starting CCE index and number of CCEs) for the first one of the two linked PDCCH candidates is applied for PUCCH resource index determination.  In addition, we think this issue is only one of the listed FFS issues in previous agreement.   * FFS: implicit PUCCH resource determination for >8 PUCCH resources in the resource set, scheduling offset for “timeDurationForQCL”, Out-of-order / in-order definition for PDCCH-to-PDSCH and PDCCH-to-PUSCH, DAI for Type-2 codebook, Slot offset  for scheduling the same PDSCH/PUSCH/CSI-RS/SRS, rate matching PDSCH around the scheduling DCI.   Maybe we can discuss them together. And in our opinion, based on the explicit linkage, using parameters of only one PDCCH candidate can solve almost all of the issues. |
| ZTE | Agree with NEC, **one solution is :** one of two linked PDCCH candidates can be used as a reference PDCCH to solve the following issues  - implicit PUCCH resource determination for >8 PUCCH resources in the resource set  - Out-of-order / in-order definition for PDCCH-to-PDSCH and PDCCH-to-PUSCH  - DAI  - Slot offset  for scheduling the same PDSCH/PUSCH/CSI-RS/SRS  For rate matching, we think following Rel-15/16 procedure is enough, i.e. rate matching for scheduled PDSCH is only around the scheduling PDCCH(s). Specifically, if UE detects both PDCCH repetitions, UE should do rate matching around both PDCCHs. If UE detects only one PDCCH repetition, that means one PDCCH is not transmitted, or one PDCCH is blocked, so there is no much interference to PDSCH. Then, UE only needs to do rate matching around the detected PDCCH.  **Another solution** for PUCCH resource determination for >8 PUCCH resources is up to implementation. At gNB side, gNB can ensure the same PUCCH index derived from two PDCCHs. If not, it will be up to UE to choose one PUCCH, then gNB should detect twice but only one can be received successfully. |
| CATT | Agree with NEC. |
| MediaTek | Agree with Apple. In addition to starting CCE, other parameters like AL and candidate index should be the same. |
| Nokia/NSB | We do not think that the following is a common understanding “it is possible that # of CCEs of the two CORESETs (in Alt3) are different.”.  At least if RAN1 agrees on certain restrictions on CORESETs (e.g same number of CCEs) used for Alt.3, the above may not be valid?  Should not we first discuss any restrictions we foresee on Alt.3 such that we avoid most of FFS items? We feel that companies need time to digest this a bit. |
| Convida Wireless | Agree with NEC. However, for some issues it may be suitable to define the first PDCCH as a reference, while for other issues it may be suitable to define the second PDCCH as a referent. |
| Intel | Agree with the main part of FL proposal. |
| QC | A solution is needed (similar to NEC / ZTE’s solutions) if at least one of start CCE of the two PDCCH candidates, or # of CCEs of the two CORESETs are different. We can decide after linking and CORESET configuration restrictions become more clear. |
| Ericsson | We have a slightly different version of the Alternative proposed by NEC.  Alt2: Starting CCE index and number of CCEs associated with the PDCCH candidate of one of the linked CORESETs is applied for PUCCH resource index determination.  FFS: Which one of the linked CORESETs is used. |
| vivo | In general we agree with Apple’s comment. We should not aim for over complicated MTRP PDCCH enhancement. We also agree with Nokia/NSB whether baseline assumption “#of CCEs of two CORESETs are different” is appropriate. Perhaps we should discuss what restriction can be applied then the remaining issues will be clear. |
| NTT Docomo | We support the main part.  For PUCCH determination, we think having restrictions on CORESETs with same number of CCE will limit the flexibility.  One of the PDCCH candidates needs to be determined as reference. And a same rule should be applied for intra-slot TDM/inter-slot TDM/FDM. We suggest alternative as:  Alt. Starting CCE index/number of CCEs of one of the linked PDCCH candidates/CORESETs is applied for PUCCH resource index determination.  FFS: Which one of the linked PDCCH candidates/CORESETs is used. |
| Xiaomi | Either Apple’s or NEC’s solution is OK.  One way is to make sure the starting CCE index for each PDCCH repetition and number of CCEs for two CORESETs to be the same.  Another way is to use one of two CORESETs as reference. |
| Samsung | Agree with the principle that the reference can be the parameters of one of two PDCCH candidates. However, when the PDCCH repetition is performed by FDM manner, the term “the first one of the two linked PDCCH candidate” can be ambiguous. Hence we think the specific reference for “the first” should be added for FDM case. |
| LG | Whether new rule is needed or not depends on restriction between the two PDCCH candidates. If starting CCE index and # of CCE are the same for the two CORESET, it is not needed. Or, as ZTE mentioned, we can leave it with implementation. We prefer to have further study on this issue before making an agreement. We suggest the following revision.  ***Proposal 2: Further study whether to define a fixed rule to determine the PUCCH resource for HARQ-Ack when the corresponding PUCCH resource set has a size larger than eight When DL DCI is transmitted via PDCCH repetition (Option2 + Case 1), with consideration of some restriction for the two CORESET.*** |
| OPPO | The proposals from NEC and Ericson are good starting points to avoid the potential ambiguity of PUCCH resource.  The implementation solution from ZTE that gNB ensures the PDCCHs indicate the same PUCCH resource is difficult for practical system if inter-slot repetition is supported. The reason is that the hash function is based on the slot index.  We also agree Apple and MTK that some restrictions are needed to reduce the complexity of the whole system and simplify UE implementation (e.g., soft combination), which may include   * The candidate index * The number of CCEs of each CORESET * Aggregation level * CORESET configuration (may impact the filter of PDCCH channel estimator) |
| Spreadtrum | Support the main bullet.  Maybe we should firstly discuss about how to linkage and some restrictions for option 2+case 1+Alt3 considering UE’s complexity and spec workload, and form the basic framework. Then discuss the possible candidate solutions for the listed FFS issues.   * FFS: implicit PUCCH resource determination for >8 PUCCH resources in the resource set, scheduling offset for “timeDurationForQCL”, Out-of-order / in-order definition for PDCCH-to-PDSCH and PDCCH-to-PUSCH, DAI for Type-2 codebook, Slot offset  for scheduling the same PDSCH/PUSCH/CSI-RS/SRS, rate matching PDSCH around the scheduling DCI. |
| Lenovo&MotM | We think PUCCH resource can be selected based on starting CCE index and number of CCEs of one of two linked PDCCH candidates. We support Ericsson’s proposal and the FFS part can be further discussed. |
| Huawei, HiSilicon | The issue can be resolved after the linkage is clearer. If there is any difference on linkage between TDM/FDM based schemes, the consideration here may also be impacted. |
| FL Summary | Companies are generally ok with the proposal. However, multiple companies pointed out that based on the CORESET configuration restrictions / Linking options, a fixed rule may not be needed. To address it, we can add that as one alternative (Alt1). Furthermore, Alt2 and Alt3 are added based on Ericsson’s and ZTE’s suggestions with some edits:  ***Updated FL Proposal 2: When DL DCI is transmitted via PDCCH repetition (Option2 + Case 1), ~~a fixed rule will be defined to determine the~~ for PUCCH resource determination for HARQ-Ack when the corresponding PUCCH resource set has a size larger than eight:***   * ***Alt 1: Ensure same start CCE index (based on linking options) and the same number of CCEs in the two CORESETs (based on CORESET configuration restriction)*** * ***Alt 2: Starting CCE index and number of CCEs in the CORESET of one of the linked PDCCH candidates is applied***   + ***FFS: Which one of the linked PDCCH candidates is used.*** * ***Alt 3: It is up to the UE to determine the PUCCH resource based on the starting CCE index and number of CCEs in the CORESET of any of the two linked PDCCH candidates*** |
| Futurewei | Support the updated FL proposal.  We are fine to further study Alt 1 and Alt 2. |
| FL Summary | Based on the Email discussions, the following can be considered as an offline agreement (bullet mentioned by InterDigital is added) as all comments have been addressed.  ***Offline Agreement: When DL DCI is transmitted via PDCCH repetition (Option2 + Case 1), for PUCCH resource determination for HARQ-Ack when the corresponding PUCCH resource set has a size larger than eight:***   * ***Alt 1: Ensure same start CCE index (based on linking options) and the same number of CCEs in the two CORESETs (based on CORESET configuration restriction)*** * ***Alt 2: Starting CCE index and number of CCEs in the CORESET of one of the linked PDCCH candidates is applied***   + ***FFS:  Which one of the linked PDCCH candidates is used.*** * ***Alt 3: It is up to the UE to determine the PUCCH resource based on the starting CCE index and number of CCEs in the CORESET of any of the two linked PDCCH candidates*** * ***Other alternatives are not precluded.*** |

## **Alternatives**

We can continue to discuss the alternatives based on the following working assumption:

**Working Assumption**

**For PDCCH reliability enhancements with non-SFN schemes and Option 2 + Case 1, support Alt3 (two SS sets associated with corresponding CORESETs).**

We can limit the discussions to Alt 3 and Alt 1-3. The main points to discuss are:

* Complexity difference between Alt 3 and Alt 1-3.
* The need to increase # of CORESETs for Alt 3 (in the absence of CORESETPoolIndex)
* How Alt 1-3 can support FDM.

Please continue the discussions based on above

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| Company | Comments |
| MediaTek | We have some comments on the Alt 1-2, 1-3, and 3.   1. **The number of CORESETs**: CORESET 0 can be also used for PDCCH repetition. If we think the number of CORESETs is not enough, we can increase the number to 4 or 5 like M-DCI MTRP. The number of CORESETs don’t increase the UE complexity. The number of SS sets and MOs increase the UE complexity. For PDCCH repetition, the gNB needs to allocate the same number of RBs (even exactly same RBs) because the entire SS should be repeated. From the following example, 3 alternatives lead to the same UE complexity.      1. **FDM**: Alt 1-3 cannot support FDM as many companies already pointed out. Only Alt 1-2 with the same monitoring occasion can support FDM. Half of candidates map to TRP 1 and the other candidates map to TRP 2. But in this case, SS can be reduced by half which limits scheduling flexibility. Also, the gNB cannot use AL 16+AL16 due to not enough resources or scheduling to another UE. 2. **Spec impact**: Alt 3 has much less spec impact because we need to introduce two TCI states for Alt 1-2 and 1-3. Also, we need to associate each TCI state to each MO (1-2) or each SS set (1-2). 3. **Flexibility**: Alt 3 easily support TDM, FDM, TDM+FDM compared to Alt 1-2 and 1-3.   In addition to the above reasons, each CORESET per TRP aligns with the current design of M-DCI.  Considering super majority of companies are supporting Alt3, I hope Alt 3 can be accepted by the proponents for Alt 1-2 and Alt 1-3. |
| Nokia | We think additional methods are not needed. Let’s try to fix the issues of limitation of CORESETs without introducing a different flavour. |
| Convida Wireless | Same view as Nokia. |
| Intel | We generally agree with MTK.  Its not clear Alt-3 is more complex than Alt-1-3 because hardware complexity at UE is mainly driven by BD/CCE limits  # of CORESETs for Alt-3, we can think of increasing # of CORESETs (although we think 3 CORESETs can also work)  Supporting Alt-1-3 with FDM is complicated. Even if we consider some complicated linkage that allows linking non-overlapping candidates the UE will not be able to use the nested property of CCEs for channel estimation across different candidates. So CCE limit will be violated. Practically we think Alt-1-3 if introduced should be strictly limited to TDM. |
| QC | Agree with Nokia and Intel. In addition, we think complexity-wise, there is no difference as mentioned by MediaTek and Intel.  With respect to Alt 1-3, here is the reason why FDM cannot be supported: To support strict FDM, the two SS sets should occupy the same exact symbols. In Alt 1-3, the RBs are also exactly same, which means they are completely overlapping. Now, if we link candidate x of SS set 1 with candidate y of SS set 2 to support FDM, how does the UE treat candidate y of SS set 1 and candidate x of SS set2? Does it mean that for every CCE, UE needs to do channel estimation two times once based on TCI state 1 assumption and another time based on TCI state 2 assumption? Note that this is not an issue with Alt3 since a) the two CORESETs can be non-overlapping in frequency b) Even if they are overlapping (or partially overlapping), CCEs of “non-overlapped CCEs” limit is counted two times if they are in different CORESETs based on the current spec:  “**CCEs for PDCCH candidates are non-overlapped if they correspond to**  **- different CORESET indexes, or**  **- different first symbols for the reception of the respective PDCCH candidates.**”  While it may not be impossible, in order to support FDM with Alt 1-3, a lot of changes seem to be needed. |
| Ericsson | We have similar view as Nokia and Convida Wireless. From spec impact point of view, we think Alt 3 is sufficient and no further need to agree Alts 1-2 or 1-3. |
| NTT Docomo | We share similar view as Nokia. Alt.3 is sufficient. |
| Xiaomi | We think there is no problem to support FDM with Alt 1-3.  If we link candidate x of SS set 1 with candidate x+1 of SS set 2, Alt 1-3 can support FDM. We think do channel estimation two times for every CCE is not a problem, since the total time of channel estimation is 2M if the number of CCE in the CORESET of Alt 1-3 is M. And for Alt 3, if the number of CCE in each CORESET is M, it needs 2M times channel estimation too.  In addition, there is no problem for PUCCH resource determination with Alt 1-3. |
| Samsung | We also think that Alt 3 is sufficient. |
| LG | For the progress, we don’t object current working assumption. However we don’t think FDM cannot be supported with Alt 1-3. In our view, there are several ways to support FDM for Alt 1-3. In order to avoid double channel estimation for one CCE, which Qualcomm pointed out, we can consider exclusive CCE linkage to SS set 1 and SS set 2. For example, half of CCE in the CORESET is used for SS set 1 and remains are for SS set 2. |
| OPPO | More explanations for Alt.1-2 including reply to MediaTek’s comments on Alt.1-2   1. For Alt.1-2, one possible design is that for the first TCI state, UE follows the Rel-15/16 procedure. Then, for each PDCCH occasion, there can be a “replica” by offset(s) in frequency domain and/or time domain. Everything for the replica is the same except the offset. UE will receive the PDCCH repetition in the “replica” 2. Based on the above design, Alt.1-2 can support FDM by using an offset in frequency domain for the “replica”. There will be no impact on the number of candidates and the size of aggregation levels 3. Alt.2 can support TDM by using an offset in time domain for the “replica” 4. Alt.2 can support TDM+FDM by using an offset in time domain and another offset in frequency domain for the “replica”   Thus, Alt.3 and Alt.1-2 have the same flexibility. Moreover, the PUCCH resource determination (in section 1.2) is simpler for Alt.1-2. |
| Spreadtrum | Share the same view with the majority, Alt.3 is enough. |
| Huawei, HiSilicon | We don’t the difference on the UE complexity between alt 3 and alt 1-3.  On # of CORESETs, we can consider to increase CORESET number even when *CORESETPoolIndex* is absent. But the cases when number of CORESET is not enough needs to be identified.  On the support of FDM, as QC mentioned, it can be supported by Alt 1-3 by association of different candidate IDs, although with increase of channel estimation complexity to some extent.  We can follow the majority to confirm the working assumption. |
| FL Summary | @ Xiaomi: Based on the current spec, one CCE is not counted two times if they are in the same CORESET.  @ LG: Thanks for the compromise. Yes, if we consider half of the RBs of the CORESET for each SS set, then it is possible to support FDM, but this basically means that frequency domain property also becomes a property of the SS set (in addition to TCI state becoming a property of SS set).  @ All: I suggest to confirm the working assumption and move on based on the comments above. This issue has been discussed multiple times, and it is preferred to not come back to it again in the next meeting.  ***FL Proposal 3: Confirm the working assumption:***  ***For PDCCH reliability enhancements with non-SFN schemes and Option 2 + Case 1, support Alt3 (two SS sets associated with corresponding CORESETs).*** |
| Futurewei | Support the updated FL proposal. |
| FL Summary | Based on the latest Email from Yushu, I added the sub-bullet:  ***FL Proposal 3: Confirm the working assumption with the following update:***  ***For PDCCH reliability enhancements with non-SFN schemes and Option 2 + Case 1, support Alt3 (two SS sets associated with corresponding CORESETs).***   * ***This does not require to increase the maximum number of CORESETs per BWP*** |