3GPP TSG-RAN2 Meeting #116e-bis R2-210xxxx

e-Meeting, 16th-27th August 2021

Source: Email discussion Rapporteur (Ericsson)

Title: [Post116-e][514][RACH partitioning] Signaling design (Ericsson)

Agenda item: x.y.x

Document for: Discussion and Decision

# Introduction

This document contains summary of **detailed** input to the email discussion as detailed below:

* [Post116-e][514][RACH partitioning] Signaling design (Ericsson)
* Discussion points on details/principles yet to be defined
* A running CR (based on current status) that also incorporates the above when some kind of direction can be made; maybe with a few, preferable very few, alternatives.
* Deadline: Long

Deadline for company comments and responses to technical isses: 15th December, 12:00 am UTC.

The Rapporteur will attempt to summarize and make updates to the running CR based on progress and consensus.

# General

In a draft running CR for RA partitioning a first draft proposed signalling structure have been implemented.

In the below table, please fill in applicable **detailed** comments, if any, on the draft running CR for RA partitioning.

Note that current agreements made for RA partitioning can be found as an Annex in the draft running CR.

🡪 *Minor comments related to the running CR can be made directly in the CR itself*. However, for discussion points where companies would to present more complex comments or suggestions, the below table should be used.

Suggestion: In the below companies should aim for a technical discussion, not only single view input in order to progress outstanding design principals/details.

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| Company | Section/Item or IE, etc | Detailed comment with motivation | Example code, procedure |
| Intel#1 | RACH-ConfigCommon | We noticed tha feaureCombination-r17 is in 2 places: One in the RACH-ConfigCommon-r17 and another in the featureCombinationPreambles-r17. We think that only the one in the featureCombinationPreambles-r17 is needed when the RACH resource configured is for both RO sharing case and non-RO sharing cases.For the non-RO sharing case, the featureCombinationPreambles-r17 just provides the featureCombination-r17 | Remove the IE featureCombination-r17 in the RACH-ConfigCommon-r17 |
| Intel#2 | FeatureCombinationPreambles-r17 | With the change in Intel#1, the featureCombination-r17 can be made mandatory in FeatureCombinationPreambles-r17. Currently, it is unclear the expected behaviour if this field is absent with the configuration of featureCombinationPreambles-r17 | Remove OPTIONAL for featureCombination-r17 |
| Intel#3 | featureCombinationPreambles-r17 added to RACH-ConfigCommon and RACH-ConfigCommonTwoStepRA | Our understanding is that this new addition can also be applied to legacy 2-step and 4-step RACH configuration. Is this the intended/correct understanding?If so, the preamble partitioning for the other feature combination has to come after the end of the preamble partitioning of the legacy 2-step RACH. If this still needs further discussion, please add an editor note. |  |
| Intel#4 | featureCombinationPreambles-r17 added to RACH-ConfigCommon and RACH-ConfigCommonTwoStepRA | For the additional RACH configuration, we assume that the preamble partitioning will start with the 4-step RACH and will be partitioned with the group A + B of the first feature combination to the group A + B of the last feature combination configured for the 4-step RACH configuration. The preamble partitioning for 2-step RACH will then start from the end of the of the last feature combination configured for the 4-step RACH configuration and the preamble partitioning for the feature combination configured for 2-step RACH will follow as like the 4-step case (i.e. partitioned with the group A + B of the first feature combination to the group A + B of the last feature combination configured for the 2-step RACH configuration).If this still needs further discussion, please add an editor note. | Summarizing the RACH partitioning in the case of shared RO among feature/feature combinations of e.g. F1, F2, F1+F2 with 2-step and 4-step RACH also sharing the RO will be like the following: |
| ZTE#1 | FeatureCombination  | The detailed meaning of each feature bit should be captured somewhere. For example, if the slicing info is not included, then the feature combination is available to all slices. We are fine to capture it in either MAC or RRC. If we capture this in MAC, then a reference to MAC should be added here. For example, …is one of the features of this feature combination as specified in TS 38.321 [3] | ***If we want capture the meaning of each feature bit in RRC, then the following principles can be considered (e.g. the detailed description in the RRC field description):***1. if REDCAP indication is configured for the partition, then the RACH partition is only applicable to the RACH procedure triggered for REDCAP UE where Msg1 identification is required. Otherwise, if REDCAP indication is not configured, then the RACH partition is applicable to non-REDCAP UE and REDCAP UE where Msg1 identification is not required. (FFS how to determine whether Msg1 identification is required or not)
2. if slice info is configured for the partition,then the RACH partition is only applicable to the RACH procedure triggered for the slice. Otherwise, if the slice info is not configured, then the RACH partition is applicable to all slices.
3. if SDT indication is configured, then the RACH partition is only applicable to the RACH procedure triggered for SDT. Otherwise, if SDT indication is not configured, then the RACH partition is applicable to the RACH procedure not triggered for SDT.
4. if CE indication is configured, then the RACH partition is only applicable to the RACH procedure where CE is required. Otherwise, if CE indication is not configured, then the RACH partition is applicable to the RACH procedure where CE is not required. (if CE is considered as part of feature combination)

***If we want to capture it in MAC, then a reference can be added here. For example:******redCap***If present, this field indicates that RedCap is one of the features of this feature combination as specified in TS 38.321 [3].  |
| ZTE#2 | Generic for RO sharingRACH-ConfigCommon-r17FeatureCombinationPreambles-r17 | For RO sharing, we think the following three cases shall be considered:* Case 1: RA resource in R17 RA partition shares the RO with legacy RA resource.
* Case 2: Different types of RA resource within one RA partition share the RO with each other
* Case 3: RA resource in one RA partition share the RO with RA resource from another RA partition

In general, we think all the three cases above shall be supported, and a common structure is preferred.For the detail structure, since RACH-ConfigGeneric is mandatory present in RACH-ConfigCommon. we prefer to introduce a new structure RACH-ConfigCommon-r17 instead of the RACH-ConfigCommon.With the common structure proposed, the FeatureCombinationPreambles is not needed. | RACHPartition-ConfigCommon-r17 ::= SEQUENCE { rachPartition-ConfigID-r17 INTEGER(1..maxRACHAdditionalRACH-r17) rach-ConfigCommon-r17 RACH-ConfigCommon-r17 OPTIONAL, -- Need M msgA-ConfigCommon-r16 MsgA-ConfigCommon-r16 OPTIONAL, -- Cond SpCellOnly2 featureCombination-r17 FeatureCombination-r17 OPTIONAL}RACH-ConfigCommon-r17 ::= SEQUENCE { occasions CHOICE { shared-RO-r17 Shared-RO-r17, separate-RO-r17 Separate-RO-r17 }  groupBconfigured SEQUENCE { ra-Msg3SizeGroupA ENUMERATED {b56, b144, b208, b256, b282, b480, b640, b800, b1000, b72, spare6, spare5,spare4, spare3, spare2, spare1}, messagePowerOffsetGroupB ENUMERATED { minusinfinity, dB0, dB5, dB8, dB10, dB12, dB15, dB18}, numberOfRA-PreamblesGroupA INTEGER (1..64)} OPTIONAL, -- Need R ra-ContentionResolutionTimer ENUMERATED { sf8, sf16, sf24, sf32, sf40, sf48, sf56, sf64}, rsrp-ThresholdSSB RSRP-Range OPTIONAL, -- Need Rrsrp-ThresholdSSB-SUL RSRP-Range OPTIONAL, -- Cond SUL ra-PrioritizationForAccessIdentity-r16 SEQUENCE { ra-Prioritization-r16 RA-Prioritization, ra-PrioritizationForAI-r16 BIT STRING (SIZE (2))},...}Shared-RO-r17 ::= SEQUENCE { rachPartition-ConfigID-r17 INTEGER (1.. maxRACHAdditionalRACH-r17) OPTIONAL, -- Need S shared-RACH-resource ENUMERATED {ra4step,ra2step,raCE,spare} OPTIONAL, -- Need S}Separate-RO-r17 ::= SEQUENCE { rach-ConfigGeneric RACH-ConfigGeneric, totalNumberOfRA-Preambles INTEGER (1..63) OPTIONAL, -- Need S ssb-perRACH-OccasionAndCB-PreamblesPerSSB CHOICE { oneEighth ENUMERATED {n4,n8,n12,n16,n20,n24,n28,n32,n36,n40,n44,n48,n52,n56,n60,n64}, oneFourth ENUMERATED {n4,n8,n12,n16,n20,n24,n28,n32,n36,n40,n44,n48,n52,n56,n60,n64}, oneHalf ENUMERATED {n4,n8,n12,n16,n20,n24,n28,n32,n36,n40,n44,n48,n52,n56,n60,n64}, one ENUMERATED {n4,n8,n12,n16,n20,n24,n28,n32,n36,n40,n44,n48,n52,n56,n60,n64}, two ENUMERATED {n4,n8,n12,n16,n20,n24,n28,n32}, four INTEGER (1..16), eight INTEGER (1..8), sixteen INTEGER (1..4)} }For MsgA, we can have a similar structure above, or we can consider the following one as a simplified version.RACH-ConfigGenericTwoStepRA-r16 ::= SEQUENCE { msgA-PRACH-ConfigurationIndex-r16 INTEGER (0..262) OPTIONAL, -- Cond 2StepOnly msgA-RO-FDM-r16 ENUMERATED {one, two, four, eight} OPTIONAL, -- Cond 2StepOnly msgA-RO-FrequencyStart-r16 INTEGER (0..maxNrofPhysicalResourceBlocks-1) OPTIONAL, -- Cond 2StepOnly msgA-ZeroCorrelationZoneConfig-r16 INTEGER (0..15) OPTIONAL, -- Cond 2StepOnly msgA-PreamblePowerRampingStep-r16 ENUMERATED {dB0, dB2, dB4, dB6} OPTIONAL, -- Cond 2StepOnlyNoCFRA msgA-PreambleReceivedTargetPower-r16 INTEGER (-202..-60) OPTIONAL, -- Cond 2StepOnlyNoCFRA msgB-ResponseWindow-r16 ENUMERATED {sl1, sl2, sl4, sl8, sl10, sl20, sl40, sl80, sl160, sl320} OPTIONAL, -- Cond NoCFRA preambleTransMax-r16 ENUMERATED {n3, n4, n5, n6, n7, n8, n10, n20, n50, n100, n200} OPTIONAL, -- Cond 2StepOnlyNoCFRA...,[[ shared-RachPartition-index INTEGER (0.. maxNrofRACHResourcePool-1) OPTIONAL, -- Need S shared-RACH-resource ENUMERATED {ra4step,ra2step,raCE,spare} OPTIONAL, -- Need S]]} |
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# Summary and proposals

TBD

# Annex (contact details for email discussions)

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| --- | --- | --- |
| Company | Contact name | Contact email |
| Intel | Seau Sian Lim | seau.s.lim@intel.com |
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