TSG-RAN Working Group 4 (Radio) meeting #19 **R4-011231**
Edinburgh, Scotland 3rd-7th September 2001

Source: Motorola

Title: CPICH cancellation, UE sample-time offsets

Agenda item: 9.1

Document for: Discussion

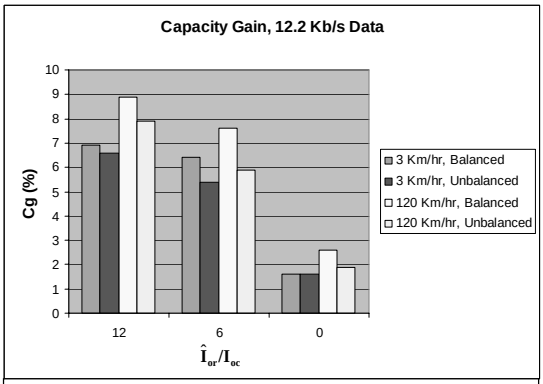
1.0 Introduction

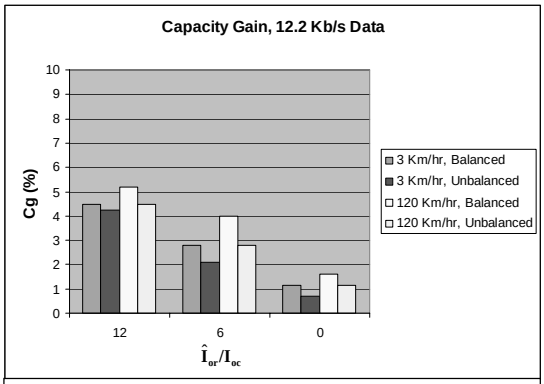
A number of contributions [1]-[4] to 3GPP have pointed out the benefits of CPICH cancellation at the UE. As pointed out in [5] the capacity gain due to CPICH cancellation is best evaluated by system-level simulations rather than link-level simulations, as the link-level performance (SIR vs. BER/BLER) is a function of the cell geometry (*Îor/Ioc*). However, since the UE operates at a given SIR and channel condition, link-level simulations are useful in assessing the performance of the UE for deviations from ideal operating points, such as sample-time offsets. This paper presents link-level simulation results that address this concern. These results should aid in evaluating the performance/cost trade-off for CPICH cancellation.

2.0 Simulation results

A list of simulation assumptions is given in Table 1. These are the same assumptions used in [5], including the salient point that the channel models consist of the following different scenarios: balanced and unbalanced two-ray multipath at 3 and 120 Km/hr. For the unbalanced case the power profile is {0, -6} dB. Additionally, the UE timing offsets for the two fingers associated with the multipath rays are +0.25 and –0.25 chips. A ¼-chip fixed-tracking error is significantly greater than the RMS ray tracking error Motorola would expect to observe under typical operating conditions.

Figure 1 is a repeat of that given in [5][1], i.e., no timing offset is assumed. This figure shows the capacity gain due to CPICH cancellation based on the link-level improvement for a given channel condition and cell geometry. Figure 2 is based on the same set of channel conditions with the inclusion of a ±0.25 chip timing offset at the UE. As can be seen, there is a definite degradation due to this sampling offset. However, it should be noted that there is still a discernable link improvement when CPICH cancellation is used. Consequently, there seems to be no reason for concern that CPICH cancellation would degrade a system in the presence of timing offset by the UE.





---

[1] There is a modification to Figure 1; the capacity gain for the unbalanced, 120 Km/hr, *Ior/Ioc*=12 dB has been changed from 9.1% to 7.9 %. With this correction there is the consistency with the data that the unbalanced condition performs worse than balanced, as it should.

3.0 Conclusion

The results presented in this contribution indicate that CPICH cancellation will not cause system degradation due to UE sample-time errors. Furthermore, even with a rather large timing error, there still is a noticeable link-level improvement when CPICH cancellation is activated compared to no CPICH cancellation.

These results should help determine if CPICH cancellation provides sufficient capacity gain, when compared to the complexity increase, for inclusion in the UE.

4.0 Reference

[1] 3GPP TSGR1-00-1371, "CPICH interference cancellation as a means for increasing DL capacity," Intel Corporation, Nov. 2000.

[2] 3GPP TSGR1-00-0030, "Further Results on CPICH Interference Cancellation as A Means for Increasing DL Capacity," Intel Corporation, Jan. 2001.

[3] 3GPP TSGR4-01-0238, "CPICH Interference Cancellation as a Means for Increasing DL Capacity," Intel Corporation, Feb. 2001.

[4] 3GPP TSGRP-01-077, "Mitigating the Effect of CPICH Interference at the UE," Intel Corporation, Mar. 2001.

[5] 3GPP TSGR4-01-0967, "CPICH cancellation," Motorola, July 2001.

Annex A Simulation assumptions

Table 2. Parameters used for link level evaluation

Item	Parameter
Data rate	12.2, 144 Kb/s
Channel	2 Ray (balanced), and 2 Ray 0, -6 (unbalanced)
Ior/Ioc	6 dB
Doppler	3 and 120 Km/hr
Power control	Inner-loop ON
BLER target	12.2 Kb/s 1%, 144 kb/s 10%
UE Finger Timing Offset	Figure 1: none Figure 2: +0.25 chip - finger 1, -0.25 chip - finger 2