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Amendment 1
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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Packet over Transport aspects – Synchronization, quality and availability targets

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

Network limits for time synchronization in packet networks

Amendment 1

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Amendment 1 to Recommendation ITU-T G.8271.1/Y.1366.1 (2013)

Network limits for time synchronization in packet networks: Amendment 1

Summary

Amendment 1 to Recommendation ITU-T G.8271.1/Y.1366.1 (2013) provides the following updates:

- Further details on Network Limits at reference point C.
- Updates in the HRM.
- Updates on the examples of the design options.
- Updates on mitigation of time error due to synchronous Ethernet transients.

Amendment 1 to Recommendation ITU-T G.8271.1/Y.1366.1 (2013)

Amendment 1 Network limits for time synchronization in packet networks: Amendment 1

1 Clause 7 - Network Limits

Replace Clause 7 by the following:

7 Network Limits

The following main (worst case) scenarios have been identified and are considered in the definition of the relevant network limits:

- Deployment Case 1: Time distribution chain with T-TSC integrated in the End Application and End Application with a distributed architecture.
- Deployment Case 2: Time distribution chain with a T-TSC external to the End Application and End Application with a distributed architecture. Note: a specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

The above deployment cases are shown in Figure 1.

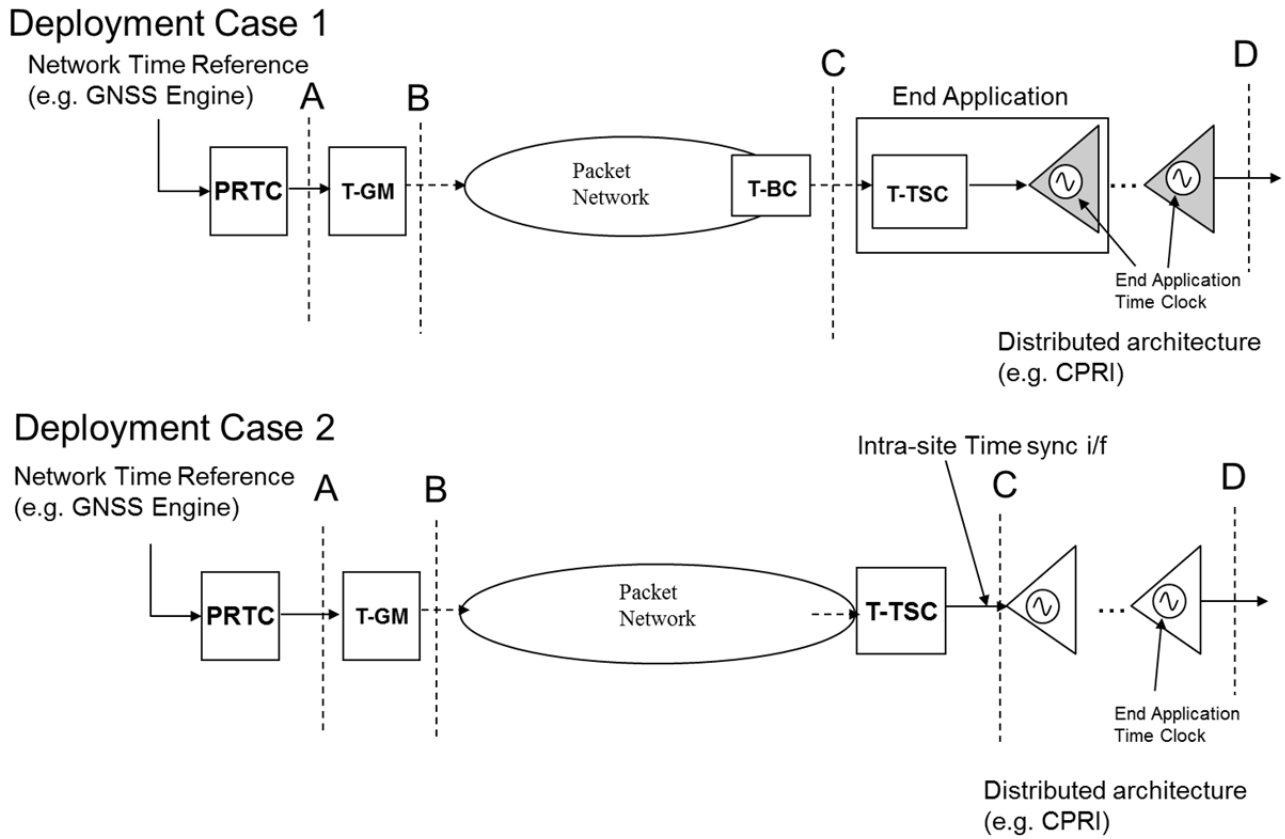

Figure 1- Time synchronization deployment cases

Note: an example of distributed architecture is in case of mobile applications where the base stations have the base band unit (also called REC, Radio Equipment Control) connected remotely to the Radio Units (also called RE, Radio Equipment). In this case a point to point connection (e.g. via

fiber) is assumed and chain topologies are possible. The time error budget applicable to this connection is assumed to be 150 ns; the details on the chain topology are for further study.

2 Clause 7.3 - Network Limits at reference point C

Replace Clause 7.3 by the following:

7.3 Network limit at reference point C

The limits given in this clause represent the maximum permissible levels of phase/time error and noise at interfaces within a packet network in charge of distributing phase/time synchronization according to the applications corresponding to the class 4 mentioned in table 1/G.8271.

The limits applicable to other classes at the reference point C are for further study.

The noise generated by a chain of T-BC is characterized by two main aspects:

- the constant time error produced by the chain, for instance due to various fixed and uncompensated asymmetries (including the PRTC);
- the dynamic time error produced by the various components of the chain (including the PRTC).

The network limits applicable at reference point C are expressed in terms of two quantities:

- the maximum absolute time error: max |TE|, which includes all the noise components, i.e., the constant time error and dynamic time error
- a suitable metric applied to the dynamic time error component (note: the calculation of maximum time interval error (MTIE) and time deviation (TDEV) are considered as appropriate)

The limits given below shall be met for all operating conditions (except during PTP rearrangements and long holdover conditions in the network that are for further study; see also examples in Appendix V), regardless of the amount of equipment preceding the interface. In general, these network limits are compatible with the minimum tolerance to time error and noise that all equipment input ports are required to provide. Further guidance about how to design a phase/time distribution network is provided in Appendix V of this Recommendation.

The limits are:

- Maximum absolute time error network limit applicable at the reference point C: max |TE| ≤ 1100 ns.

Dynamic time error network limit applicable at the reference point C: the specification in terms of MTIE is presented in the figure and table below. The specification in terms of TDEV is for further study.

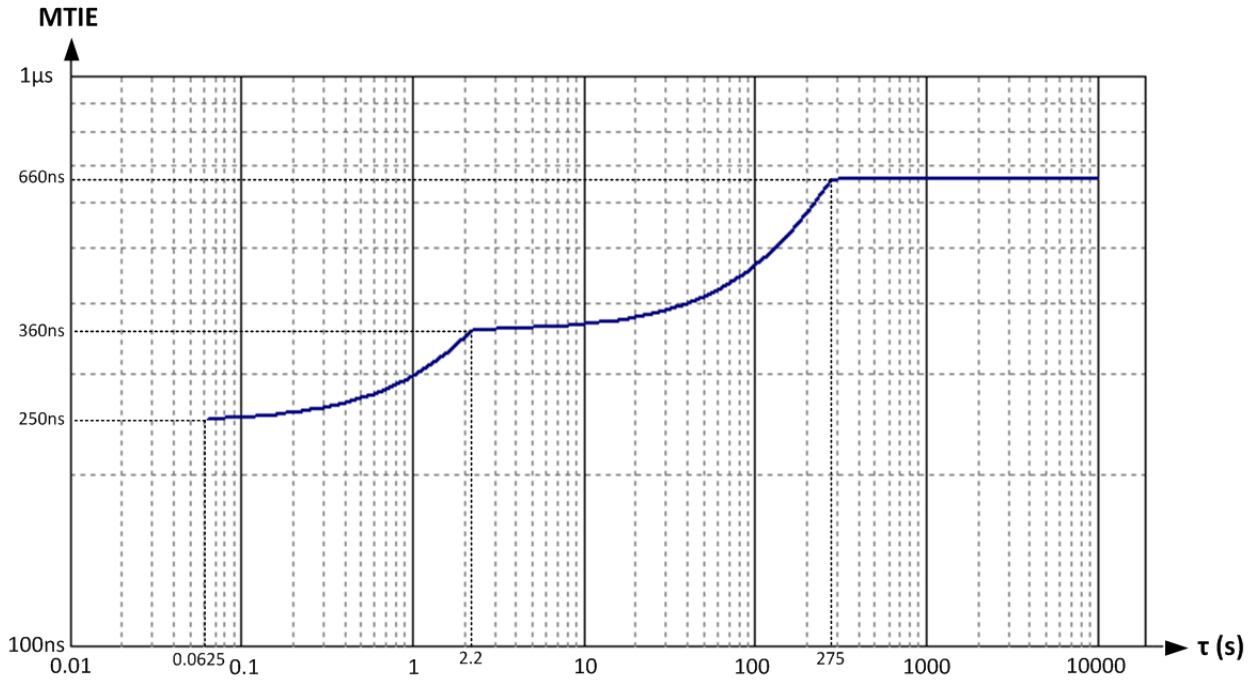

Figure 2 – Dynamic Time Error network limit (MTIE)

Table 1 – Dynamic Time Error network limit expressed in MTIE

MTIE limit (ns)	Observation interval, τ (s)
250	0.0625
247 + 51.1τ	0.0625 < τ ≤ 2.2
357 + 1.1τ	2.2 < τ ≤ 275
660	275 < τ ≤ 10000

Note: a filter with bandwidth of 0.1Hz is applied to the TE samples measured at the packet timing interface prior to evaluating the max |TE|, MTIE and TDEV. Additional details on the test equipment characteristics and measurement period are also for further study.

Note: the need for a measurement filter on the 1 PPS output is for further study.

Specification in terms of high frequency noise is for further study.

3 Appendix II - HRMs used to derive the network limits

Replace Appendix II by the following:

Appendix II

HRMs used to derive the network limits

(This appendix does not form an integral part of this Recommendation)

II.1 HRM composed of T-BCs

The HRM models that are presented in the following sections are applicable to the network reference models defined in Figure 4/G.8271 and Figure 1. This is essential to derive the network limits between point 'B to C' when the packet network consists of network elements with T-BCs.

The purpose of these HRMs is to:

- Establish reasonable worst-case network models for phase/time distribution using T-BCs
- Derive network limits and verify that they are consistent with performance requirements. Some of the performance requirements are summarized in Table 1/ G.8271.
- Construct end-to-end phase and time error budget.

To determine the network limits, the most important aspects that need to be considered when a reference network is constructed are those that influence the accumulation of phase and time error of a reference "packet time signal" that is transported, and some of these are:

- Specification of individual clocks and their noise specifications. In this case Rec. G.8273 shall be considered for the characteristics of the clock implemented in the T-BC. The model of the T-BC for noise accumulation simulations is described in Appendix I.
- The composition of a synchronization chain, cascade of clocks and ordering of clocks. This is defined by the related HRM.
- Other sources of errors besides the noise generated by clocks. These are described in Appendix I of G.8271.

The following HRMs are based on a shorter chain of 12 clocks and a longer chain of 22 clocks.

II.1.1 Hypothetical Reference Model (HRM) without physical layer frequency support from the network

The reference chain below shows a T-GM (Telecom Grandmaster Clock) and a T-TSC (Telecom Time Slave Clock) interconnected by a number of T-BC (Telecom Boundary Clocks).

In this HRM-1 model, both frequency and time are transported via PTP. Both frequency and time follow the same synchronization path. The T-GM acts as both the source of frequency and time (e.g., the T-GM can receive its time and frequency from a GNSS receiver).

At the end of the chain, the phase/time reference is delivered to an end application (e.g. a mobile base station). Two cases are possible and are represented in the figure below:

- The T-TSC is embedded in the end application

- The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g. 1PPS interface). Note: a specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

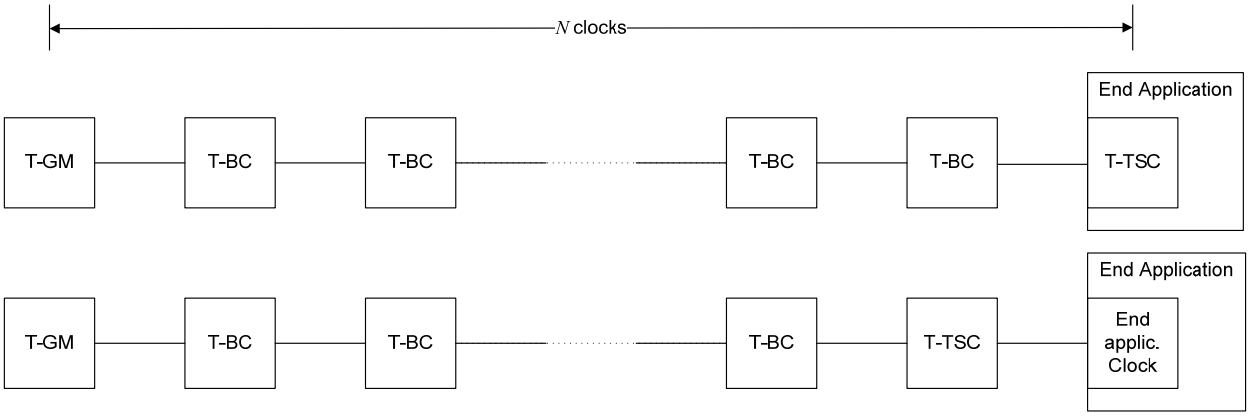

Figure II.1 – HRM-1 without physical layer frequency support

The number of clocks *N* cascaded in the HRM-1 for the shorter chain is 12. It corresponds to:

- 1 T-GM, 10 T-BC and 1 T-TSC for the case of a T-TSC embedded in the end application
- 1 T-GM, 9 T-BC, 1 T-TSC and the end application clock for the case of a T-TSC external to the end application

The number of clocks *N* cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- 1 T-GM, 20 T-BC and 1 T-TSC for the case of a T-TSC embedded in the end application
- 1 T-GM, 19 T-BC, 1 T-TSC and the end application clock for the case of a T-TSC external to the end application

NOTE – Noise accumulation in networks without physical layer frequency synchronization support is for further study.

II.1.2 Hypothetical Reference Models (HRM) with physical layer frequency support from the network

The reference chains below represent the cases where phase/ time is transported via PTP and frequency via SDH/synchronous Ethernet.

Note: the analysis has been done with a synchronous Ethernet network based on option 1 EECs (see G.8262).

<u>Congruent scenario</u>

In this HRM-2 model, both frequency and phase/time follow the same synchronization path.

At the end of the chain, the phase/time reference is delivered to an end application (e.g. a mobile base station). Two cases are possible and are represented in the figure below:

- The T-TSC is embedded in the end application
- The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g. 1PPS interface). Note: a specific equipment implementation may also be based on implementing a T-BC

function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

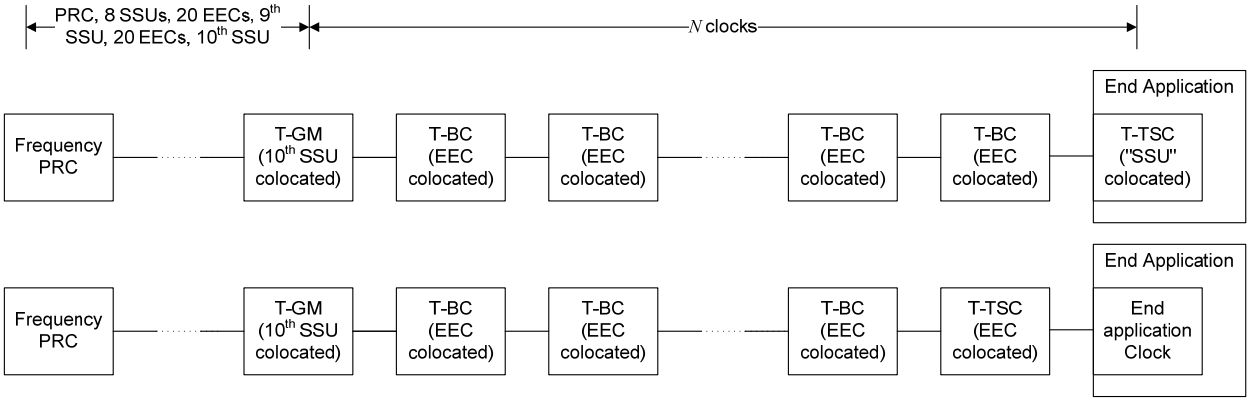

Figure II.2 – HRM-2 with physical layer frequency support – congruent scenario

The number of clocks *N* cascaded in the HRM-2 for the shorter chain is 12. It corresponds to:

- 1 T-GM, 10 T-BC and 1 T-TSC for the case of a T-TSC embedded in the end application
- 1 T-GM, 9 T-BC, 1 T-TSC and the end application clock for the case of a T-TSC external to the end application

The number of clocks *N* cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- 1 T-GM, 20 T-BC and 1 T-TSC for the case of a T-TSC embedded in the end application
- 1 T-GM, 19 T-BC, 1 T-TSC and the end application clock for the case of a T-TSC external to the end application

The following physical layer frequency clocks are co-located with the PTP clocks:

- For the T-GM: an SSU supporting phase/time transport
- For the T-BC: an EEC supporting phase/time transport
- For the T-TSC external to the end application: an EEC supporting phase/time transport
- For the T-TSC embedded in the end application: the clock supporting phase/time transport is for further study. The initial assumption is that this clock might be close to the characteristics of an SSU (e.g. equivalent type of oscillator, but some characteristics of the clock may be different, e.g. different bandwidth, etc.). For the purpose of the simulations it is assumed that this clock is the only timing function of the end application (no other clock is cascaded after).

The SDH/synchronous Ethernet reference chain is a full G.803 reference chain with the EECs as close to the end of the chain as possible: a PRC, followed by 8 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU (co-located with the T-GM), followed by 9 EECs (each co-located with a T-BC) related to the shorter chain or 19 EECs (each co-located with a T-BC) related to the longer chain, followed by a final EEC (co-located with the T-TSC external to the end application or with a last T-BC). A final clock is at the end of the chain: either the “end application clock”, or a clock co-located with the T-TSC embedded in the end application.

<u>Non-congruent scenario</u>

In this HRM-3 model, phase/time and frequency synchronization follow different synchronization paths (i.e., phase/time is distributed horizontally and frequency vertically). This model is similar in spirit to Figure A.1/G.823 and is used to represent a possible worst-case when PTP and SDH/synchronous Ethernet are used.

At the end of the chain, the phase/time reference is delivered to an end application (e.g. a mobile base station). Two cases are possible and are represented in the figures below:

- The T-TSC is embedded in the end application
- The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g. 1PPS interface). Note: a specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

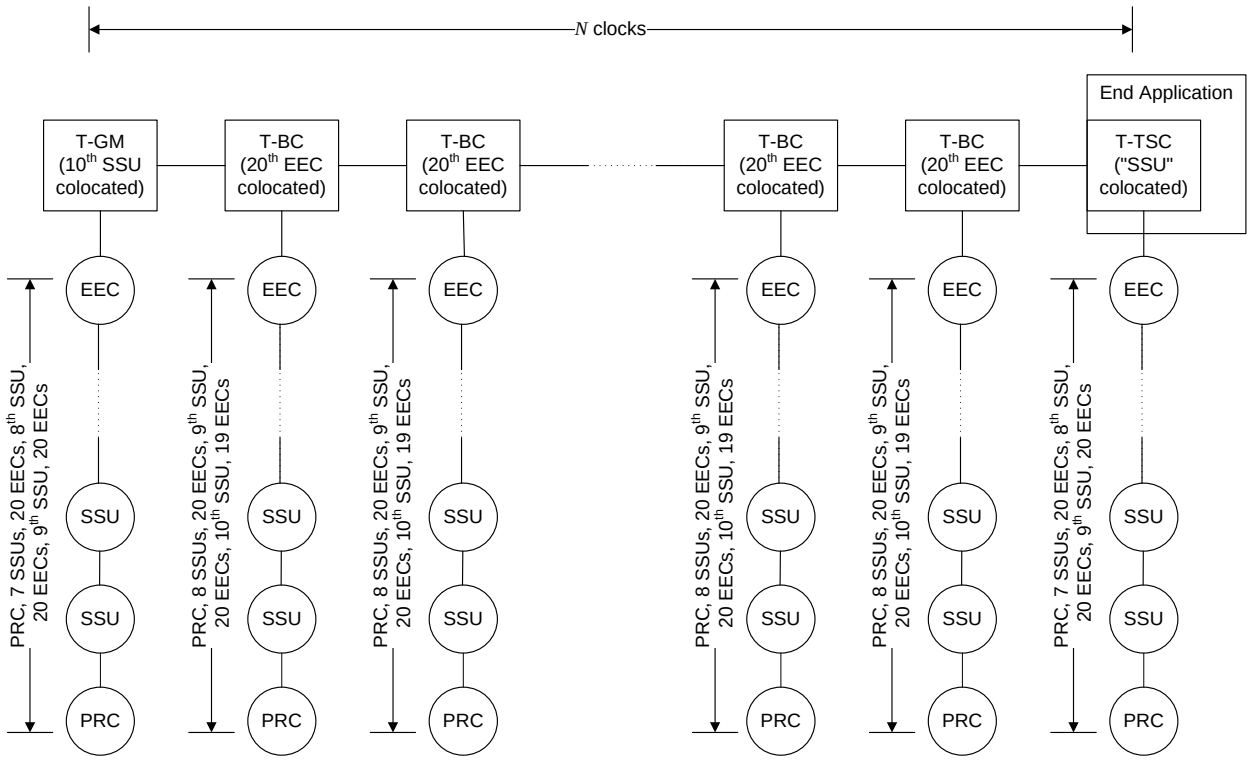

Figure II.4 – HRM-3 with physical layer frequency support – non-congruent scenario, Deployment case 1

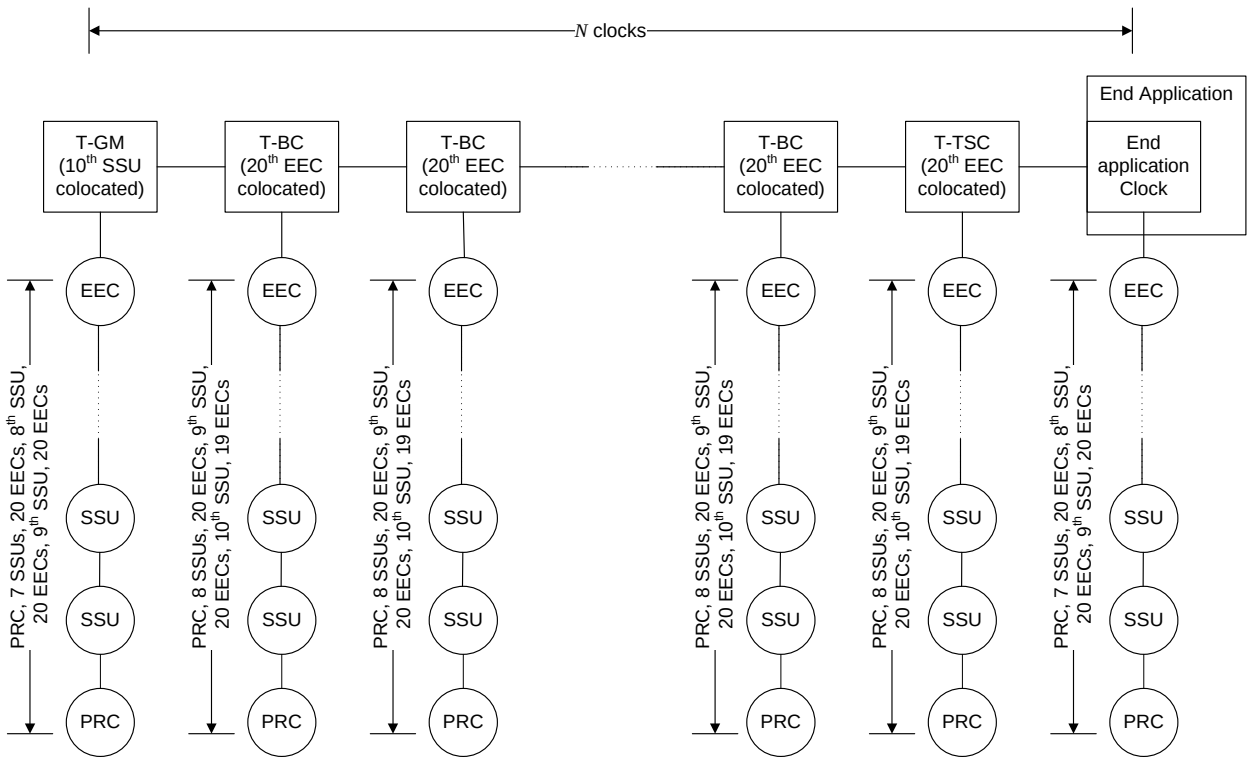

Figure II.3 – HRM-3 with physical layer frequency support – non-congruent scenario, Deployment case 2

The number of clocks *N* cascaded in the HRM-3 for the shorter chain is 12. It corresponds to:

- 1 T-GM, 10 T-BC and 1 T-TSC for the case of a T-TSC embedded in the end application
- 1 T-GM, 9 T-BC, 1 T-TSC and the end application clock for the case of a T-TSC external to the end application

The number of clocks *N* cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- 1 T-GM, 20 T-BC and 1 T-TSC for the case of a T-TSC embedded in the end application
- 1 T-GM, 19 T-BC, 1 T-TSC and the end application clock for the case of a T-TSC external to the end application

The following physical layer frequency clocks are co-located with the PTP clocks:

- For the T-GM: an SSU supporting phase/time transport
- For the T-BC: an EEC supporting phase/time transport
- For the T-TSC external to the end application: an EEC supporting phase/time transport
- For the T-TSC embedded in the end application: the clock supporting phase/time transport is for further study. The initial assumption is that this clock might be close to the characteristics of an SSU (e.g. equivalent type of oscillator, but some characteristics of the clock may be different, e.g. different bandwidth, etc.). For the purpose of the simulations it is assumed that this clock is the only timing function of the end application (no other clock is cascaded after).

The SDH/synchronous Ethernet reference chain is a full G.803 reference chain with the EECs as close to the end of the chain as possible (the final SSU may be at the end of the chain):

- For the PTP clocks supported by an EEC: a PRC, followed by 8 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU, followed by 19 EECs, the 20th EEC being integrated in the T-BC or T-TSC clock.
- For the PTP clocks supported by an SSU: a PRC, followed by 7 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU, followed by 20 EECs, the 10th SSU being integrated in the T-GM or T-TSC clock .

4 Appendix V - Example of design options

Replace Appendix V by the following:

Appendix V

Example of design options

(This appendix does not form an integral part of this Recommendation)

As described in Appendix IV the network limits are expressed in terms of the maximum time error, max |TE| and this is the result of two main components:

- the dynamic time error component, $dTE(t)$,
- the constant time error component cTE,

In order to take into account

a the internal noise sources of the end application, (indicated by TE_{EA})

b the residual noise caused by the dynamic time error component, and

c short holdover at the End Application during rearrangements in the synchronization network (indicated by TE_{REA}),

the network limit applicable at reference point C expressed in terms of maximum absolute time error must satisfy the following relationship:

$$\max |TE| \leq (TE_D - TE_{EA} - TE_{REA}) \qquad \text{(V-1)}$$

with

$$|(cTE + dTE')| + TE_{HO} \leq \max |TE| \qquad \text{(V-2)}$$

Where TE_D indicates the network limit at reference point D expressed in terms of maximum absolute time error, TE_{HO} represents the budget allocated to holdover and rearrangements in the network and $|dTE'|$ is the maximum absolute value of a filtered version of the dynamic time error component $dTE(t)$. In practice dTE' estimates the dynamic component of the time error at the output of the End Application.

Note: the End Application is not required to handle long time synchronization holdover periods but only short interruptions that could be caused by network rearrangements. Time synchronization and rearrangements that may happen in the network and that are modeled by TE_{HO} are included in the network limits. As a first approximation, TE_{REA} and TE_{HO} shall not be considered at the same time; in fact, TE_{REA} assumes that the End Application enters holdover as soon as a failure is detected in the network, while TE_{HO} assumes that the End Application continues to be locked to the incoming reference and in this case there is no need to allocate a budget to TE_{REA}.

Note: the terms cTE and dTE' in the previous relationship are not measured separately, but indicate the components that build max |TE|. In the worst case, cTE and dTE' are both of the same polarity, but in a specific deployment they may partly compensate each other if the polarity is different.

The simulations performed have shown that is possible to limit $|dTE'|$to 200 ns or less (i.e., in the worst case $|dTE'| = 200$ ns), and this value is considered in the time error budgeting analysis. Refer to Appendices I and II for further information on these simulations.

Note: in order to meet the TE_D limits, the End application shall tolerate noise at points C. In case $dTE(t)$ exceeds the target limit of 200 ns, the end application should provide appropriate filtering to reduce the noise at reference point D to the value of dTE', expressed in terms of maximum absolute time error. Further information is provided in Appendix VI.
Note: the time to restore (e.g., time to lock to a secondary time-synchronization reference) at the end application depends on the availability of physical frequency synchronization support and on the characteristics of the clock implemented in the end application.
Further information on the protection scenarios and related budget is provided in this Appendix and in G.8275.

Based on (V-1) and (V-2), the following applies:

$$|cTE| \leq TE_D - (TE_{EA} + TE_{HO} + dTE') \qquad \text{(V-3)}$$

or, in case the End Application enters holdover during network rearrangements,

$$|cTE| \leq TE_D - (TE_{EA} + TE_{REA} + dTE'). \qquad \text{(V-3)'}$$

Assuming the worst case of $|dTE'| = 200$ ns, and $TE_{EA} = 150$ ns,

$$|cTE| \leq TE_D - (350 \text{ ns} + TE_{HO}) \qquad \text{(V-4)}$$

or, in case the End Application enters holdover during network rearrangements,

$$|cTE| \leq TE_D - (350 \text{ ns} + TE_{REA}) \qquad \text{(V-4)'}$$

The constant time error component *cTE* is due to static contributions to the time error, mainly related to link asymmetries and PTP clock (T-BC, T-GM and T-TSC) constant time error accumulation. Note: *cTE* can be considered approximately constant over time assuming there are no changes in the network (e.g. re-routing).

In particular *cTE* can be expressed as follows:

$$|cTE| = ce_{ref} + ce_{ptp_clocks} + ce_{link_asyms}, \qquad \text{(V-5)}$$

where ce_{ref} is the accuracy of the PRTC as specified in G.8272, ce_{ptp_clocks} is the sum of PTP clocks constant time error as planned to be defined as part of the T-BC specification, and ce_{link_asyms} is the overall time error due to link asymmetries. ce_{ptp_clocks} for *m* number of PTP clocks (T-GM, T-BC or T-TSC) in a chain can be expressed as follows:

$$ce_{ptp_clocks} = \sum_{n=1}^{m} ce_{ptp_clock,n}, \qquad \text{(V-6)}$$

where $ce_{ptp_clock,n}$ is the constant time error for each PTP clock.

ce_{link_asyms} for *m*+1 number of links can be expressed as follows:

$$ce_{link_asyms} = \sum_{n=1}^{m+1} ce_{link_asym,n}, \qquad \text{(V-7)}$$

where $ce_{link_asym,n}$ is the time error due to link asymmetry for each link.

Assuming Level of accuracy 4 as per Table 1/G.8271 (i.e. TE_D = 1.5 us) and that ce_{ref} = 100 ns, this leads to:

$$cTE = ce_{ref} + ce_{ptp_clocks} + ce_{link_asyms} \leq 1500 \text{ ns} - 350 \text{ ns} - TE_{HO} = 1150 \text{ ns} - TE_{HO}, \quad \text{(V-8)}$$

and therefore

$$ce_{ptp_clocks} + ce_{link_asyms} + TE_{HO} \leq 1150 \text{ ns} - 100 \text{ ns} = 1050 \text{ ns}; \quad \text{(V-9)}$$

or, in case the End Application enters holdover during network rearrangements:

$$|cTE| = ce_{ref} + ce_{ptp_clocks} + ce_{link_asyms} \leq 1500 \text{ ns} - 350 \text{ ns} - TE_{REA} = 1150 \text{ ns} - TE_{REA}, \quad \text{(V-10)}$$

and therefore

$$ce_{ptp_clocks} + ce_{link_asyms} + TE_{REA} \leq 1150 \text{ ns} - 100 \text{ ns} = 1050 \text{ ns}. \quad \text{(V-11)}$$

For the case of an HRM of 10 T-BCs, of constant TE of 50 ns (T-BC with Constant Time Error Class A, see G.8273.2) and assuming that the constant time error for the T-GM also is 50 ns, this leads to

$$ce_{ptp_clocks} = 50 \text{ ns} + (10 \times 50 \text{ ns}) = 550 \text{ ns}, \quad \text{(V-12)}$$

and, therefore, in the worst case

$$TE_{HO} + e_{link_asyms} \quad 1050 \text{ ns} - 550 \text{ ns} = 500 \text{ ns}; \quad \text{(V-13)}$$

or, in case the End Application enters holdover during network rearrangements:

$$TE_{REA} + e_{link_asyms} = 1050 \text{ ns} - 550 \text{ ns} = 500 \text{ ns} \quad \text{(V-14)}$$

For the case of an HRM of 20 T-BCs, of constant TE of 20ns (T-BC with Constant Time Error Class B, see G.8273.2), and assuming that the constant time error for the T-GM also is 20ns, this leads to

$$ce_{ptp_clocks} = 20 \text{ ns} + (20 \times 20 \text{ ns}) = 420 \text{ ns}, \quad \text{(V-15)}$$

and, therefore, in the worst case

$$TE_{HO} + e_{link_asyms} = 1050 \text{ ns} - 420 \text{ ns} = 630 \text{ ns}; \quad \text{(V-16)}$$

or, in case the End Application enters holdover during network rearrangements:

$$TE_{REA} + e_{link_asyms} = 1050 \text{ ns} - 420 \text{ ns} = 630 \text{ ns} \quad \text{(V-17)}$$

Note: the deployment of long chain of clocks requires particular attention in the network planning (e.g. in the control of link asymmetries, also after network rearrangements), for which the design of networks with shorter chain of clocks might be often considered more appropriate.

In order to provide an example on how time error can be allocated in a typical network deployment, some consideration can be made on potential network failure conditions in order to evaluate possible values for TE_{HO} while meeting the overall requirement

$|cTE + dTE'| + TE_{HO} \leq \max |TE| = 1100$ ns, as per clause 7.2.

The long-term holdover condition is handled as a special case where the 1.5 µs limit is exceeded, assuming this is a particularly rare event. The time error due to the holdover in this case is assumed to be, in the worst case, 2400 ns. Short-term failure conditions should instead be handled within the

1.5 us requirement. In particular, there are two main short-term failure conditions that can be considered relevant:

a) T-GM change (e.g., due to loss of PRTC traceability of one of the redundant GMs in the network). A typical case is when the End Application enters holdover for a short period (e.g. 1 minute)

b) Short interruption of the GNSS signal (e.g. 5 minutes), As an example this might be relevant for a case of Synchronous Ethernet (or internal oscillator) used as back up to the PRTC and the End Application continues to be locked to the PTP reference.

As an example, it could be assumed that failure scenario a) can be handled within TE_{REA} = 250 ns (in the case where the rearrangement is handed within 60 s).

Depending on a specific deployment, only failure scenario a) or b) might be of interest.

The following table presents an example related to failure scenario a) (note: the terms building the network limit of 1100 ns are indicated by a shaded area in the table), an example of failure condition b where the network limit of 1100 ns at point C would be exceeded (this is for further study) and an example of a long-time synchronization holdover that would lead to exceeding the target requirement TE_D at reference point D.

Table V.1 – Example of Time Error allocation

Budget Component	**Failure scenario a)**	**Failure scenario b)**	**Long Holdover periods (e.g. 1 day)**
PRTC (ce_{ref})	100 ns	100 ns	100 ns
Holdover and Rearrangements in the network (TE_{HO})	**NA**	**400 ns**	**2400 ns**
Random and error due to synchronous Ethernet rearrangements (dTE')	200 ns	200 ns	200 ns
Node Constant including intrasite (ce_{ptp_clock})	550 ns (Note 1)	550 ns (Note 1)	550 ns (Note 1)
	420 ns (Note 2)	420 ns (Note 2)	420 ns (Note 2)
Link Asymmetries (ce_{link_asym}) (Note 3)	250 ns	100 ns	100 ns
	380 ns	230 ns	230 ns
Rearrangements and short Holdover in the End Application (TE_{REA})	250 ns	**NA**	NA
End application (TE_{EA})	150 ns	150 ns	**150 ns**
Total (TE_D)	**1500 ns**	**1500 ns**	**3500 ns (Note 4)**

Note 1: it is assumed in these examples that the T-GM and all T-BCs contribute constant TE of 50 ns as per type A T-BC (see G.8273.2).
In Deployment case 1 the HRM is composed of: 10 T-BCs, 1 T-GM and 11 links,.
In Deployment case 2 the HRM is composed of: 1 T-GM, 1 T-TSC, 9 T-BCs, 1 intra-site link, and 10 links. The time error budget allocated to the time synchronization distribution in the intra-site connection between the Packet Clock and the End Application in the worst case is 50 ns. In order to get the same constant Time Error limit as per Deployment

case 1, it should be assumed that, for example, the T-GM, the T-TSC, and the intra-site connection contribute with 100 ns in total.

Note 2: it is assumed in these examples that the T-GM and all T-BCs contribute constant TE of 20 ns as per type B T-BC clock (see G.8273.2).
In Deployment case 1 the HRM is composed of: 20 T-BCs, 1 T-GM and 21 links,.
In Deployment case 2 the HRM is composed of: 1 T-GM, 1 T-TSC, 19 T-BCs, 1 intra-site link, and 20 links. The time error budget allocated to the time synchronization distribution in the intra-site connection between the Packet Clock and the End Application in the worst case is 20 ns. In order to get the same constant Time Error limit as per Deployment case 1, it should be assumed that, for example, the T-GM, the T-TSC, and the intra-site connection contribute with 40 ns in total.

Note 3: in order to simplify the comparison between Deployment cases 1 and 2, the same number of links should be assumed in both deployment cases. In order to do that, the additional link of the Deployment case 1 model, could be combined with the T-GM budget.

Note 4: exceeding the TE_D limit of 1500 ns is related to the operator requirements in terms of service degradation.

5 Appendix VI , Mitigation of time error due to synchronous Ethernet transients

Replace Appendix VI by the following:

Appendix VI

Mitigation of time error due to synchronous Ethernet transients

(This appendix does not form an integral part of this Recommendation)

Appendix II, subclause II.1.2 illustrates hypothetical reference models for the transport of phase/time via PTP with physical layer frequency support. Figure II.2 illustrates the congruent scenario, where the frequency and phase/time transports follow the same synchronization path. Figure III.3 illustrates the non-congruent scenario, where the frequency and phase/time transports follow different synchronization paths. A rearrangement of the physical layer frequency, e.g., Synchronous Ethernet, transport results in phase/time error at each T-BC, the T-TSC, and the end application. The time error is generally larger in the congruent scenario than in the non-congruent scenario, because in the congruent scenario each T-BC has errors due to the rearrangement transient in both the time and frequency planes. The latter occurs in the physical layer frequency input to a T-BC, and the former occurs in PTP Sync messages input to a T-BC from the upstream T-BC. In the non-congruent scenario, a T-BC has an error due only to the physical layer frequency input (assuming that only one synchronous Ethernet reference chain at a time undergoes a rearrangement).

Details on requirements and solutions to address this issue are provided in G.8273.2.

Note: in the case where in the congruent scenario the T-BC does not comply with G.8273.2 Annex B, the time error due to the synchronous Ethernet rearrangement can be reduced to an acceptable level by using an end application clock with sufficiently narrow bandwidth and sufficiently small gain peaking, and by collocating a suitable clock with the end application in the frequency plane. For the hypothetical reference model of Appendix II, a maximum end application clock bandwidth of 5 mHz, with a maximum gain peaking of 0.1 dB, will reduce the time error due to the synchronous Ethernet rearrangement to an acceptable level. The analysis was done assuming a G.812 Type I clock is collocated with the end application clock in the frequency plane; however, a different type of clock might still result in acceptable time error. This has not been verified.

In the non-congruent scenario, the time error will be acceptable if the T-BCs, T-TSC, and end application have minimum bandwidth of 0.05 Hz, maximum bandwidth of 0.1 Hz and maximum gain peaking of 0.1 dB, and if the frequency plane clocks collocated with the T-BCs, T-TSC, and end application are EECs. This is true whether or not the synchronous Ethernet transient is rejected at each T-BC.

Note: the case of a network where SSM is not used is for further study.