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Title: **TDD synchronisation**

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Introduction

The optimised TDD operation requires two levels of synchronisation, i.e. Frame Synchronisation and Multi frame synchronisation.
In order to achieve synchronisation different solutions are possible.
The main possibilities are:

- Synchronisation of nodes B to an external reference via a standardised synchronisation port;
- Synchronisation of nodes B via the air interface e.g. through nodes B cross measurements or assisted by UEs.

All these solutions have some advantages and some drawbacks, and it can be foreseen that a combined solution will be adopted as final mechanism.
For R99 however it is proposed to base TDD synchronisation on the usage of a standardised Node B synchronisation port, that allows the node B to be synchronised to an external reference.
The aim of this paper is therefore to describe the different synchronisation aspects and to define the standardised synchronisation port.

1. TDD Synchronisation Issues

The optimised TDD operation requires two levels of synchronisation:

- Frame Synchronisation;
- Multi frame synchronisation.

Both these issues are described in the following subsections.

1.2. Frame Synchronisation

This kind of synchronisation is necessary to ensure that the uplink/downlink switching points be positioned at the same time instant at least in adjacent cells (see Figure 1).
This requirement is necessary to avoid that a receiving UE can be saturated by a transmitting UE in a neighbouring cell.
In addition it automatically ensures that the slots of different cells are synchronised, i.e. they do not overlap at the UE.

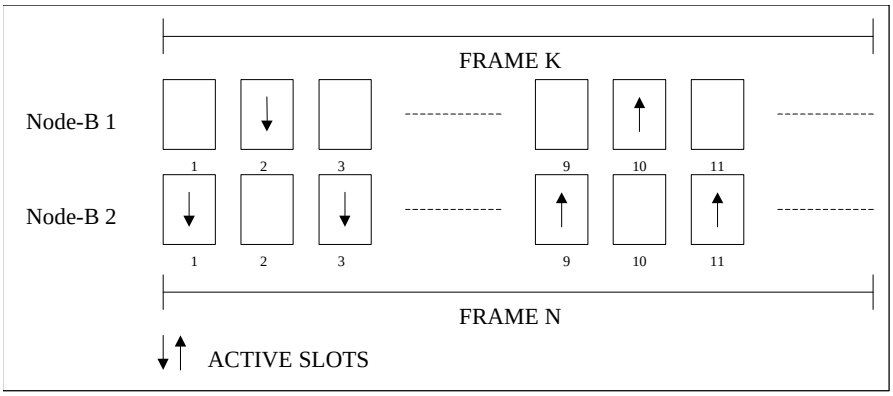

Figure 1: Frame synchronisation

1.3. Multi Frame Synchronisation

This kind of synchronisation may be required to keep more efficient and faster all procedures involving a switch from one Node-B to another, such as searching for new Base Stations, locking to new Base Stations or handover.
Note that a prerequisite for Multi Frame Synchronisation is that frames are synchronised.
For Multi Frame Synchronisation it is required that the frame numbers in neighbouring cells are time aligned, i. e. in Figure 1 this would mean N=K.

2. Node B Synchronisation Ports

This section defines the Node B input and an output synchronisation ports.
The input synchronisation port (SYNC IN) allows the node B to be synchronised to an external reference (e.g. GPS), while the output synchronisation port (SYNC OUT) allows the node B to synchronise directly another node B.
The node B starts the synchronisation to the external reference when a valid input synchronisation signal is detected at the input synchronisation port.
If a valid synchronisation signal is detected, the node B regenerates that signal at its output synchronisation port. The propagation delay between the input and output synchronisation ports shall not exceed [FFS] ns.
The electrical characteristics of the synchronisation ports shall conform to RS422 [1] (output synchronisation port: section 4.1; input synchronisation port: section 4.1).
The synchronisation signal (illustrated in figure 2) is a 100 Hz signal having positive pulses of width between 5 μs and 1 ms, except for frame 0 (every 72nd pulse), which has a pulse width between 2 ms and 5 ms. This signal establishes the 10 ms frame interval and the 720 ms multiframe interval.
The start of the multiframe is defined by the falling edge of the pulse corresponding to frame 0 (i.e. of width between 2 ms and 5 ms).
The synchronisation signal at the input port shall have a frequency accuracy better than the one of the node B.
The relative phase difference of the synchronisation signals at the input port of two neighbouring nodes B shall not exceed [FFS] μs.

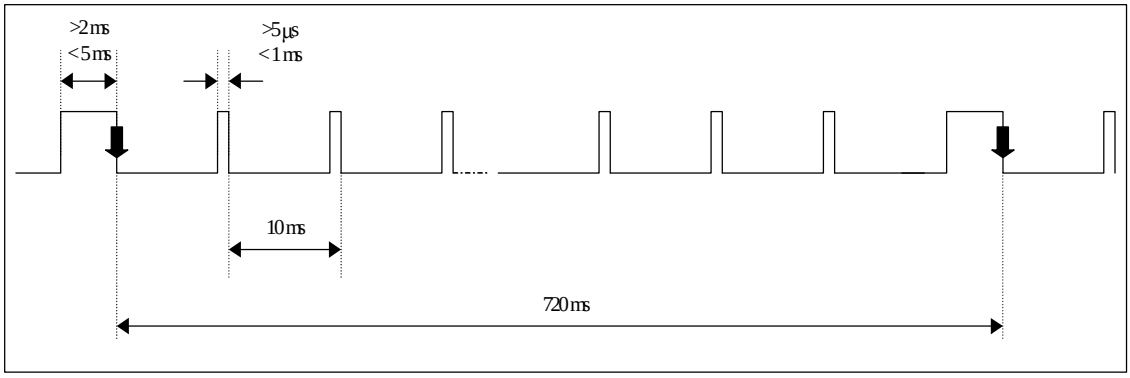

Figure 2: Synchronisation signal

Proposal

We propose to include sections 1and 2 of this contribution in section 9.7 of TS 25.401.

References

[1] EIA 422-A-78 “Electrical characteristics of balanced voltage digital interface circuits”.