**3GPP TSG RAN WG1 Meeting #106bis-e R1-21xxxxx**

**e-Meeting, October 11th – 19th, 2021**

**Source: Moderator (vivo)**

**Title: Discussion summary #1 of [106bis-e-NR-52-71GHz-05]**

**Agenda item: 8.2.5**

**Document for:** [Status]

# Introduction

In this contribution, we summarize issues regarding PDSCH/PUSCH enhancements for new SCSs on supporting NR from 52.6 GHz to 71 GHz for the following email discussion in RAN1 #106bis-e.

[106bis-e-NR-52-71GHz-05] Email discussion/approval on defining maximum bandwidth for new SCSs, timeline related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals with checkpoints for agreements on October 14 and 19 – Huaming (Vivo)

Note that the scope of agenda 8.2.5 including defining maximum bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz, reference signals, scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ, etc. In this summary, only issues related to bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals are summarized. Issues related to scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ are not in the scope of this summary.

# PDSCH/PUSCH enhancements for new SCSs

In this section, we provide a summary of issues, observations and proposals related to PDSCH/PUSCH enhancements for new SCSs discussed in the submitted contributions.

As in WID, the related objectives for this summary of agenda 8.2.5 are the following.

* Physical layer aspects including [RAN1]:
  + In addition to 120kHz SCS, specify new SCS, 480kHz and 960kHz, and define maximum bandwidth(s), for operation in this frequency range for data and control channels and reference signals, only NCP supported.

Note: Except for timing line related aspects, a common design framework shall be adopted for 480kHz to 960kHz

* + Time line related aspects adapted to 480kHz and 960kHz, e.g., BWP and beam switching timing, HARQ timing, UE processing, preparation and computation timelines for PDSCH, PUSCH/SRS and CSI, respectively.
  + Evaluate, and if needed, specify the PTRS enhancement for 120kHz SCS, 480kHz SCS and/or 960kHz SCS, as well as DMRS enhancement for 480kHz SCS and/or 960kHz SCS.

## 2.1. Timeline

### Individual observations/proposals

The following are individual observations and proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | Proposal 1: The absolute time of 120 kHz SCS timelines should be adopted by default unless the reduced value for specific timeline(s) can be verified by implementation.  Proposal 2: For single slot/multi-slot scheduling with 480 kHz and 960 kHz SCS, N1, N2 and N3 values providing same absolute processing time as that of 120 kHz SCS in FR2 are the only values supported in Rel-17. RAN1 should stop discussing smaller values of N1, N2 and N3.  Proposal 3: The value range of k0 and k2 should be extended to 0~128 and 0~256 for 480 kHz and 960 kHz SCS respectively.  Proposal 4: The value range of k1 should be defined for DCI format 1\_0, 1\_1 and 1\_2 separately:  For DCI format 1\_0: define a new set with scaled values for 480 kHz and 960 kHz respectively;   * {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz * {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz   For DCI format 1\_1: define -1~63 and -1~127 as the value range of k1 for 480 kHz and 960 kHz;  For DCI format 1\_2: define 0~63 and 0~127 as the value range of k1 for 480 kHz and 960 kHz.  Proposal 5: For single slot/multi-slot scheduling with 480 kHz and 960 kHz SCS, values of Z1, Z2 and Z3 agreed at RAN1#106e are the only values supported in Rel-17. RAN1 should stop discussing smaller values of Z1, Z2 and Z3. |
| [2, Futurewei] | Observation 1. Specifying a set of smaller timeline values is not a practical target to complete in one meeting, given the relevant open discussions in parallel and the dependency of required factors to consider on other timeline values that have not been opened for discussion for 480/960kHz SCS.  Proposal 1. If RAN1 decides that an alternative timeline besides the adopted upper bounds is necessary, one way to move forward is to adopt the potential lower bounds as an optional UE capability.  Proposal 2. For multi-PxSCH, to be compatible with the enhanced TDRA table, the offsets K0/K1/K2 can be defined relative to each PxSCH of a multi-PxSCH.  Proposal 3. To achieve better flexibility, it is recommended that the unit is number of slot for K0/K1/K2 when multiple-PxSCH is scheduled for all SCSs.  Observation 2. It is needed to restrict the maximal allowable gap values between adjacent PxSCHs according to the practical needs to avoid excessively large gaps that negatively impact the latency/throughput of the system or triggers additional requirement for LBT.  Proposal 4. Discuss and decide the maximal gaps first and then extensions for K0/K1/K2 based on introducing SCS-dependent slot offsets. |
| [4, ZTE] | Proposal 6: For NR FR2-2, extend the value range of K1 from (0..15) to (0..31).  Proposal 7: For NR FR2-2, at least for 480/960 kHz SCS, increasing the PDSCH-to-HARQ\_feedback timing indicator field to 4 or 5 bits should be supported.  Proposal 8: Adopt the already agreed values of N1, N2 and N3 for single and multi-PDSCH/PUSCH scheduling if there is no consensus on smaller values. |
| [5, vivo] | Proposal 6: Among parameters d1,1, d2, Text, d2,1, Tswitch, d2,2, only parameter d2,2 for 480/960 kHz SCS should use the absolute time duration for 120 kHz SCS as the upper bound for FR2-2 in Rel-17.  Proposal 7: For FR2-2, the range of k0 for 480/960 kHz SCS can be kept as 0~32.  Proposal 8: For FR2-2, the range of k1 for 480/960 kHz SCS should be defined as offset ~ offset+15, where the offset is dependent on SCS, for example, offset = 6/12 for 480/960 kHz SCS respectively.  Proposal 9: For FR2-2, the range of k2 for 480/960 kHz SCS should be defined as offset ~ offset+32, where the offset is dependent on SCS, for example, offset = 11/21 for 480/960 kHz SCS respectively. |
| [10, CATT] | Proposal 1: Compared with the processing time of 120 KHz SCS, considering the maximum system bandwidth and maximum PRB number can be scheduled, N1/N2 of capability 2 is proposed as follows:   * For SCS=480 KHz, the N1/N2 can be 1.5 times as 120 KHz N1/N2 value. * For SCS=960 KHz, the N1/N2 can be 1.25 times as 480 KHz N1/N2 value.   Proposal 2: The range of k1 value specified for PDSCH HARQ process operation for 480 KHz/960 KHz SCS should take the N1 processing time into account with the starting slot from the value.  Proposal 3: The range of k2 value specified for PUSCH process for 480 KHz/960 KHz SCS should take the N2 processing time into account with the starting slot from the value. |
| [12, Ericsson] | Proposal 16 Increase the maximum value for K0 to 64 slots at least for SCS 480 and 960 kHz to support multi-PDSCH scheduling.  Proposal 17 Increase the maximum value for K1 to 128 slots at least for SCS 480 and 960 kHz to support multi-PDSCH scheduling for non-fallback DCI.  Proposal 18 For PDSCH scheduled by fallback DCI, the K1 value in number of slots is directly indicated by the PDSCH-to-HARQ\_feedback timing indicator field value, scaled by 4 and 8 for 480 and 960 kHz SCS respectively.  Proposal 19 Increase the maximum value for K2 to 128 slots at least for SCS 480 and 960 kHz to support multi-PUSCH scheduling.  Observation 7 UE PDSCH/PUSCH processing timelines for 480/960 kHz SCS should to be tightened compared to 4x / 8x scaling of the 120 kHz SCS values to enable high performance NR operation in 52.6 to 71 GHz.  Proposal 26 RAN1 should discuss tightening of the N1/N2/N3 processing timelines. A starting point for discussion can be ½ of the values listed in the RAN1#106-e agreement.  Proposal 27 RAN1 should discuss tightening of the Z1/Z1'/Z2/Z2'/Z3/Z3' CSI computation delay requirements. A starting point for discussion can be ½ of the values listed in the RAN1#106-e agreement. |
| [13, Nokia] | Observation 1: The processing times agreed in RAN1 #106 result in too tight processing times for gNB   * Increasing the PDCCH monitoring periodicity can alleviate the problem to some extend   Proposal 11: For NR operation with 480 and 960 kHz SCS, introduce 30% smaller values of N1, N2 and N3 for single and multi-PDSCH/PUSCH scheduling for = [5, 6] (compared to values agreed in RAN1 #106e).  Proposal 12: No additional CSI computation delay is supported in addition to the value agreed in RAN1 106e.  Observation 2: Rel-15/16 schemes for CPU can be reused for 480kHz and/or 960kHz SCS. |
| [15, Samsung] | Proposal 1: Focus on the agreed processing timeline for Rel-17.  Proposal 2: Support SCS-specific K1/K2 by reusing existing default/configured K1/K2 plus a SCS specific offset. |
| [16, MediaTek] | Proposal 12: For determining the processing timelines for 480kHz and 960kHz, the following parameters are scaled by 4 and 8 for 480kHz and 960kHz, respectively.   * (in PDSCH processing time) * (in PUSCH preparation time)   Proposal 13: The necessity of advanced processing timelines for 480kHz and 960kHz should be justified and the methodology for evaluation should be discussed together if the advanced processing timelines are needed. |
| [17, Intel] | **Proposal 1:**   * Support the following advanced N1, N2, and N3 processing times as optional capability.   + N1 = N3 = [36], N2 = [90] for 480 kHz   + N1 = N3 = [49], N2 = [144] for 960 kHz * Support the following advance Z1,Z2,and Z1 processing times for CSI as optional capability  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  | ***Z1* [symbols]** | | ***Z2* [symbols]** | | ***Z3* [symbols]** | | | *Z1* | *Z'1* | *Z2* | *Z'2* | *Z3* | *Z'3* | | 5 | [194] | [170] | [304] | [280] | [min([194], *X*5+ KB3)] | [*X*5] | | 6 | [388] | [340] | [608] | [560] | [min([388], *X*6+ KB4)] | [*X*6] | |
| [20, Lenovo] | Proposal 9: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, following enhancements should be supported to efficiently utilize UE’s limited processing capability to reduce latency and efficiently handle processing/preparation of CSI reports associated with multiple numerologies in parallel:   * Same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values |
| [22, LG] | Proposal #25: Consider additional UE PDSCH processing procedure time (i.e., N1 symbols) when UE is required to perform both of CPE and ICI compensation, e.g., for 120 kHz SCS and 64 QAM.  Proposal #26: Consider scaling values for the extra symbols (e.g. *d1,1* and *d2* to derive *Tproc,1*) which are added to N1 when the PDSCH processing procedure time is calculated.  Proposal #27: Consider scaling values for the extra symbols (e.g. *d2,1* and *d2* to derive *Tproc,2*) which are added to N2 when the PUSCH preparation procedure time is calculated.  Proposal #28: The configured and default value of k1 (or PDSCH-to-HARQ\_feedback), should be adjusted to practical value considering the increased N1, e.g., ceil(N1/14) or floor(N1/14).  Proposal #29: The configured and default value of k2 should be adjusted to practical value considering the increased N2, e.g., ceil(N2/14) or floor(N2/14).  Proposal #30: The configured value of k0 should be adjusted to practical value considering the UE PDSCH reception preparation time with cross carrier scheduling with different numerologies for PDCCH and PDSCH.  Proposal #31: Consider the dependence of each other when determining the value range of k0 and k1.  Proposal #32: Clarify that requirement 2 is applied when an aperiodic CSI report is triggered without PUSCH multiplexing and all CPUs are unoccupied at UE, for which requirement 1 was applied in Rel-15.  Proposal #33: Consider the mixed SCS configuration for the aperiodic CSI reporting in applying CSI computation delay requirement for 480 kHz and 960 kHz.  Proposal #34: Consider CSI processing timeline enhancements for better availability for CPUs for multiple CSI reports associated with different numerologies. |
| [23, Apple] | Proposal 1: RAN1 to finalize the UE processing timeline values for N1, N2, N3, Z1, Z2 and Z3 as agreed on in RAN1 #106-e.  Proposal 2: For NR operation with 480 and 960 kHz SCS, adopt at least the values of for all UE processing times for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.  Proposal 3: For 489 kHz/960 kHz SCS, the UE should support cross-slot scheduling only at least in RRC connected state with Kmin\_values specified for K2.   * a minimum offset in unit of slots can be added to the configured/signaled timing with the value different for different SCS. * The minimum offset can be either pre-defined in the specifications or configured via higher layer signaling   Proposal 4: The values of k1 and k2 should be modified to accommodate the increased values of N1 and N2)   * For K2, increase slot offset per subcarrier in ‘Default’ lookup table to accommodate larger SCSs.   + For Type 1 configured grants increase the value of the timeDomainOffset * For K2, modify the RRC configuration parameter to allow for more than 32 (current maximum value is 32). * For K1, modify the RRC configuration parameter to allow a slot offset of more than 15 slot candidates (current maximum value is 15). * Set a minimum slot offset based on SCS with Min\_offset = (K1min, K2min) e.g. for 960 kHz, K2min ≥288 symbols (21 slots)=>K2min) = 21 slots.   + The value of Min\_offset is configured in the puschTimeDomainAllocationList with pusch-ConfigCommon or puschConfig. The actual slot offset is then given by   Slot offset = Min\_offset + DCI signaled slot offset   * + Note that the DCI field size may also be modified to signal more slot offset values from the increased set.   Proposal 5: The slot configuration period and the existing FR2 TD UL/DL configuration using either 60 kHz or 120 kHz is reused for 480kHz/960kHz SCS and the number of configuration slots is scaled accordingly. |
| [25, Qualcomm] | Proposal 21: Do not introduce smaller values for N1/N2/N3 and Z1/Z2/Z3.  Proposal 22: Shift the range of K1, RRC configured and the default ones before RRC configuration, by floor(N1/14) for SCS 480kHz and 960kHz and choose the j values for PUSCH default TDRA tables as ceil(N2/14). |

### Summary on timeline

#### N1, N2 and N3

The following were agreed in RAN1#106-e.

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, value(s) for PDSCH processing time (N1) for PDSCH processing capability 1 and PUSCH preparation time (N2) are to be defined for PDSCH/PUSCH timing capability 1 only.

Agreement:

For NR operation with 480 and 960 kHz SCS, adopt at least the values of N1, N2 and N3 as in the following tables for single and multi-PDSCH/PUSCH scheduling.

* Note: N1/N2 applies to any PDSCH/PUSCH for multi-PDSCH/PUSCH scheduling
* RAN1 to study (until RAN1#106b-e) and possibly introduce smaller values considering at least the following factors
  + PDCCH monitoring capability
  + Mix numerology scheduling
  + Multi-PDSCH/PUSCH scheduling
  + Cross-carrier scheduling
* Note: The decision for the number of HARQ processes should take this agreement into account.

Table 2-2.1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 3 (120 kHz) | 20 | 24 |
| 5 (480 kHz) | 80 | 96 |
| 6 (960 kHz) | 160 | 192 |

Table 2-2.2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 3 (120 kHz) | 36 |
| 5 (480 kHz) | 144 |
| 6 (960 kHz) | 288 |

Table 2-2.3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 3 (120 kHz) | 20 |
| 5 (480 kHz) | 80 |
| 6 (960 kHz) | 160 |

Regarding the remaining issue whether to introduce smaller values for N1/N2/N3, the following contribution expressed their views.

[1, Huawei] proposed that for single slot/multi-slot scheduling with 480 kHz and 960 kHz SCS, N1, N2 and N3 values providing same absolute processing time as that of 120 kHz SCS in FR2 are the only values supported in Rel-17. RAN1 should stop discussing smaller values of N1, N2 and N3. Similarly, [2, Futurewei], [15, Samsung], [16, MediaTek], [23, Apple] and [25, Qualcomm], all thought further timeline reduction should be justified and proposed to focus on the agreed values in Rel-17.

Stated opposing reasons and/or concerns on the introduction of smaller values are:

* Additional complexity/delay caused by algorithms (e.g., ICI compensation)
* On-going discussion on other aspects (mix numerology scheduling, multi-PDSCH/PUSCH scheduling, and cross-carrier scheduling) which may have adverse impact on timeline
* No clear justification on necessity and/or feasibility
* Limited time to complete this Rel-17 WI

On the other hand, [10, CATT], [12, Ericsson], [13, Nokia] and [17, Intel] proposed to introduce smaller/tighter timeline values to enable high performance (low latency) NR operation in 52.6 to 71 GHz. [10, CATT] provided their values of N1 and N2 based on an analysis on the impact of channel bandwidth, the number of PRB and LDPC coding to UE processing timeline, where for SCS=480 KHz, the N1/N2 can be 1.5 times as 120 KHz N1/N2 value and for SCS=960 KHz, the N1/N2 can be 1.25 times as 480 KHz N1/N2 value. [12, Ericsson] observed that the amount of processing time provisioned for decoding a PDSCH/PUSCH grows exponentially with the numerology and took an exponential function a∙2^(b∙μ) fitted to the Rel-15 values that provides extrapolated values of N1, N2, and N3 for 480 and 960 kHz (correspond to roughly half of those agreed values) as starting point for discussion. [13, Nokia] analysed a multi-PDSCH/PUSCH scheduling case and observed that the agreed UE timeline values result in too tight processing time for gNB (note increasing the PDCCH monitoring periodicity can alleviate the problem to some extend) and proposed 30% reduction for N1, N2 and N3 with respect to the agreed values. [17, Intel] provided their values based on the projection for processing capability which can be achieved by future implementation and/or advance UE.

The proposed smaller values of N1, N2 and N3 from companies are summarized in the following tables.

Table 1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 5 (480 kHz) | 30 ([10, CATT])  40 ([12, Ericsson])  56 ([13, Nokia])  36 ([17, Intel]) | 36 ([10, CATT])  48 ([12, Ericsson])  67 ([13, Nokia])  36 ([17, Intel]) |
| 6 (960 kHz) | 42 ([10, CATT])  80 ([12, Ericsson])  112 ([13, Nokia])  49 ([17, Intel]) | 50 ([10, CATT])  96 ([12, Ericsson])  134 ([13, Nokia])  49 ([17, Intel]) |

Table 2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 5 (480 kHz) | 60 ([10, CATT])  72 ([12, Ericsson])  100 ([13, Nokia])  90 ([17, Intel]) |
| 6 (960 kHz) | 72 ([10, CATT])  144 ([12, Ericsson])  200 ([13, Nokia])  144 ([17, Intel]) |

Table 3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 5 (480 kHz) | 40 ([12, Ericsson])  56 ([13, Nokia])  36 ([17, Intel]) |
| 6 (960 kHz) | 80 ([12, Ericsson])  112 ([13, Nokia])  49 ([17, Intel]) |

Companies’ views on whether to introduce additional smaller values of N1/N2/N3 in Rel-17.

Yes: [10, CATT], [12, Ericsson], [13, Nokia], [17, Intel]

No: [1, Huawei], [15, Samsung], [16, MediaTek], [23, Apple], [25, Qualcomm]

If necessary, as optional UE capability: [2, Futurewei]

Moderator’s comment:

Companies’ views are split on this issue. Four companies support (but with different values for each of the timeline) and five companies oppose introducing smaller values. One company suggested if RAN1 think this is necessary, consider it as optional UE capability.

Considering the limited remaining time of this WI, we need to finalize the design and make the decision on whether to introduce smaller values in this meeting as we agreed. Formulate the following proposal with two alternatives: conclude not to support other values for N1/N2/N3 in Rel-17 and close this discussion point; or see if tightened timeline (note that the proposed smaller values in [12] are taken as they are roughly average/median among proponents) as optional UE capability can resolve the concerns from opposing companies and move forward.

##### Proposal 1-1 (high priority)

Alt1 (as conclusion):

In Rel-17, for NR operation with 480 and/or 960 kHz SCS, no other values of N1, N2 and N3 is supported.

Alt2:

For NR operation with 480 and 960 kHz SCS, adopt the values of N1, N2 and N3 (in addition to previous agreed values) as in the following tables for single and multi-PDSCH/PUSCH scheduling as optional UE capability.

* Note: N1/N2 applies to any PDSCH/PUSCH for multi-PDSCH/PUSCH scheduling

Table 1-1.1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 5 (480 kHz) | 40 | 48 |
| 6 (960 kHz) | 80 | 96 |

Table 1-1.2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 5 (480 kHz) | 72 |
| 6 (960 kHz) | 144 |

Table 1-1.3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 5 (480 kHz) | 40 |
| 6 (960 kHz) | 80 |

Companies are encouraged to provide comments and/or to indicate preference/objection (if any).

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Ideally speaking, we would be open to discussing new values for N1, N2 and N3.  However, considering the limited time and divergence on the values from proponent companied, we would **prefer to support Alt 1** i.e. no further consideration of additional values. |
| Qualcomm | We support Alt 1 |
| Intel | Supportive of Alt 2.  We would like to point out that it is unlikely that 60 GHz enhancements WI will be approved for release-18. Therefore, its it now even more important for release 17 to have some provisions for future implementation developments. Having an additional optional capability should ease companies who have concern on supporting somewhat aggressive numbers while allowing the specification to be more future proof.  We would like to ask proponents of Alt 1, what would be the concern for additional optional capability? |
| vivo | The concerns for additional optional capability include it takes time to:   1. Converge from diverse options; 2. Prove the converged values are feasible.   If these concerns can’t be resolved, Alt 1 will be the only option. |
| LG Electronics | We support Intel’s view and prefer Alt 2.  If additional values do not replace the mandatory value that has already been agreed upon, it would be better to introduce aggressive values as an optional UE capability to effectively support advanced UEs in the future. Unless other values have a special reason, it seems appropriate to set them to half of the mandatory values. |
| Nokia/NSB | Share view with Intel and LGE. Support Alt 2.  The processing times agreed in RAN1 #106 result in too tight processing times for gNB. This will mean e.g. that processing times start limiting the DL or UL throughput in DL heavy or UL heavy traffic scenarios. At least we need additional values even optional UE capability. |
| Apple | Support Alt 1 |
| CATT | ALT2. The agreed values are the lower-bound capability UE. The network’s scheduling will be affected if only the these are specified. |
| InterDigital | Supporting additional strict values for N1, N2, and N3 under optional UE capability could be helpful to make the specifications futureproof. Therefore, we support Alt 2, however, the exact values could be further discussed. |
| Samsung | We support Alt 1.  Regarding Intel’s suggestion on additional optional capability, is the intention to define PDSCH/PUSCH processing capability 2? If yes, our understanding is the PDSCH/PUSCH processing capability 2 does not defined for 480/960kHz SCS in FR2-2. If no, what is difference between processing capability 2 and additional optional capability? |
| Futurewei | We prefer Alt 1. For additional capability, we see the difficulty to converge to a feasible set of values. |
| ZTE, Sanechips | We support Alt-1. |
| Ericsson | We share a similar view with Nokia that DL/UL throughput can be limited with loose processing timelines. Hence we support Alt-2 from a future proof perspective. As previously agreed, the 2nd set of values would use the same frame as PDSCH/PUSCH timing capability 1, but would be optional. |
| Intel | To respond to Samsung question.  So the our proposal is not to define processing capability 2. Processing capability 1 and 2 in FR1 not only defer how timelines are defined but also in how MCS and TBS limitations are applied.  While FR1 capability 2 was mainly targeting for improved processing for URLLC, the small subcarrier spacing in FR2-2 does not necessarily need to differentiate advanced processing UEs in this manner.  So our proposal is to define optional values for processing capability 1. In effect, the specification would be completely identical and the only thing that would change for this optional UE capability is lower processing values. In essence, there would be two set of processing capability 1 (one basic, and one more advanced).  As for convergence and burden of proof that values are feasible. Several companies provide some input on the potential values. I don’t think companies have provided random number out of thin air, but provide with estimates based on each company’s understanding of currently available technology and to be available technology in the future.  For the values that we have suggested, we have some confidence that these values can be achieved. Please note that mobile devices are not the only form factor for deployment of interest. We believe for 60 GHz fixed wireless will be an important deployment scenario. For these scenarios, UE hardware implementation may not need to be power constrained.  As mentioned, it is unlikely rel-18 will have enhancements for 60GHz. Release 17 for 60GHz will need to be used thought release 19+ timeframe. So we would like to understand, why companies think more faster processing capability will not be available (or infeasible) in Rel-19+ timeframe, considering UEs formfactor may not be limited to just small mobile devices? |
| DOCOMO | Prefer Alt 1 considering limited time in Rel-17. But we don’t object Alt 2 for smaller values. |
| Xiaomi | Prefer Alt 1,but if companies can agree on the values for Alt 2, we are also OK with Alt 2. |
| Huawei, HiSilicon | We support Alt1 from the moderator. Even though RAN1 has discussed the possibility of smaller UE processing times for a few meetings, it is still not clear whether and by how much the UE processing times could actually be reduced even as an optional capability.  A small reduction would mean that two UE capabilities are very close to each other, so the faster processing capability may not really bring substantial benefit from UE implementation, i.e. it is unclear why a UE would implement the slightly faster timeline if the only benefit is to alleviate the gNB processing burden as pointed out by Nokia.  On the other hand, keeping only the reduced processing timeline (to address gNB processing burden) is also putting burden on the UE side for the additional processing due to e.g. CPE/ICI compensation. |

#### k0, k1 and k2

In RAN1#106-e, the following was agreed.

Agreement:

When defining value ranges and/or default values for k0/k1/k2 for NR operation with 480 and 960 kHz SCS, RAN1 assumes the following definitions (this agreement does not define the following and these definitions may be updated later)

* The value of k0 indicates the slot offset between DCI and its scheduled PDSCH in number of slots
* The value of k1 indicates the slot offset between the slot of the last PDSCH scheduled by the DCI and the slot carrying the HARQ-ACK information corresponding to the scheduled PDSCHs in number of slots
* The value of k2 indicates the slot offset between DCI and its scheduled PUSCH in number of slots
* Note: Default values are indicated by DCI format 1\_0 and 0\_0

On the ranges and default value for k0/k1/k2, multiple contributions expressed their views.

[1, Huawei] proposed value range of k0 and k2 considering scaled TDD configuration and non-continuous resource mapping in time domain. [1, Huawei] also proposed values of k1 for DCI format 1\_0, 1\_1 and 1\_2 separately. [4, ZTE] proposed to increase the value range of k1 and also increase the bit width of PDSCH-to-HARQ\_feedback timing indicator field. [12, Ericsson] proposed to increase the maximum value for k0, k1 and k2. [23, Apple] proposed that the values of k1 and k2 should be modified to accommodate the increased values of N1 and N2.

[5, vivo] thought the value range of k0 should not be changed for 480 kHz and 960 kHz SCS. While [22, LG] proposed the configured value of k0 should be adjusted to practical value considering the UE PDSCH reception preparation time with cross carrier scheduling with different numerologies for PDCCH and PDSCH.

[5, vivo] proposed to define an offset (depends on the SCS) for the value of k1 and k2. [10, CATT] proposed the range of k1 (k2) value specified for PDSCH (PUSCH) HARQ process operation for 480 kHz/960 kHz SCS should take the N1 (N2) processing time into account with the starting slot/offset from the value ⌊N1/14⌋ (⌊N2/14⌋). [15, Samsung] also proposed to support SCS-specific K1/K2 by reusing existing default/configured K1/K2 plus a SCS specific offset. Similarly, [22, LG] proposed that the configured and default value of k1 and k2, should be adjusted to practical value considering the increased N1 and N2 respectively, examples are given as ceil(N1/14) or floor(N1/14) for k1 and ceil(N2/14) or floor(N2/14) for k2. [25, Qualcomm] proposed to shift the range of K1, RRC configured and the default ones before RRC configuration, by floor(N1/14) for SCS 480kHz and 960kHz and choose the j values for PUSCH default TDRA tables as ceil(N2/14).

Proposed value ranges of k0, k1 and k2 are summarized in the following table.

Table 4 k0, k1 and k2 values

|  |  |  |
| --- | --- | --- |
| **Notation** | **Range** |  |
| k0 | * Option 1 ([1, Huawei]): 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz * Option 2 ([5, vivo]): 0 ~ 32 * Option 3 ([12, Ericsson]): 0 ~ 64 |  |
| k1 | * Option 1 ([1, Huawei]):   for DCI format 1\_1: -1~63 for 480 kHz and -1~127 for 960 kHz  for DCI format 1\_2: 0~63 for 480 kHz and 0~127 for 960 kHz   * Option 2 ([4, ZTE]): 0 ~ 31 * Option 3 ([5, vivo], [10, CATT], [15, Samsung], [22, LG], [25, Qualcomm]): existing range + offset where offset is ceil(N1/14) or floor(N1/14). * Option 4 ([12, Ericsson]): 0 ~ 128 | ***Set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0***   * Option 1 ([1, Huawei], [12, Ericsson]):   {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz   * Option 2 ([5, vivo], [10, CATT], [15, Samsung], [22, LG], [25, Qualcomm]): existing set + offset where offset is ceil(N1/14) or floor(N1/14) |
| k2 | * Option 1 ([1, Huawei]): 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz * Option 2 ([5, vivo], [10, CATT], [15, Samsung], [22, LG]): existing range + offset where offset is ceil(N2/14) or floor(N2/14) * Option 3 ([12, Ericsson]): 0 ~ 128 |  |

Moderator’s comment:

For the value range of k0, there’s limited input from contributions. Companies are encouraged to provide their preference.

##### Proposal 1-2-1 (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the value range of k0 in RAN1#106b-e.

* Option 1: 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz
* Option 2: 0 ~ 32 (same as in existing specification)
* Option 3: 0 ~ 64

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We **support the proposal,** and our preference is scaled values corresponding to 480kHz and 960kHz, so we **prefer Option 1** |
| Qualcomm | We are fine with proposal and support Option 3 |
| Intel | Ok with Option 1, but also can accept option 3 as compromise. |
| Vivo | We are fine with either of option 2 and option 3. |
| LG Electronics | Considering the maximum number of PDSCHs that can be scheduled with a single DCI is 8, the current k0 values (i.e. 0~32) may be sufficient for most cases.  However, for the case of the cross-carrier scheduling with different numerologies, an additional gap corresponding to the number of Npdsch PDCCH symbols should be considered to determine the practical k0 value. How to handle this should be further discussed together with the definition of Npdsch for 480/960 kHz SCS. |
| Nokia/NSB | Fine with option 1, but also fine with option 3 for 480kHz. We think at least 0~128 should be supported for 960kHz. |
| Apple | Fine with the proposal and support Alt 1. |
| CATT | Option 2. We think the current value range is sufficient. |
| InterDigital | We are fine with either of Option 2 and 3. |
| Samsung | Fine with proposal. We slightly prefer option 3. |
| Futurewei | Ok with Option 1, but can accept Option 3 for compromise. |
| ZTE, Sanechips | We are ok for option1. |
| Ericsson | We support Option 3  We think the 0 – 32 in current specs (Option 2) is insufficient considering 960 kHz with the large (agreed) value for timeDurationForQCL, maximum number of scheduled PDSCHs, as well as potential slot gaps between the PDSCHs.  Regarding Option 1, we don’t think there is a need to defined SCS specific maximum values. |
| NTT DOCOMO | We prefer option 3.  We understand the motivation of option 1 to keep same absolute time duration for the maximum k0 as that for 120kHz SCS. But the range seems too wide. We think option 3 can be a trade-off between option 1 and option 2. |
| Xiaomi | Ok with Option 1, but also can accept option 3 |
| Huawei, HiSilicon | Option 1: 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz |

Moderator’s comment:

On the value range of k1, formulate the following proposal for discussion.

Proposal 1-2-2 (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the value range for k1 (*dl-DataToUL-ACK, dl-DataToUL-ACK-DCI-1-2*)in RAN1#106b-e.

* Option 1: for DCI format 1\_1: -1~63 for 480 kHz and -1~127 for 960 kHz; for DCI format 1\_2: 0~63 for 480 kHz and 0~127 for 960 kHz
* Option 2: 0 ~ 31
* Option 3: 6 ~ 21 for 480 kHz and 12 ~ 27 for 960 kHz
* Option 4: 0 ~ 128

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We **support the proposal,** and our preference is scaled values corresponding to 480kHz and 960kHz for each DCI formats, so we **prefer Option 1** |
| Qualcomm | We don’t see a need for keeping values less than the PDSCH processing timeline, i.e., no need to start from 0 |
| Intel | Ok with option 1, or 4. |
| vivo | We share the same view as Qualcomm that there is no need to start from 0. Option 3 is preferred by us. |
| LG Electronics | We agree with Qualcomm that there is no need to use a value less than the PDSCH processing time, and we support option 3 in this regard.  However, two methods are possible for Option 3. One is to change the value range on the RRC parameter, and the other is for the UE to interpret by adding an offset while maintaining the currently defined value range for the RRC parameter. We are open in both directions, but prefer the latter, which does not require any changes to the current RRC values. |
| Nokia, NSB | Option 4 is the preferred starting point. It should be noted that PDSCH processing time eats quite some of the range already (N1 is up-to 192 symbols for 960 kHz SCS, ~14 slots). |
| Apple | Fine with the proposal. Support Option 1 with no need to start from zero. |
| CATT | existing range + offset (where offset is ceil(N1/14) or floor(N1/14) ) is the most simple solution. |
| InterDigital | We are fine with Options 1 or 4. |
| Samsung | Fine with proposal. For forward compatibility, we support k1 values starting from 0 (or some values less than N1/14). For example, tighter processing time (e.g., PDSCH processing capability 2) can be supported in future release. |
|  |  |
| Moderator | Added option 3a in proposal 1-2-2a to address LG and CATT’s comment. |
|  |  |

##### Proposal 1-2-2a (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the value range for k1 (*dl-DataToUL-ACK, dl-DataToUL-ACK-DCI-1-2*)in RAN1#106b-e.

* Option 1: for DCI format 1\_1: -1~63 for 480 kHz and -1~127 for 960 kHz; for DCI format 1\_2: 0~63 for 480 kHz and 0~127 for 960 kHz
* Option 2: 0 ~ 31
* Option 3: 6 ~ 21 for 480 kHz and 12 ~ 27 for 960 kHz
* Option 3a: 0 ~ 15 (same as in existing specification).
  + Note: the actual slot offset of k1 is the indicated value + offset where offset is ceil(N1/14)
* Option 4: 0 ~ 128

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Futurewei | Option 1 and Option 4 can also be revised to start from non-zero offsets, which are both fine. |
| ZTE, Sanechips | We are ok for Option 4, and Option 2 is for 120kHz. |
| Ericsson | We support Option 4  We have concerns on Options 2 and 3 – the maximum values are too low considering typical DL/UL switching patterns. For example, consider a TDD DL/UL pattern for 960 kHz with switching times the same as a 4:1 TDD DL/UL pattern for 120 kHz (see diagram below). This means that there are 5 equivalent 120 kHz slots between PUCCH occasions. For 960 kHz, this translates to 5 \* 8 = 40 slots. Considering the PDSCH processing time is ceil(192/14) = 14 slots, K1 should be at least 40 + 14 = 54 slots to account for the scenario shown below where the last scheduled PDSCH is just a bit too late for feedback in the nearest PUCCH occasion and thus needs to be in the next PUCCH occasion. For a more DL heavy TDD pattern, e.g., 9:1, K1 should be 80 + 14 = 94 slots.  Hence we think a values of 128 is safe to cover such typical configurations.    Regarding Option 1, we don't think there is a need for SCS specific maximum values. |
| Intel | As mentioned previously option 1 or 4 are ok. |
| NTT DOCOMO | Option 1/2/4 are acceptable. But no objection to option 3. |
| Xiaomi | Support Option 2/4. We don't think there is a need for SCS specific maximum values. |
| Huawei, HiSilicon | Option 1: for DCI format 1\_1: -1~63 for 480 kHz and -1~127 for 960 kHz; for DCI format 1\_2: 0~63 for 480 kHz and 0~127 for 960 kHz  Regarding option 4, the range should start at -1 for DCI format 1\_1 in unlicensed operation.  Given that 32 is the maximum for 120 kHz SCS, then even if 128 is agreed for both 480 and 960 kHz SCS, it will still be the case that the maximum value depends on SCS. It is not clear why 128 is needed for 480 kHz SCS, so our preference is still option 1 rather than option 4. |
| Apple | Option 1 /4 are okay. Agree with Huawei that Option 4 should be modified to start from -1. |

Moderator’s comment:

On the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0, formulate the following proposal for discussion.

Proposal 1-2-3 (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0in RAN1#106b-e.

* Option 1: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz
* Option 2: {7, 8, 9, 10, 11, 12, 13, 14} for 480 kHz and {13, 14, 15, 16, 17, 18, 19, 20} for 960 kHz

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal and **prefer option 1** |
| Qualcomm | We are fine with the proposal |
| Vivo | We are fine with the proposal |
| LG Electronics | We support Option 2. Values only with integer multiples of 4 or 8 would induce the scheduling constraint.  However, two interpretations are possible for Option 2. One is to change the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0. The other is for the UE to interpret by adding an offset while maintaining the currently defined set of values. We are open in both directions, but prefer the latter, which does not require any changes to the existing values. |
| Nokia, NSB | Support Option 1.  Option 1 can be seen a better starting point for defining the values.  On the other hand, with the agreed PDSCH processing times, the smallest values may be never used. Hence, it might be a better option to replace those values with the one compatible with the agreed processing time values. |
| Apple | Will prefer Option 2 with an offset added. |
| CATT | Option2. Also share the same view with LGE that the offset approach will be better. |
| InterDigital | We are fine with the proposal and we prefer Option 1. |
| Samsung | We slightly prefer option 2. Option 1 change granularity of k1 values from 1 and 2, which results in scheduling restriction. For example, with Option 1, if a TDD structure is 8D:1S:1U with 480kHz, to only 2 D slots used for last PDSCH occasion. |
|  |  |
| Moderator | Added option 2a in proposal 1-2-3a to address LG and CATT’s comment. |

##### Proposal 1-2-3a (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the set of values for PDSCH-to-HARQ\_feedback timing indicator field in DCI format 1\_0in RAN1#106b-e.

* Option 1: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz
* Option 2: {7, 8, 9, 10, 11, 12, 13, 14} for 480 kHz and {13, 14, 15, 16, 17, 18, 19, 20} for 960 kHz
* Option 2a: {1, 2, 3, 4, 5, 6, 7, 8} (same as in existing specification)
  + Note: the actual slot offset of k1 is the indicated value + offset where offset is ceil(N1/14)

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| ZTE, Sanechips | We are OK with Option 1. |
| Ericsson | We support Option 1 due to simplicity – existing DCI 1\_0 can be reused and the indicated value is simply scaled by 4x / 8x for 480/960 kHz.  The maximum values in Option 2 and 2a are too low. For example, see the diagram we included in our comments on the previous proposal for DCI 1\_1. For typical TDD DL/UL patterns with the same switching times as 120 kHz, there is a need to indicate a fairly large number of slots. |
| Intel | Among the options option 1 is preferred. |
| NTT DOCOMO | Slightly prefer option 1 due to wider range of values. |
| Xiaomi | We are OK with Option 1. |
| Huawei, HiSilicon | Option 1: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz |
| Apple | Option 1 may result in scheduling restrictions but larger maximum value. Option 2/2a removes the scheduling restriction but the largest value may not be large enough. One possibility to get the best of both worlds is to to create an option that removes the scheduling restriction with a wider range of values e.g offset + multiplier \* value. |

Moderator’s comment:

On the value range of k2, formulate the following proposal for discussion.

Proposal 1-2-4 (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the value range for k2in RAN1#106b-e.

* Option 1: 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz
* Option 2: 10 ~ 42 for 480 kHz and 20 ~ 52 for 960 kHz
* Option 3: 0 ~ 128

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We **support the proposal,** and our preference is scaled values corresponding to 480kHz and 960kHz, so we **prefer Option 1** |
| Qualcomm | We are fine with the proposal but also there is no need to start from 0 for options 1 and 3 given the agreed timeline |
| Intel | Ok with option 1. |
| vivo | Fine with the proposal. |
| LG Electronics | We agree with Qualcomm that there is no need to start from 0 given the agreed N2 values. Instead of values that are less likely to be used, they should be taken as practical values. In this regard, we support option 2.  However, two methods are possible for Option 2. One is to change the value range on the RRC parameter, and the other is for the UE to interpret by adding an offset while maintaining the currently defined value range for the RRC parameter. We are open in both directions, but prefer the latter, which does not require any changes to the current RRC values. |
| Nokia, NSB | We see Option 3 as the best starting point for defining the values for k2.  Again, it should be noted that PDSCH processing time eats quite some of the range already (N2 is up-to 288 symbols for 960 kHz SCS, ~21 slots). |
| Apple | Prefer Option 1 with no need to start from zero. |
| CATT | Fine with the proposal. Also share the same view with LGE that the offset approach will be better. |
| InterDigital | We are ok with the proposal. We prefer scaling values based on SCS. |
| Samsung | Fine with the proposal and we slightly prefer option 3 as a starting point. |
|  |  |
| Moderator | Added option 2a in proposal 1-2-4a to address LG and CATT’s comment. |

##### Proposal 1-2-4a (high priority)

For NR operation with 480 kHz and/or 960 kHz SCS, select one of the following options as the value range for k2in RAN1#106b-e.

* Option 1: 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz
* Option 2: 10 ~ 42 for 480 kHz and 20 ~ 52 for 960 kHz
* Option 2a: 0 ~ 32 (same as in existing specification).
  + Note: the actual slot offset of k2 is the indicated value + offset where offset is floor(N2/14)
* Option 3: 0 ~ 128

Companies are encouraged to provide comments (including other options) and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Futurewei | Prefer Option 1 with an offset to start from non-zero values; but can accept Option 3 with an offset. |
| ZTE, Sanechips | We are OK with Option 1. |
| Ericsson | We support Option 3.  We don't think there is a need for SCS specific maximum values. |
| Intel | Prefer option 1, can also accept option 3. While some of the smaller values might not be used in practice, not indicating seems to be optimization of the bits. We are not stating optimization is not important, but for this case having some flexibility for the gNB seems to outweigh the benefit of saving 1 or 2 bits in RRC. |
| NTT DOCOMO | Slightly prefer option 3. |
| Xiaomi | Prefer option 3. |
| Huawei, HiSilicon | Option 1: 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz |
| Apple | Option 1 |

#### Z1, Z2 and Z3

The following were agreed in RAN1#106-e.

Agreement:

For NR operation with 480 kHz and/or 960 kHz SCS, only value(s) for CSI computation delay requirement 2 are to be defined.

* FFS: The specific values

Agreement:

For NR operation with 480 and 960 kHz SCS, adopt at least the values of Z1, Z2 and Z3 as in the following table for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.

* Note: is UE reported capability *beamReportTiming*; KB3 and KB4 is UE reported capability *beamSwitchTiming* for 480 and 960 kHz SCS respectively.
* RAN1 to study (until RAN1#106b-e) and possibly introduce smaller values for CSI computation delay requirement

Table 2-4. CSI computation delay requirement 2

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | ***Z1* [symbols]** | | ***Z2* [symbols]** | | ***Z3* [symbols]** | |
| *Z1* | *Z’1* | *Z2* | *Z’2* | *Z3* | *Z’3* |
| 3 | 97 | 85 | 152 | 140 | min(97, *X*3+ KB2) | *X*3 |
| 5 | 388 | 340 | 608 | 560 | [min(388, *X*5+ KB3)] | [*X*5] |
| 6 | 776 | 680 | 1216 | 1120 | [min(776, *X*6+ KB4)] | [*X*6] |

Regarding the remaining issue of whether to introduce tighter CSI delay requirement, the following contributions expressed their views.

[1, Huawei] proposed that for single slot/multi-slot scheduling with 480 kHz and 960 kHz SCS, values of Z1, Z2 and Z3 agreed at RAN1#106e are the only values supported in Rel-17 and RAN1 should stop discussing smaller values of Z1, Z2 and Z3. This view is shared by [15, Samsung], [23, Apple] and [25, Qualcomm] where the stated reasons are similar as for the case of N1/N2/N3. [13, Nokia] also looked at this issue and expected no very critical performance degradation with the agreed CSI computation delay as long as we assume the same number of CSI process (NCPU) for all SCS and hence proposed to not to consider additional CSI computation delay requirement.

On the other hand, [12, Ericsson] proposed that RAN1 should discuss tightening of the Z1/Z1’/Z2/Z2’/Z3/Z3’ CSI computation delay requirements with a starting point for discussion can be ½ of the values listed in the RAN1#106-e agreement. [17, Intel] also thought 2x and 4x scaling compared with 120kHz could be feasible for advanced UEs.

Companies’ views on whether to introduce additional smaller values of Z1/Z2/Z3 in Rel-17.

Yes: [12, Ericsson], [17, Intel]

No: [1, Huawei], [13, Nokia], [15, Samsung], [23, Apple], [25, Qualcomm]

Moderator’s comment:

Companies’ views are split on this issue with majority of companies prefer not to consider additional smaller values for CSI delay requirement.

Compared to the case of N1/N2/N3 timelines, it seems there’s less impact on system performance if no smaller CSI computation delay requirement was introduced. Moderator’s first suggestion is to conclude not to support other values for Z1/Z2/Z3 in Rel-17 and close this discussion point.

In case smaller N1/N2/N3 timeline values were agreed as optional UE capability, it may be better to have tighter CSI computation delay requirement as well. As back up, moderator also formulate an alternative proposal to see if tightened CSI computation delay requirement as optional UE capability can be agreed on the condition of the potential support of smaller N1/N2/N3 timeline values (as in Alt2 of Proposal 1-1 in section 2.1.2.1).

##### Proposal 1-3 (high priority)

Alt1 (as conclusion):

In Rel-17, for NR operation with 480 and/or 960 kHz SCS, no other values of Z1, Z2 and Z3 is supported.

Alt2:

For NR operation with 480 and 960 kHz SCS, if smaller values of N1/N2/N3 as in Proposal 1-1 were agreed in RAN1#106b-e, adopt the values of Z1, Z2 and Z3 (in addition to previous agreed values) as in the following table for single and multi-PDSCH/PUSCH scheduling as option UE capability.

* Note: is UE reported capability *beamReportTiming*; KB3 and KB4 is UE reported capability *beamSwitchTiming* for 480 and 960 kHz SCS respectively.

Table 1-3. CSI computation delay requirement 2

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | ***Z1* [symbols]** | | ***Z2* [symbols]** | | ***Z3* [symbols]** | |
| *Z1* | *Z’1* | *Z2* | *Z’2* | *Z3* | *Z’3* |
| 5 | [194] | [170] | [304] | [280] | [min([194], *X*5+ KB3)] | [*X*5] |
| 6 | [388] | [340] | [608] | [560] | [min([388], *X*6+ KB4)] | [*X*6] |

Companies are encouraged to provide comments and/or to indicate preference/objection (if any) to the above alternatives.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | As commented for other proposal, we would **prefer to support Alt 1** and do not consider any other values for Z1, Z2 and Z3 due to limited remaining time |
| Qualcomm | We support Alt 1 |
| Intel | Support Alt 2.  This is similar for Proposal 1-1 discussion. We would like to point out that it is unlikely that 60 GHz enhancements WI will be approved for release-18. Therefore, its it now even more important for release 17 to have some provisions for future implementation developments. Having an additional optional capability should ease companies who have concern on supporting somewhat aggressive numbers while allowing the specification to be more future proof.  Same question as for Proposal 1-1. We would like to ask proponents of Alt 1, what would be the concern for additional optional capability? |
| vivo | We support Alt. 1 |
| LG Electronics | We support Alt2 for now, but prefer to defer this decision until the N1/N2/N3 decision is concluded.  As Moderator said, it may be better to have tighter CSI computation delay requirement if smaller N1/N2/N3 values are introduced. |
| Nokia, NSB | Support Alt 1. CSI computation is more relevant to channel but processing timeline. |
| Apple | Prefer Alt 1 |
| CATT | Alt2. |
| Samsung | Support Alt 1 |
| Futurewei | We support Alt 1. |
| ZTE, Sanechips | We support Alt 1. |
| Ericsson | Support Alt-2. Okay to decide after N1/N2/N3 timeline discussion is concluded. |
| NTT DOCOMO | Prefer Alt 1 considering limited time in Rel-17. But we don’t object Alt 2 for smaller values. |
| Huawei, HiSilicon | We support Alt1 from the moderator, and removing the [] for some of values of Z3 that still need to be confirmed. |

[22, LG] raised an issue on the interpretation of previous agreement of only defining CSI computation requirement 2 for 480 and 960 kHz SCS. [22, LG] thought it is uncertain whether CSI computation delay requirement 2 could be still applied when a CSI report for 480 kHz or 960 kHz is triggered without transmitting a PUSCH with either transport block or HARQ-ACK when UE’s all CPUs are unoccupied (where CSI computation delay requirement 1 is specified for this situation as in TS 38.214). Two interpretations (the first one is preferred in [22, LG]) are identified:

* for 480 and 960 kHz, delay CSI computation requirement 2 is applied regardless;
* above situation is not expected to occur in FR2-2 with 480 and/or 960 kHz SCS.

[22, LG] also raised an associated question on how to determine CSI delay for aperiodic CSI reporting in mixed SCS operation.

Moderator’s comment:

It is moderator’s understanding that the CSI computation delay requirement 1 in NR is defined for a very restricted/simplistic scenario in which only wideband CQI corresponding to up to 4 CSI-RS port in a single CSI resource without CRI report is requested and only single-panel codebook is configured. That is also the motivation/reason for previous agreement of only defining CSI computation delay requirement 2 for NR operation with 480 and/or 960 kHz SCS. Although the above mentioned situation (where CSI computation delay requirement 1 is applied in TS 38.214) is less likely to occur in FR2-2 with 480 and/or 960 kHz SCS, an explicit agreement to align the interpretation would help to clarify.

##### Proposal 1-4

For NR operation with 480 kHz and/or 960 kHz SCS, CSI computation delay requirement 2 is always applied.

* Note: this applies to mixed SCS operation

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We tend to agree with LG and also **support the proposal** |
| Qualcomm | We support the proposal |
| Intel | Ok with proposal. |
| Vivo | We support the proposal. |
| LG Electronics | In our view, two clarifications are required for the agreement of CSI computation requirement 2.  The first is the question of whether the delay requirement 2 is always applied for NR with 480/960 kHz SCS, as Moderator has outlined well, and we agree with the proposal (except Note above).  Second, in the case of mixed SCS, it is necessary to check whether the delay requirement 2 is always applied only when all SCSs related to the aperiodic CSI report are 480 kHz (and/or 960 kHz), or when at least one of the related SCSs is 480 kHz (or 960 kHz). To give an example of this, we have excerpted a paragraph from our contribution as below.  *In addition, according to TS 38.214, the CSI computation delay is determined as the minimum SCS of (1) aperiodic CSI-RS, (2) PDCCH scheduling the CSI-RS, and (3) PUSCH with corresponding CSI report. Considering this fact together with the above agreement, it may be necessary to clarify whether the requirement 2 is only applied even in the case of mixed SCS of PDCCH, CSI-RS and PUSCH. For example, when PDCCH is configured with 120 kHz SCS and CSI-RS/PUSCH are configured with 480 kHz SCS, the CSI computation delay for 120 kHz SCS may be applied to that CSI reporting. At this time, if the aperiodic CSI report is triggered without transmitting a PUSCH with either transport block or HARQ-ACK when L = 0 CPUs are occupied, the UE may assume 43 symbols for 120 kHz as the CSI computation delay by requirement 1, instead of 388 symbols for 480 kHz. The absolute time of 43 symbols for 120 kHz is less than the half of the time of 388 symbols for 480 kHz. Whether it is an intended behavior is needed to clarify.* |
| Nokia/NSB | Support the proposal. |
| Apple | Fine with the proposal |
|  |  |
| Moderator | To LG:  Thanks for your further clarification. Previous wording of note means that CSI computation delay requirement 2 is always applied for the case of mixed SCS (where at least one of SCS is 480 kHz or 960 kHz). In the example you mentioned: PDCCH is configured with 120 kHz SCS and CSI-RS/PUSCH are configured with 480 kHz SCS. Let’s say the CSI computation delay for 120 kHz SCS may be applied to that CSI reporting according to TS 38.214. If following the above proposal, that’s CSI computation delay requirement 2 for 120 kHz SCS with aperiodic CSI report triggering, which has the same absolute time as that for 480 kHz SCS. Do you see a problem with this approach?  If your intention is to discuss some case where delay requirement 2 may be not applied, then I’ve added FFS instead of the original note in Proposal 1-4a. Please check if that is aligned with your intention.  To all companies, please comment on whether you see the need of FFS in Proposal 1-4a or support original Proposal 1-4. |
|  |  |

##### Proposal 1-4a

For NR operation with 480 kHz and/or 960 kHz SCS, CSI computation delay requirement 2 is always applied.

* FFS: whether CSI computation delay requirement 2 is not applied in the case of mixed SCS of PDCCH, CSI-RS and PUSCH.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Futurewei | We are fine with the proposal 1-4a. |
| ZTE, Sanechips | We are Ok with this proposal. |
| Ericsson | Fine with Proposal 1-4a.  Certainly it is important to support mixed SCS cases especially given that RAN4 has agreed on FR1 + FR2-2 band combinations. |
| NTT DOCOMO | Support the proposal. |
| Huawei, HiSilicon | Fine with Proposal 1-4a |
| Apple | We are fine with the proposal. |

#### Other timeline parameters

Multiple contributions looked at other timeline parameters.

[1, Huawei] proposed that in general, the absolute time of 120 kHz SCS timelines should be adopted by default unless the reduced value for specific timeline(s) can be verified by implementation.

Among parameters d1,1, d2, Text, d2,1, Tswitch, d2,2, [5, vivo] proposed that only parameter d2,2 (BWP switch delay) for 480/960 kHz SCS should use the absolute time duration for 120 kHz SCS as the upper bound for FR2-2 in Rel-17.

For 480kHz and 960kHz, [16, MediaTek] and [22, LG] proposed *d1,1* and *d2* (to derive *Tproc,1* in PDSCH processing time) and *d2,1* and *d2* (to derive *Tproc,2* in PUSCH preparation time) are scaled by 4 and 8 for 480kHz and 960kHz, respectively.

[23, Apple] proposed that for NR operation with 480 and 960 kHz SCS, adopt at least the values of for all UE processing times for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2 to the following parameters.

* + HARQ-ACK information in response to a SPS PDSCH release, 38.213 Section 10.2
  + HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, 38.213 Section 10.3
  + BWP Delay, 38.133, Section 8.6
  + Minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6): 38.213 Section 10.3
  + Determination of the resource allocation table to be used for PUSCH, 38.214 Section 6.1.2.1
  + UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, 38.214 Section 5.5
  + Application delay of the minimum scheduling offset restriction: 38.214 Section 5.3.1/6.1

[25 Qualcomm] proposed to choose the j values for PUSCH default TDRA tables as ceil(N2/14).

Moderator’s comment:

Considering previous agreement of N1/N2/N3 and Z1/Z2/Z3 values, formulate the following proposals to maintain the same absolute time duration as that of 120 kHz SCS in FR2 for other timeline values.

##### Proposal 1-5

For NR operation with 480 kHz and/or 960 kHz SCS, *d1,1* and *d2* (to derive *Tproc,1* in PDSCH processing time) and *d2,1* and *d2* (to derive *Tproc,2* in PUSCH preparation time) are scaled by 4 and 8 for 480kHz and 960kHz, respectively.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We support the proposal |
| Vivo | We support the proposal |
| LG Electronics | We support the proposal. The extra symbols *d1,1, d2,1* and *d2* to derive Tproc should be scaled by 4/8 for 480/960 kHz. Otherwise, the effect of the extra symbol cannot be expected for 480/960 kHz. |
| Nokia, NSB | There is no need to scale these values. The impact is neglectable in any case (due to the large parameter values defined for N1/N2) |
| Apple | We support the proposal |
| InterDigital | We are fine with the proposal. |
| Samsung | It is unclear to us. Contrary to N1, the value of d1,1 and d2 is independent to SCS in Rel-15/16. Now, the proposal is to scale d1,1 and d2 according to SCS. Proponents please elaborate motivations behind the proposal. Also, N1 and N2 for 480/960k SCS is quite loose so that additional processing time relaxation may be unnecessary. |
| Futurewei | We suggest to make this issue FFS. |
| ZTE, Sanechips | We are OK with the proposal. |
| Ericsson | Agree with view from Nokia and Samsung given large N1/N2/N3 and also that these values due not scale with SCS in Rel-15/16. |
| NTT DOCOMO | Support the proposal. |
| Xiaomi | Fine with the proposal |
| Huawei, HiSilicon | We support proposal 1-5 |

##### Proposal 1-6

For NR operation with 480 kHz and/or 960 kHz SCS, scale the corresponding values of 120 kHz SCS by 4x/8x for 480 kHz and 960 kHz SCS respectively for the following UE timeline parameters for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.

* + HARQ-ACK information in response to a SPS PDSCH release, *N* in 38.213 Section 10.2
  + HARQ-ACK information in response to a detection of a DCI format 1\_1 indicating SCell dormancy, *N* in 38.213 Section 10.3
  + BWP switch delay, in 38.133 Section 8.6
  + Minimum time gap for wake-up and Scell dormancy indication (DCI format 2\_6): X in 38.213 Section 10.3 and 38.133 Section 8.2.1.2.7
  + Determination of the resource allocation table to be used for PUSCH, *Δ* in 38.214 Section 6.1.2.1.1
  + UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH, *Npdsch* in 38.214 Section 5.5
  + Application delay of the minimum scheduling offset restriction, *Zµ* in 38.214 Section 5.3.1

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We support the proposal |
| Vivo | We support the proposal |
| LG Electronics | We support the proposal in principle.  However, applying the same principle to all of the above parameters may cause several issues. For example, in the case of BWP switch delay, in fact it is the RAN4 responsibility, the following agreement was already made at the last meeting.   * Update Table 8.2.2.2.1-1 in TS 38.133 with 480/960 kHz subcarrier spacing as below:   **Interruption length X**   |  |  |  | | --- | --- | --- | | **cid:image001.png@01D7AA79.D2378E60** | **NR Slot** | **Interruption length X (slots)** | |  | **length (ms)** |  | | 0 | 1 | 1 | | 1 | 0.5 | 1 | | 2 | 0.25 | 3 | | 3 | 0.125 | 5 | | 5 | 0.03125 | 17 | | 6 | 0.015625 | 33 | | Note1:       void | | |   Therefore, it is necessary to investigate each timeline parameter on a case-by-case basis. |
| Nokia/NSB | Agree in principle. |
| Apple | Support the proposal |
| InterDigital | We are fine with the proposal. |
| Samsung | For the first two, *N* should be *N3*(HARQ-ACK multiplexing timeline).  For other values, more discussion is needed. |
| Futurewei | Agree with the proposal in principle. But as pointed out by LG, certain parameter might need further consideration. |
| ZTE, Sanechips | We are OK with the proposal. |
| Ericsson | Agree with LGE that the BWP switch delay is a RAN4's responsibility  Agree with views from Samsung that more discussion is needed |
| NTT DOCOMO | Support the proposal. |
| Xiaomi | Fine with the proposal |
| Huawei, HiSilicon | We support proposal 1-6 |

##### Proposal 1-7

For NR operation with 480 kHz and/or 960 kHz SCS, *j* = 11 for 480 kHz and *j* = 21 for 960 kHz for determination of the default PUSCH time domain resource allocation (in 38.214 Section 6.1.2.1.1).

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We support the proposal |
| Vivo | We support the proposal |
| Nokia, NSB | This is too early to decide. One should e.g. decide first what is the default the mode of operation (i.e. single PUSCH, or multi-PUSCH). |
| Ericsson | The proposed values of j make sense, i.e., ceil(N2/14). Hence we support Proposal 1-7. |
| NTT DOCOMO | Support the proposal. |
| Xiaomi | Fine with the proposal |
| Huawei, HiSilicon | Agree with proposal 1-7 |
| Apple | We are fine with the proposal |

#### CSI processing unit

Several contributions discussed issues related to CSI processing unit (CPU).

Regarding CPU, [13, Nokia] argued that CPU is the UE capability for simultaneous CSI calculations which is indicated as and is related to channel variation or UE mobility rather than scheduling/subcarrier spacings. Therefore, there is no reason to increase the frequency of CSI reporting or rule for calculation of CSI occupancy. Given is independent from numerology, [13, Nokia] observed that the existing specification for CPU can be reused for 480kHz and 960kHz SCS.

[20, Lenovo] raised an issue and thought it is critical to handle CPU availability check for UEs when it is required to process multiple CSI reports associated with different SCS values ranging from 15kHz to 960kHz in a parallel manner. It proposed same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values.

[22, LG] also looked into CPU availability check for multiple numerologies across active BWPs in different component carriers. It observed that in case multiple CSI reports are configured with multiple SCSs, the chance for high SCS to get available CPU at the time of checking unoccupied CPU may be less than that for low SCS. One mentioned solution for that is use of reference SCS for all CPU availability check regardless of actual SCS where reference SCS can be the lower SCS than the configured SCS, especially when high SCS is configured for UE.

Moderator’s comment:

Two companies proposed to enhance CPU availability check and one company thought existing specification can be reused with no enhancement.

On the mentioned issue of CPU availability check for multiple numerologies, it seems the same issue would happen for Rel-15/16 NR as long as there’re multiple numerologies involved. Suggest the proponent companies to clarify the necessity of this enhancement/solution for 480 and/or 960 kHz SCS.

With limited input on this issue, suggest other companies to provide input for discussion.

##### Discussion point 1-8

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | As commented in previous discussions related to this issue, indication of number of CPUs is UE capability, however the intervals at which CPU availability is checked is related to symbol duration. Now, with the introduction of higher SCS up to 960kHz, the CPU availability check with 960kHz and 480kHz can be much more frequent in comparison to lower SCS. Therefore, the absolute opportunities could vary quite significantly. Therefore, the proposal to have same intervals/granularity for CPU availability check regardless of SCS should be supported.  Also, this is quite a simple enhancement and doesn’t impact how the actual processing timeline, but just fairer in terms of CPU availability check for all SCS values. |
| LG Electronics | Since the last meeting, many timelines for 480/960 kHz SCS have been aligned with those for 120 kHz. The reason is that consecutive processing of symbols/slots having a shorter length may be a burden to the UE. In addition, the CSI computation time for 480/960 kHz was also determined based on 120 kHz. The same principle can be applied to the CPU availability check, which was done in units of symbols in Rel-15. Simple solution for that is use of reference SCS for all CPU availability check regardless of actual configured SCS. For instance, the reference SCS used to check the CPU availability for 480/960 kHz SCS can be set to 120 kHz. That is, by using 4/8 symbol duration for 480/960 kHz as a time unit for CPU check, the use of the common time unit for CPU check is possible for both 480/960 kHz and 120 kHz SCSs. Moreover, through the use of 120 kHz as a reference SCS for CPU availability check, any issue that may occur due to the asymmetric CPU check rate between 480/960 kHz and 120 kHz in a mixed SCS can be solved. |
| Nokia, NSB | We think that no enhancements are needed (i.e. Rel-15/16 schemes for CPU can be reused for 480kHz and/or 960kHz SCS). |

## 2.2. PTRS

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | Observation 6: Block PTRS with the designed circular sequence has better BLER and spectrum efficiency than distributed PTRS when power boosting is applied.  Proposal 15: Support block PTRS as one type of PTRS pattern for 120 kHz, 480 kHz and 960 kHz SCS of CP-OFDM. The use of block PTRS can be indicated by MCS, scheduled bandwidth, and power boosting scheme. The PTRS sequence is composed of ZC sequence and circular part based on ZC sequence for block PTRS.    Observation 7: With more PTRS groups and less PTRS samples per PTRS group denoted as (, ) = (16, 2), the BLER performance of all the SCSs are improved significantly.  Proposal 16: A new PTRS pattern with more PTRS groups and less PTRS samples per PTRS group denoted as (, ) = (16, 2) within one DFT-s-OFDM symbol should be supported for large scheduling bandwidth and high scheduled MCS.  Proposal 17: The detailed scheduling bandwidth and MCS threshold to use for the new PTRS pattern can be reported by UE or decided by gNB for different SCSs.  Observation 8: Due to Rx timing shift, (at least part of) a PTRS group placed at the tail of the transmitter’s DFT-s-OFDM symbol, may wrap-around to the head of the symbol from the receiver’s perspective, thus spoiling the original intention of the design and unnecessarily increasing Rx complexity, as well as deteriorating PN compensation performance, especially for the high MCS.  Observation 9: New PTRS location which is in the middle of each interval can solve the influence on BLER performance caused by Rx advance timing shift.  Proposal 18: For PTRS with , the mapping of last PTRS group should consider potential Rx timing shift and avoid the last X pre-DFT symbol(s).  Proposal 19: New PTRS location which is in the middle of each interval with same overhead whose last PTRS group won’t be mapped at the tail of the symbol should be supported to solve the influence induced by Rx advance shift especially for high MCS which is larger than MCS22. |
| [2, Futurewei] | Proposal 5. For PDSCH with CP-OFDM and small number of RBs allocated, consider increasing the density of PTRS to (K=1, L=1).  Proposal 6. For larger RB allocations, increasing PTRS density to (Ng = 16, Ns = 4, L = 1) can be considered for PUSCH in FR2-2 if 64QAM is used; for lower order modulations such as 16QAM and QPSK, the legacy density (Ng = 8, Ns = 4, L = 1) offers fine performance, thus can be reused. For smaller RB allocations, the legacy density performs well under different modulations and no enhancement is necessary. |
| [4, ZTE] | Observation 1: When PRB number is not larger than 32, CPE compensation with lower PTRS density can achieve similar or better performance than ICI compensation with higher PTRS density.  Proposal 11: Do not introduce K=1 for Rel-15 PTRS pattern for CP-OFDM with small (< =32) RB allocation.  Observation 2: Block PTRS with cyclic sequence cannot provide performance gain compared with legacy PTRS.  Observation 3: Block PTRS with power boosting cannot achieve better performance than legacy PTRS.  Observation 4: Introducing a new PTRS pattern requires great spec efforts at least on sequence construction, RRC parameters and PTRS pattern type indication.  Proposal 12: Reuse the Rel-15 legacy PTRS pattern for 52.6GHz~71GHz.  Observation 5: Increasing PTRS groups for DFT-s-OFDM waveform can bring benefit to performance of 120kHz SCS and MCS 22.  Proposal 13: Support to increase the number of PTRS groups for DFT-s-OFDM. |
| [5, vivo] | Observation 1:   * The performance of de-ICI (3-tap filter) with K\_PTRS = 2 is worse than K\_PTRS = 1 when PDSCH RB number <= 16; * When PDSCH RB number <= 16, CPE only with K\_PTRS = 2 has much better performance than de-ICI with K\_PTRS = 1. * For all evaluated cases, the preferred method for PN compensation (with the best performance) is shown in Table 4. The best performance is obtained with legacy PTRS density in frequency, i.e. K\_PTRS = 2. There’s no motivation to justify higher PTRS density in frequency domain for small RB allocation.   Table 4 Preferred PN compensation method when number of RB <=32   |  |  |  |  |  | | --- | --- | --- | --- | --- | | SCS (kHz)/MCS | 7 | 16 | 22 | 26 | | 120 | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | no method to achieve 10% BLER. | | 480 | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | If PDSCH RB num <= 16, use CPE only (K\_PTRS=2); else, use de-ICI (K\_PTRS=2). | | 960 | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | If PDSCH RB num <= 16, use CPE only (K\_PTRS=2); else, use de-ICI (K\_PTRS=2). |   Proposal 1: For FR2-2, there is no need to introduce higher PTRS frequency density as K\_PTRS = 1 in Rel-17.  Observation 2: With current simulation parameters, the performance of de-ICI with Rel-15 PTRS pattern outperforms the performance of block-based PTRS pattern with cyclic ZC sequence.  Observation 3: For block-based PTRS pattern with zero-power RE, the performance of ‘6dB power boosting’ is around 2.5 dB worse than that of ‘full power boosting’ for SNR achieving 10% BLER.  Observation 4: For block-based PTRS pattern with zero-power RE, the performance of ‘full power boosting’ doesn’t outperform the performance of ‘de-ICI with Rel-15 PTRS pattern’.  Proposal 2: For FR2-2, do not support block-based PTRS pattern in Rel-17.  Observation 5: The performance gap is not obvious between (CN, CS) = (8, 4) and the configuration with the best performance for most of the cases on MCS-7 and MCS-16.  Observation 6: For MCS-22/MCS-26 and PUSCH RB number as 256, configuration (CN, CS) = (16, 4) achieves best performance.  Proposal 3: The necessity to introduce more PTRS chunk number needs further discussion as there is no significant performance benefit. If there is valid reason to introduce more PTRS chunks, configuration (CN, CS) = (16, 4) can be considered. |
| [9, Mitsubishi] | [Observation 1: For a distributed PT-RS pattern, the performance is poor even with de-ICI filtering, due to an insufficient number of PT-RS samples. Cyclic block patterns still yield better results.](#_Toc83998901)  [Observation 2: For a distributed PT-RS pattern, de-ICI Wiener filtering outperforms CPE in all cases, but high MCS still not reach FER=0.1.](#_Toc83998902)  [Observation 3: Distributed PT-RS patterns are not robust enough to ensure system performance in bands above 52.6GHz, especially with high MCS and/or at 70GHz.](#_Toc83998903)  [Observation 4: For a similar overhead, block PT-RS (with any ordinary non-cyclic sequence) is outperformed by distributed PT-RS pattern when a same de-ICI Wiener filter is used at the receiver side. There is no interest in supporting block non-cyclic sequences.](#_Toc83998904)  [Observation 5: PT-RS blocks with a ZP pattern outperforms the distributed PT-RS pattern, even with dense distributed patterns.](#_Toc83998905)  [Observation 6: Block PT-RS with cyclic sequence significantly outperforms the distributed PT-RS pattern with ICI compensation. The gain increases with the carrier frequency and the MCS.](#_Toc83998906)  [Observation 7: Block PT-RS with cyclic sequence outperforms block PT-RS with ZP pattern.](#_Toc83998907)  [Observation 8: Block PT-RS with cyclic sequence requires lower complexity phase noise compensation filtering than the de-ICI filter needed for the distributed PT-RS pattern.](#_Toc83998908)  Proposal 1: Support block PT-RS with cyclic sequence for OFDM waveform.  Proposal 2: A PT-RS sequence for OFDM waveform composed of KP samples includes a cyclic prefix of floor(KP/2) samples.  Proposal 3: Support density extension of current Rel.15 PT-RS for DFTsOFDM waveform. |
| [10, CATT] | Proposal 17: For NR operation in 52.6 to 71 GHz with OFDM, PTRS enhancement is not supported. |
| [12, Ericsson] | Observation 8 Even for small RB allocation, enhanced PTRS structure with K = 1 or K=0.5 does not provide additional performance gain over the existing Rel-15 PTRS structure (K = 2 and K=4).  Observation 9 For every tested scenario, Rel-15 PTRS + direct de-ICI receiver with multiple settings for the PTRS density can be used to outperform the best settings for square and orthogonal circulant PTRS with square and orthogonal circulant ICI filter approximation without significant phase noise compensation complexity increase or even decreased phase noise compensation complexity.  Observation 10 For every tested scenario, best setting for orthogonal circulant PTRS with 3 dB power boosting does not provide additional gain over the best setting for existing Rel-15 PTRS structure + direct de-ICI receiver.  Observation 11 The performance of square and orthogonal ICI filter approximation is worse than Rel-15 PTRS structure with direct de-ICI filtering because of the various fundamental design issues identified in Annex A:  1. ICI filter approximation with block PTRS does not fully utilize all received PTRS symbols.  2. Phase noise compensation with ICI filter approximation approach relies on an auto-deconvolution assumption that is not valid in practice.  3. The construction of a circulant matrix with cyclic block PTRS sequence relies on an assumption that is invalid for frequency selective channels.  4. The approximate filter estimation with circulant PTRS matrix involves anti-match-filter combining, which amplifies noises from clusters and subcarriers with weak received SNR.  Observation 12 The ICI filter approximation receiver with single-tone PTRS (see Annex A.5) requires excessive power boosting which can result in both substantial link performance losses and severe out-of-band intermodulation leakages.  Proposal 28 Retain the same Rel-15 distributed PTRS design for OFDM for all RB allocations. Additional PTRS structure(s) are not needed. |
| [13, Nokia] | Observation 3. Existing PTRS configurations for OFDM provide good allocation flexibility to achieve good performance for any bandwidth, SCS, or MCS.    Observation 4. Considerable benefit from increasing PTRS density to K=1 is observed only in a single case when high-order modulation is used and PRBs=16 and ICI compensation is used.  Observation 5. No gain is achieved using K=0.5.  Observation 6. Using small PRB allocations with high MCSs is a corner case and should not be considered to motivate new PTRS configurations  Proposal 13. Do not consider increasing PTRS frequency density for small PRB allocations (<32).  Observation 7. PN compensation algorithm has impact on the block PTRS performance.  Observation 8. Block PTRS patterns can achieve similar performance as distributed patterns.  Proposal 14. If the receiver compensation complexity reduction using block PTRS patterns is proved to be clear, block PTRS could be considered for Rel-17.  Observation 9. PUSCH performance of DFT-s-OFDM may be improved by increasing the maximum number of PTRS groups with well affordable PTRS overhead.  Observation 10. New PTRS configurations can give performance gains for high order modulations.  Observation 11. Increasing the number of PTRS groups to 16 by the proposed fractional mapping can provide 1.2dB gain using 4 samples per group, and 0.8dB gain using 2 samples per group over existing 8x4 pattern when using MCS22.  Proposal 15. Consider increasing number of PTRS groups for DFT-s-OFDM to make high order modulations robust to phase noise when a large number of PRBs is used.  Proposal 16: Consider increasing the number of PTRS groups to 16 by introducing a PTRS mapping unit in terms of fraction (or multiple of) DFTsOFDM symbols, to flexibly control PTRS overhead and allocation. |
| [15, Samsung] | Observation 1: At 60GHz, two block PTRS patterns with ICI approximation filter show some performance gain comparing to Rel-15 PT-RS with de-ICI algorithm. The gains are widened at 70GHz.  Observation 2: Block PTRS patterns 2 (cyclic PTRS sequence with 3dB power boost) provides better performance than block PTRS pattern 1 (patterns with ZP tones in both side) at 10% target BLER. The performance order reverses at 1% target BLER.  Proposal 3: Block PTRS pattern is beneficial for performance improvement and UE complexity reduction compared to legacy PTRS pattern.  Observation 3: For small RB allocations (32RB/16RB/8RB) and legacy PTRS frequency density (K=2 and K=4), CPE compensation outperforms the one with ICI compensation.  Observation 4: For small RB allocations (32RB/16RB/8RB), K=1 provides further gains compared with legacy PTRS frequency density.  Proposal 4: For smaller RB allocations, increasing PTRS frequency density (ex, K=1) is beneficial for further performance optimization. |
| [17, Intel] | Proposal 14: RAN1 to introduce UE capability of supporting high MCS/rank combinations in FR2-2.  Observation 1: De-ICI filtering performance can be improved by using conjugate anti-symmetric filter.  Observation 2: De-ICI filtering performance can be improved by using CP-based linear phase ramp pre-compensation.  Observation 3: De-ICI performance can be improved by applying the unit-magnitude de-ICI compensation in time domain.  Observation 4: block PT-RS pattern (42-tone blocks) with PN spectrum-based de-ICI filter estimation provides ~1dB better performance than Rel-15 PT-RS pattern with direct de-ICI filter estimation at MCS20 Rank 2.  Observation 5: the maximal supported MCSs are as follows: SCS120kHz, rank 1 – MCS27 (high complexity), MCS26 (medium complexity), SCS120kHz, rank 2 – MCS21, SCS960kHz, rank 1 – MCS27, SCS960kHz, rank 2 – MSC25.  Proposal 15: Adopt block PT-RS pattern for PDSCH.  Observation 6: Unequal distribution of PN estimation error among DFT-s-ODFM samples may lead to systematic unbalance between code blocks’ BLERs.  Observation 7: PUSCH PTRS patterns with only 4 and 8 PTRS groups provide acceptable performance with 120kHz SCS.  Observation 8: Code blocks interlacing within a DFT-s-OFDM symbol provides performance gain from 0.5dB to 1.7dB at MCS22.  Proposal 18: RAN1 to consider code blocks interlacing for PUSCH with transform precoding.  Proposal 19: Adopt PT-RS pattern with Ng = 16, Ns = 2 for PUSCH with transform precoding.  Observation 9: per-OFDM symbol CBs interlacing substantially improves the performance for all the tested scenarios (across different PT-RS patterns, MCSs, SCSs and FDRAs).  Observation 10: applying CBs interlacing allows to support the full range of MCSs using the existing (8,4) PT-RS pattern for 960kHz SCS.  Observation 11: time shift agnostic DFT-s-OFDM PN compensation leads to ~6-10dB degradation when Rx time shift is close to the time spacing between the last PT-RS group and the end of the symbol.  Observation 12: time shift aware DFT-s-OFDM PN compensation reduces the degradation to ~0.3-4.5dB when Rx time shift is close to the time spacing between the last PT-RS group and the end of the symbol.  Observation 13: edge-aligned and center-aligned DFT-s-OFDM PT-RS patterns outperforms one another within different Rx timing shift ranges, if time shift agnostic PN compensation is applied.  Observation 14: center-aligned DFT-s-OFDM PT-RS pattern ensures slow performance degradation with small Rx timing shifts, if time shift agnostic PN compensation is applied.  Observation 15: center-aligned DFT-s-OFDM PT-RS patterns outperform edge-aligned patterns across the whole range of Rx timing shifts, if time shift aware PN compensation is applied.  Proposal 20: adopt the center-aligned version of (8,4) and (16,2) PT-RS patterns. |
| [19, CEWiT] | Proposal 1: Support for new PT-RS design for NR above 52.6GHz at least for 120KHz SCS.  Proposal 2: Support Block-PTRS as one of the candidates for new PTRS design for NR above 52.6GHz.  Proposal 3: Time density can be decided based on MCS, as in FR1 and FR2.  Proposal 4: Higher PTRS densities such as (Ng = 16, Ns = 2, L = 1) and/or (Ng = 16, Ns = 4, L = 1) are not required for DFT-s-OFDM for FR2-2. |
| [21, InterDigital] | Observation 4: Compared to Rel-15 PTRS configuration, block PTRS designs with similar PTRS overhead does not provide significant performance gains.  Observation 5: A low-complex 3 taps de-ICI filter () based on existing Rel-15 NR PTRS structure can provide protection against performance degradation due to phase noise.  Proposal 10: Rel-17 NR operation in 52.6-71 GHz follow Rel-15/Rel-16 PTRS design for CP-OFDM, at least when allocated RBs > 32.  Proposal 11: The need of PTRS enhancement for small RB allocation ( 32 RBs) should be carefully evaluated.  Proposal 12: Use Rel-15/16 PTRS design for DFT-s-OFDM unless new use cases are found for which enhancements are necessary. |
| [22, LG] | Proposal #19: Retain the existing distributed PT-RS structure for all SCS in FR2-2. It seems that further improvement either by advanced estimation algorithms or by new PT-RS pattern cannot achieve a noticeable improvements.  Proposal #20: Keep current PTRS density values K = 2 and K = 4, without extending the set.  Proposal #21: Do not support (Ng=16, Ns=4) configuration  Proposal #22: Consider (Ng=16, Ns=2) configuration for high MCS only if the necessity of using high MCS in DFT-s-OFDM transmission is identified |
| [23, Apple] | Observation 1: At lower SNRs, there is a trade-off between the overhead of the PTRS selected and the throughput. Achieving the best throughput performance requires a lower value of K (K =1) than is currently available in the Rel-15 specification.  Proposal 8: RAN1 should support K = 1 for smaller frequency allocation sizes for PTRS in CP-OFDM.  Observation 2: Gains over the baseline are made with Ng = 16, Ns = 2, L = 1 only and only at high SNRs  Proposal 9: Support Ng = 16, Ns = 2, L = 1 only if need for high MCS for DFT-S-OFDM can be justified. |
| [25, Qualcomm] | Proposal 1: Do not introduce new PTRS pattern (block-based pattern) for Rel. 17.  Observation 1: For small RB allocation, e.g., 16 or 8 RBs, sending the PTRS over every RB, i.e., K=1, enhances the performance as it helps in having more accurate ICI filter calculations or CPE estimates. In addition, the performance is degraded when the density is increased with K=0.5 due to the large overhead and increase coding rate.  Proposal 2: As PTRS enhancement for assisting ICI compensation, increasing the frequency domain density, of Rel. 15 PTRS, for small RB allocation can be considered.  Observation 2: For small RB allocation such as 64 RB, the legacy pattern (Ng = 8, Ns = 4, L = 1) is outperforming the other patterns.  Observation 3: For 128 RB allocation, the gain from the new pattern (Ng = 16, Ns = 4, L = 1) can be observed at the tail of the BLER curve, while for 256 RB allocation, the gain from the new pattern (Ng = 16, Ns = 4, L = 1) can be observed at both 10% and 1% BLER points (~0.8 dB).  Observation 4: The performances of the legacy pattern (Ng = 8, Ns = 4, L = 1) and the new pattern (Ng = 16, Ns = 2, L = 1) are very close to each other for larger RB allocations 128 and 256 RBs  Proposal 3: Do not introduce new PTRS pattern for the SC-FDM waveform. |

### Summary on PTRS

#### For CP-OFDM

In RAN1#104-e meeting, the following was agreed.

* At least existing PTRS design for CP-OFDM is supported for NR operation in 52.6 to 71 GHz.
* Companies are encouraged to study the need of potential PTRS enhancement for CP-OFDM with respect to phase noise compensation performance considering at least the following aspects:
  + PTRS density/pattern (e.g. distributed, block-based) and sequence (e.g. cyclic sequence)
  + Frequency domain power boosting and its impact to PDSCH performance and PDSCH to DMRS EPRE
  + Receiver complexity, including possible aspects related to supporting both existing PTRS design and potential PTRS enhancement
  + Possible specification impact of supporting potential PTRS enhancement in addition to existing PTRS design
  + Note: PTRS overhead should be accounted for in the evaluations, e.g. by showing spectral efficiency results and/or reporting effective coding rate

In RAN1#106-e, the following was agreed.

Agreement:

Further study and conclude on whether to introduce any PTRS enhancement for CP-OFDM by RAN1#106b.

* Note: details of specification impact for any proposed PTRS enhancement shall be provided to facilitate drawing conclusion in RAN1#106b

The following contributions submitted to this meeting evaluated and compared different PN compensation performance using the existing Rel-15 NR distributed PTRS structure against new PTRS patterns and/or new sequence.

[1, Huawei] compared BLER performance of Rel-15 PTRS and a block PTRS with cyclic sequence when ICI PN compensation is used. Power boosting is applied to only block PTRS with decreased power of data, making sure the total power per OFDM symbol are same between block PTRS and Rel-15 PTRS pattern. It observed a performance gain of {0.2dB, 0.5dB and 0.8dB} for {MCS22, MCS26 and MCS28} respectively with 64QAM and 120 kHz, 64 RB, when compared block PTRS with Rel-15 PTRS. It also observed about 0.9 dB and 0.55 dB gain for block PTRS for 480 kHz and 960 kHz respectively with 256QAM and MCS 21, 64 RB.

The corresponding text proposal to specification 38.211 and 38.214 for the proposed block PTRS patterns is provided in [1, Huawei].

[4, ZTE] evaluated PDSCH with CP-OFDM performance with the legacy PTRS and block PTRS with cyclic ZC sequence for 120 and 480 kHz SCS with 64QAM/MCS 22 and 256 RB. The evaluation was performed with different ICI estimation filter tap number, block number and sequence length for each block. It is observed that the performance of ICI compensation based on legacy PTRS is always better than block PTRS with cyclic sequence. It also evaluated the performance both PTRS patterns with and without 3dB power boosting and showed that the performance of legacy PTRS without power boosting is still better than block PTRS with 3 dB power boosting.

[4, ZTE] also observed that introducing a new PTRS pattern requires great specification efforts at least on sequence construction, RRC parameters and PTRS pattern type indication.

[5, vivo] compared CP-OFDM performance for CPE with Rel-15 PTRS, de-ICI (5-tap filter) with Rel-15 PTRS, ICI filter approximation (3 PTRS blocks, 21 PTRS tones/ Block, 5-tap filters), de-ICI (5-tap filter) with a block PTRS with cyclic ZC sequence and PN-spectrum based ICI filter approximation (3 PTRS blocks, 21 PTRS tones/ Block, 5-tap filters) for 120 kHz SCS with 64QAM/MCS22, 256 RB. When 3 dB power boosting is applied to PTRS for all schemes, it observed that the performance of de-ICI with Rel-15 PTRS pattern outperforms block PTRS schemes. [5, vivo] also evaluated performance for a block PTRS with ZP. It observed that a significant performance loss for block PTRS of 7 clusters with 9 tones (8 ZP and 1 NZP) when power boosting is 6 dB for that 1 NZP RE compared to full power boosting.

[9, Mitsubishi] compared phase noise compensation performance for the following cases with 120 kHz SCS: CPE-based for Rel-15 PTRS, de-ICI for Rel-15 PTRS, de-ICI for block PTRS, de-ICI for ZP block PTRS and ICI filtering for block PTRS with cyclic sequence. It is observed that for a similar overhead, block PTRS (with any ordinary non-cyclic sequence) is outperformed by distributed Rel-15 PTRS pattern when a same de-ICI filter is used at the receiver side. It also observed that with de-ICI, PTRS blocks with a ZP pattern outperforms the distributed Rel-15 PTRS pattern. Furthermore, it observed that ICI filtering for block PTRS with cyclic sequence outperforms de-ICI for block PTRS with ZP pattern.

It is observed that for the same overhead, block PT-RS with cyclic sequence gains around 0.5dB with respect to distributed PT-RS sequence for 16QAM2/3 at 60GHz, 256 RB. It is also stated in [9, Mitsubishi] that “for medium MCS we observe gains in order of 1-2dB for FER target 10-1” and “for high MCS, in some scenarios only block PT-RS with cyclic sequence reaches target FER of 10-1”.

[9, Mitsubishi] observed that the PN compensation filter used for block-PT-RS with cyclic sequence is less complex than the de-ICI Wiener filter used for ICI compensation of the distributed PT-RS pattern.

Regarding specification impact for the proposed block PTRS with cyclic sequence, [9, Mitsubishi] identified one new higher layer parameter (to indicate which of the Rel.15 or enhanced block-based sequence is configured to be used), sequence generation and mapping to physical resources parts (a pattern , x ) in 38.211 and the corresponding modifications to the PT-RS transmission/reception procedure in 38.214.

[12, Ericsson] provided evaluation results on clustered-PTRS with cyclic sequence and investigated power boosting aspects for both 64 and 256 RB. Comparing the performance of Rel-15 PTRS and block-PTRS with square and orthogonal circulant sequence, it is observed that for every tested scenario, Rel-15 PTRS + direct de-ICI receiver with multiple settings for the PTRS density can be used to outperform (about 0.5 ~ 1 dB gain observed based on the reported results in table 9 to 12 in [12] for MCS 22 with 120 kHz) the best settings for square and orthogonal circulant PTRS with square and orthogonal circulant ICI filter approximation without significant phase noise compensation complexity increase or even decreased phase noise compensation complexity. Regarding power boosting, it observed that for every tested scenario, best setting for orthogonal circulant PTRS with 3 dB power boosting does not provide additional gain over the best setting for existing Rel-15 PTRS structure + direct de-ICI receiver. For high MCS (MCS 26), [12, Ericsson] observed that Rel-15 PTRS structure without power boosting has better or on par performance compared to orthogonal circulant PTRS with 3 dB power boosting in terms of required SNR at 10% BLER for both 64-RB and 256-RB allocation for 120 kHz, 480 kHz, and 960 kHz SCS. Finally, with respect to potential specification impact, [12, Ericsson] observed that clustered PTRS structure can frequently collide with existing NR reference symbols (such as CSI-RS and TRS) with no simple avoidance solution. [12, Ericsson] argued that introducing new clustered PTRS requires significant discussion on RB thresholds, MCS thresholds, adaptation between Rel-15 PTRS and alternative clustered PTRS structure, and new PTRS structure parameters (sequence, number of clusters, number of PTRS in each cluster, power boosting factor(s)).

[12, Ericsson] observed that complexity of ICI mitigation is dominated by frequency domain de-ICI filtering. Matrix inversion constitutes no more than 2% of the total complexity for realistic filter lengths and PXSCH allocations. With respect to block PTRS with ZP, it is observed that the ICI filter approximation receiver with single-tone PTRS requires excessive power boosting which can result in both substantial link performance losses and severe out-of-band intermodulation leakages

[12, Ericsson] also observed that the performance of square and orthogonal ICI filter approximation is worse than Rel-15 PTRS structure with direct de-ICI filtering due to various identified issues: ICI filter approximation with block PTRS does not fully utilize all received PTRS symbols; phase noise compensation with ICI filter approximation approach relies on an auto-deconvolution assumption that is not valid in practice; the construction of a circulant matrix with cyclic block PTRS sequence relies on an assumption that is invalid for frequency selective channels; ICI filter approximation with circulant PTRS matrix involves anti-match-filter combining, which amplifies noise from clusters and subcarriers with weak received SNR. On the issues identified above, [9, Mitsubishi] provided counter arguments to issue 3 (channel equalization) and issue 4 (average over PTRS blocks) and claimed issue 3 and 4 are solved.

[13, Nokia] compared performance using de-ICI filtering for legacy (distributed) PTRS and some block based patterns. For block based patterns, the following algorithms: ICI filter approximation method, de-ICI approach and Spectrum based estimation are compared. It is observed that the algorithms have some impact on the results, but basically it is possible to achieve similar performance for block PTRS patterns as distributed patterns. Thus, from performance perspective there seems to be no obvious difference for block based patterns.

[15, Samsung] compared the performance of three schemes: Rel-15 PTRS pattern with K=4 and no power boosting for PTRS, block PTRS with zeros tones and , with 9.54dB power boosted for NZP-PTRS, and block PTRS with cyclic sequence and , with 3dB power boosted for PTRS. For the case evaluated (120 kHz SCS with 256 RB, TDL-A 5 ns, MCS22, 60 GHz), it observed performance gain about 0.5~0.6 dB for both block PTRS patterns for 10% BLER target. The gains are widened at 70GHz with up to 1.9dB gain over some case.

[17, Intel] compared two PN compensation methods: PN spectrum-based (a.k.a. ICI filter approximation) and direct de-ICI filter coefficients estimation with different PTRS block sizes for 120 kHz. It observed that the performance of PN-spectrum based estimation algorithm drastically varies among the PTRS block sizes. It showed that PN-spectrum based approach is inferior to the direct one at the small PT-RS block sizes, while it outperforms the competing algorithm at large PTRS blocks. It observed that block PT-RS pattern (42-tone blocks) with PN spectrum-based de-ICI filter estimation provides ~1dB better performance than Rel-15 PT-RS pattern with direct de-ICI filter estimation at MCS20 Rank 2.

[17, Intel] stated that the coefficients estimation complexity is a smaller portion of de-ICI processing, while the larger one is the frequency domain de-ICI filtering itself. Note in their evaluation, the original Rel-15 PTRS Gold sequence was used.

[21, InterDigital] evaluated Rel-15 PTRS against block PTRS patterns for MCSs 16, 22, and 24 along with SCSs 120 kHz, 480 kHz, and 960 kHz. Two cases are considered for PN compensation (a) compensating only CPE, (b) compensating for both CPE and ICI. For ICI compensation we consider both 3-tap and 5-tap de-ICI filters. It is observed that compared to Rel-15 PTRS configuration, block PTRS designs with similar PTRS overhead does not provide significant performance gains.

[22, LG] compared the performance difference between ideal cases (no PN or ideal filter estimation) and de-ICI and CPE-only compensation based on Rel-15 PTRS for all SCSs with MCS 22 and showed that the potential performance gain by advanced estimation algorithms or by new PT-RS pattern is well bounded (< 1 dB).

[25, Qualcomm] observed that the best BLER performance is obtained with block PTRS pattern with zero-power tones, however, the performance gap with the legacy PTRS pattern is relatively small. The main benefit from block PTRS pattern with ZP tones is to reduce the complexity of the ICI compensation.

Summary of observations on performance:

* Companies’ results showing notable gain of block PTRS with cyclic sequence against Rel-15 PTRS
  + Yes: [1, Huawei], [9, Mitsubishi], [15, Samsung]
  + No: [4, ZTE], [5, vivo], [12, Ericsson]
* Companies’ results showing notable gain of block PTRS against Rel-15 PTRS
  + Yes: [17, Intel]
  + No: [5, vivo], [9, Mitsubishi], [13, Nokia], [21, InterDigital]

Arguments from proponent to support block PTRS and/or block PTRS with cyclic sequence

* Performance gain for some cases (e.g., high MCS, rank 2, 70 GHz)
* Possible complexity reduction for ICI compensation with cyclic sequence
* Better power boosting effect in ICI estimation

Arguments from companies to not to support block PTRS and/or block PTRS with cyclic sequence in Rel-17

* No significant performance gain even with power boosting for PTRS
* Matrix inversion (possible complexity reduction for filter coefficient estimation with cyclic sequence) is a small portion (~2%) of the total complexity for ICI compensation
* Requires extensive discussion on the applicable condition between Rel-15 PTRS and potential alternative PTRS structure, and potential new PTRS structure parameters (sequence, number of blocks, number of PTRS in each block, power boosting factor(s)) and concerns on not able to complete in the limited Rel-17 WI time.

Based on the contributions, companies’ view to support block PTRS with cyclic sequence are summarized below.

Yes: [1, Huawei] (ZC sequence and circular part based on ZC sequence), [9, Mitsubishi] (a sequence of KP samples includes a cyclic prefix of floor(KP/2) samples), [15, Samsung] (no preference indicated for sequence)

No: [4, ZTE], [5, vivo], [10, CATT], [12, Ericsson], [21, InterDigital], [22, LG], [25, Qualcomm],

Based on the contributions, companies’ view to support block PTRS are summarized below.

Yes: [15, Samsung], [17, Intel], [19, CEWiT]

No: [4, ZTE], [5, vivo], [10, CATT], [12, Ericsson], [21, InterDigital], [22, LG], [25, Qualcomm]

Moderator’s comment:

Looking at the available evaluation results and views expressed from contributions, it’s clear that companies have split views on whether there’s performance gain of block PTRS, the sequence of PTRS and in general the benefit/necessity of PTRS enhancement for CP-OFDM.

More evaluation results are submitted to this meeting and more results showed no significant performance gain of the potential enhancement. Given there has not been a shift in company positions to form a clear majority for any of the proposed schemes, moderator don’t see a chance for an agreement on any of the proposed scheme yet.

Since majority companies prefer not to support block PTRS and/or block PTRS with cyclic sequence in Rel-17, moderator suggest conclude and close the discussion point in this meeting considering limited time of this WI.

##### Conclusion 2-1 (high priority)

* In Rel-17, for NR operation with 480 kHz and/or 960 kHz SCS, block based PTRS pattern is not supported for CP-OFDM.

Companies are encouraged to provide comments and/or potential agreeable proposal if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We **support the conclusion** |
| Qualcomm | We support the conclusion, it will be hard to converge to a single block based PTRS pattern given the different view of the companies and the different observations about which pattern provides the best performance. |
| Intel | As we agreed at RAN1#104-e “the decision to support potential enhanced PTRS design in addition to existing PTRS design will be made based on performance benefit, receiver complexity and specification effort aspects of enhanced PTRS design together and not purely on the considerations of the specification effort caused by supporting potential enhanced PTRS design in addition to existing PTRS design”.  From our view, it’s unfortunate that some companies do not recognize the performance benefit of block based PTRS with general ICI filter approximation approach and PTRS block size ~40.  Although we still do claim that block based PTRS with proper block size and receiver algorithm provides the performance benefit over Rel-15 PTRS pattern, we can agree that in combination with the limited WI time left, the standardization effort can be considered too high to proceed with the discussion. |
| vivo | Considering the performance gain over legacy pattern is not obvious, and the limited time for this WI, we agree with this conclusion. |
| LG Electronics | Agree the Moderator’s suggestion and Conclusion 2-1 |
| Apple | We are fine with the conclusion |
| CATT | Support the proposal. |
| InterDigital | We support the conclusion. |
| Samsung | We understand the current situation on block PTRS and it is important to make a conclusion in this meeting. For the sake of progress, we can accept the conclusion. |
| Futurewei | We think that without a new PTRS sequence adopted, block PTRS does not lead to notable performance gain. |
| ZTE, Sanechips | We are OK with the conclusion. |
| Ericsson | Agree with conclusion 2-1.  Extensive evaluation results in a wide range of scenarios have shown no significant gain of block-based PTRS and often a loss compared to Rel-15 PTRS. We also have not seen a viable solution for resolving collision of block PTRS and CSI-RS for tracking (TRS) given that the frequency domain density is 3 for TRS (comb structure with 3 REs per PRB). How will block PTRS coexist with TRS? The specification work must also not be underestimated. So far, there is not convergence on the exact PTRS sequence design, the supported number of PTRS clusters, the supported number of PTRS per cluster, power boosting factors, RB thresholds for different PTRS densities, MCS thresholds for different PTRS densities. In our view, this cannot be completed with 1 remaining meeting. |
| NTT DOCOMO | We support the Conclusion 2-1 considering the gain kindly shown by companies’ evaluation. |
| CEWiT | We agree with the Intel’s view.  We still claim that, there is performance benefit of block based PTRS over Rel-15 PTRS pattern but as we have limited time for this WI, we agree with this conclusion. |
| Huawei, HiSilicon | If RAN1 is going to take this conclusion then it should be clear that it applies also to ZP-tone PTRS. However we have to repeat that we have seen gains for block PTRS with circular sequences, arguably only for certain combinations of SCS, MCS and BW and the consequence of not enhancing PTRS will be that certain combinations of {SCS, MCS, BW} will eventually not be supported in practice in FR2-2. |
| Mitsubishi | The results provided by different companies let us now identify the scenarios where block PTRS brings performance gain and which are the proper combinations of pattern/receiver algorithm that work best, and sufficient gain has been pointed out by different sources. The decision was supposed to be made based on:   * Performance benefit, which was proven to be there in a number of scenarios * receiver complexity, which is lower than for the legacy pattern * spec effort, which is pointed out to be quite limited   It is unfortunate to see that the group goes against the previous agreement and privileges the potential spec effort over all other considerations. The current conclusion is clearly not my preference, but if we do have to go that way, the correct wording should be that **no PTRS enhancements are supported in Rel.17 for CP-OFDM**, there is no reason to target block PTRS specifically and leave the door open for other enhancements. The direct outcome is that there will be a number of MCS that will not work in practice, especially at 70GHz, and we will have to live with that. |

##### Discussion point 2-2

[17, Intel] observed that de-ICI filtering performance could be improved via several receiver implementation based PN compensation methods. It then evaluated performance of high MCS for rank 1 and rank 2 using existing PTRS with direct de-ICI filter estimation. It observed that the maximal supported MCSs are as follows: SCS120kHz, rank 1 – MCS27 (high complexity), MCS26 (medium complexity), SCS120kHz, rank 2 – MCS21, SCS960kHz, rank 1 – MCS27, SCS960kHz, rank 2 – MSC25. [17, Intel] proposed to introduce UE capability of supporting certain high MCS/rank combinations in FR2-2.

Moderator’s comment:

It is moderator’s understanding that this issue is in the scope of UE feature agenda item and hence suggest companies discuss over there.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Intel | Yes, we have raised the issues in 8.17.2. Given that it is being discussed in 8.17.2 we are ok with not discussing in this agenda. |
| LG Electronics | Agree the Moderator’s assessment that this is in the scope of UE feature AI. |
| InterDigital | We agree with the moderator’s comment. |
| Samsung | We agree with FL’s assessment. |
| ZTE, Sanechips | We agree with the moderator’s suggestion. |
| Ericsson | Agree with FL's assessment |
| CEWiT | We agree with the moderator’s comment. |
| Huawei, HiSilicon | If this approach is to be pursued (even in UE capability discussion), should RAN1 agree on the set of {SCS, MCS, rank} that UEs are not expected to support, or should it be left to UE capability to signal which sets of {SCS, MCS, rank} a UE may not support? In the first case, some additional evaluations are needed. In the second case, without any restriction, the performance of UEs in FR2-2 may vary widely depending on implementations. In the second case, should RAN4 define performance requirements for all sets of {SCS, MCS, rank}? Or could it simply be left to RAN4 to determine which sets of {SCS, MCS, rank} will not have performance requirements defined? |

#### For small RB allocation with CP-OFDM

In RAN1#104b-e meeting, the following was agreed.

* In Rel-17, for NR operation in 52.6 – 71 GHz, conclude that increased PTRS frequency density is not supported for CP-OFDM at least for Rel-15 PTRS pattern when the allocated number of RB > 32
* Companies are encouraged to study whether to increase PTRS frequency density for small RB allocations for CP-OFDM for NR operation in 52.6 to 71 GHz with respect to phase noise compensation performance
  + CPE and ICI PN compensation
    - Note: Results for CPE compensation-only are to be reported for reference
  + (K = 0.5, L = 1), (K = 1, L = 1), (K = 2, L = 1),
    - Note: PTRS per K number of PRBs, and PTRS every L number of OFDM symbols
  + Number of RBs: 8, 16, 32
  + Other values of K and number of RBs are not precluded
* Study on other aspects of potential PTRS enhancement (e.g., decreased PTRS frequency density) is not precluded

In RAN1#106-e, the following was agreed.

Agreement:

Further study and conclude on whether to introduce K=1 for Rel-15 PTRS pattern for CP-OFDM with small (< =32) RB allocation by RAN1#106b.

On this subject, the following contributions submitted to this meeting evaluated and compared different frequency density of Rel-15 PTRS pattern with different PN compensation schemes for small RB allocation.

[1, Huawei] evaluated for 120 kHz with MCS 22 for 8, 16 and 32 RB. It observed no performance gain for K=0.5 or K=1 and thought it’s unnecessary to increase the frequency density of PTRS, at least for MCS22 of rank1.

[2, Futurewei] proposed to support (K=1, L=1) for small RB allocation considering performance gain and little standard effort.

[4, ZTE] compared the performance of different PTRS density (K=0.5, 1 and 2) with de-ICI and CPE only PN compensation methods for small RB allocations. It observed when PRB number is not larger than 32, CPE compensation with lower PTRS density can achieve similar or better performance than ICI compensation with higher PTRS density.

[5, vivo] evaluated and compared the performance of different PTRS density (K=0.5, 1 and 2) with de-ICI (3 taps) and CPE only PN compensation methods with different number of PDSCH RB allocation and different MCS for all SCSs. It observed that while increased PTRS density (K = 0.5 or 1) may help improve the performance of de-ICI compared to K =2 when PDSCH RB number <= 16, a better performance is obtained for CPE only with K = 2 in this case. Given de-ICI with increased density (K = 0.5 or 1) is not the PN compensation method providing the best performance in any of the evaluated cases, it proposed not to increase PTRS density.

[12, Ericsson] provided evaluation results on increased PTRS density for small RB allocation. It is observed that even for small RB allocation, enhanced PTRS structure with K = 1 or K=0.5 does not provide additional performance gain over the existing Rel-15 PTRS structure (K = 2 and K=4).

[13, Nokia] evaluated different PTRS density for small RB allocation. It observed benefit from increasing PTRS density to K=1 only in a single case when high-order modulation is used and PRBs=16 and ICI compensation is used. It observed no gain is achieved using K=0.5. Further, it argued that using small PRB allocations with high MCSs is a corner case and should not be considered to motivate new PTRS configurations.

[15, Samsung] compared the performance of different PTRS density (K=1, 2 and 4) with de-ICI (3 taps) and CPE only PN compensation for 120 kHz SCS with MCS 22. It observed that for small RB allocations (32RB/16RB/8RB) and legacy PTRS frequency density (K=2 and K=4), CPE compensation outperforms the one with ICI compensation. It also observed that for 16 RBs and 8RBs allocations, K=1 configuration provides better performance for CPE compensation (for 10% BLER target, 1.5 dB gain reported at 8 RB and 2.1 dB gain reported at 16 RB) compared with legacy PTRS frequency density (K =2 and 4).

[22, LG] compared the performance for different PTRS densities for small RB allocation. It observed that the increase of PTRS density for the case of small RB allocations, e.g., 8 RBs, does not provide enough performance gain for 3 tap de-ICI filtering. In addition, for CPE-only compensation, increasing the PTRS density does not provide any significant improvement.

[23, Apple] compared the performance for different PTRS densities for 480 kHz SCS with MCS 22 and 16 RB. It is observed there is an improvement in BLER performance with increased PTRS density while K = 1 has the highest spectral efficiency compared with K = 0.5 and K = 2 at low SNR. The performance gain of K=1 is > 1dB (moderator’s reading from Figure 2 in [23]) for 10% BLER target and <0.5 dB (moderator’s reading from Figure 3 in [23]) for spectral efficiency.

[25, Qualcomm] evaluated PN compensation performance for 120 kHz SCS at MCS 22 and MCS 24 with multiple PTRS densities. It observed that for small RB allocation, i.e., 16 or 8 RBs, K=1 enhances the performance while the performance degrades for K=0.5. The performance gain of K=1 for 10% BLER target was reported as 0.5 dB for 8 RB with MCS 22, 0.2 dB for 16 RB with MCS 24 and 0.4 dB for 16 RB with MCS 24. The performance gain of K=1 for 1% BLER target was reported as 4.5 dB for 8 RB with MCS 22, 2.9 dB for 8 RB with MCS 24, 0.6~0.7 dB for 16 RB with MCS 22 and MCS 24.

Companies’ results showing significant performance gain of increased PTRS density (i.e., K=1) for small RB (<=32) allocation are summarized below.

Yes: [2, Futurewei], [15, Samsung], [23, Apple], [25, Qualcomm]

No: [1, Huawei], [4, ZTE], [5, vivo], [12, Ericsson], [13, Nokia], [22, LG]

Companies’ view to support increased PTRS density (K=1) for small (<= 32) RB allocation are summarized below.

Yes: [2, Futurewei], [15, Samsung], [23, Apple], [25, Qualcomm]

No: [1, Huawei], [4, ZTE], [5, vivo], [10, CATT], [12, Ericsson], [13, Nokia], [22, LG]

Moderator’s comment:

Looking at the available evaluation results from contributions, the performance gain of K=1 are shown for some cases (e.g., small RB (<=32) allocation with high order modulation) by some sources while other sources showed no performance gain at all for those cases. Companies still have split views on whether there’s performance gain of increased PTRS density (K=1) for small RB allocation and hence no consensus to support K=1.

Since more companies prefer not to increase PTRS density for small RB allocation, moderator suggest conclude and close the discussion point by extending the conclusion agreed in RAN1#104b-e to cover small RB allocation.

##### Conclusion 2-3 (high priority)

In Rel-17, for NR operation in FR2-2, increased PTRS frequency density for Rel-15 PTRS pattern is not supported for CP-OFDM when the allocated number of RB <= 32.

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We **support the conclusion** |
| Qualcomm | We see performance benefit with higher density PTRS for small allocations for some cases. The benefit is more substantial than the proposals in proposal 2-4. If we don’t consider this enhancement, we should not consider 2-4 as well |
| Intel | We support adopting K=1. |
| vivo | We support the conclusion as the performance of ‘CPE only’ with K = 2 can achieve good performance for RB<=32. |
| LG Electronics | Agree the Moderator’s suggestion and Conclusion 2-3 |
| Nokia/NSB | Agree with the moderator’s proposal |
| Apple | We do see benefit in supporting K = 1 |
| CATT | Support the proposal. |
| InterDigital | Agree with the moderator’s proposal |
| Samsung | Same comments in Conclusion 2-1. For the sake of progress, we can accept the proposal. |
| Futurewei | We see for several cases the higher density PTRS provides certain performance gain. |
| ZTE, Sanechips | Fine with the proposal. |
| Ericsson | Agree with Conclusion 2-3  We have not found any gain with increased PTRS density for Rel-15 PTRS for small allocations. |
| NTT DOCOMO | We support the Conclusion 2-3. |
| CEWiT | Fine with the proposal. |
| Huawei, HiSilicon | Agree with conclusion 2-3, according to the observations from our evaluations. |
| Mitsubishi | Fine with the proposal. |

#### For DFT-s-OFDM

In RAN1#106-e meeting, the following was agreed.

Agreement:

Further study and conclude on whether to introduce (Ng = 16, Ns = 2, L = 1) and/or (Ng = 16, Ns = 4, L = 1) for DFT-s-OFDM by RAN1#106b.

* Note: Ng number of PT-RS groups, Ns number of samples per PT-RS group, and PTRS every L number of DFT-s-OFDM symbols
* FFS applicable to which RB allocation(s) if agreed to introduce (Ng = 16, Ns = 2, L = 1) and/or (Ng = 16, Ns = 4, L = 1)

The following contributions submitted to this meeting evaluated and studied on the need of potential PTRS enhancement for DFT-s-OFDM.

[1, Huawei] evaluated a new PTRS pattern with more PTRS groups within one DFT-s-OFDM symbol. It is observed that BLER performance of high MCS (e.g, MCS 22 and MCS 26) with large scheduled bandwidth can be improved by using a new pattern with more PTRS groups within one DFT-s-OFDM symbol. It observed that PTRS patterns with more PTRS groups improve the BLER performance significantly for MCS22 of all SCSs, while they perform almost the same as (, ) = (8, 4) for MCS16. It also noted that the BLER can be less than 0.01 only with PTRS pattern (, ) = (16, 2) for MCS26.

[2, Futurewei] observed that for each SCS with 64QAM, the PTRS density (Ng = 16, Ns = 4, L = 1) offers better performance than the legacy density, although the gain is more notable for the smaller SCS. It then proposed to consider increasing PTRS density to (Ng = 16, Ns = 4, L = 1) for PUSCH in FR2-2 if 64QAM is used; for lower order modulations such as 16QAM and QPSK, the legacy density (Ng = 8, Ns = 4, L = 1) offers fine performance, thus can be reused. For smaller RB allocations, the legacy density performs well under different modulations and no enhancement is necessary.

[4, ZTE] evaluated DFT-s-OFDM PUSCH performance of 120 kHz with 64QAM and showed a gain (~0.5 dB for 10% BLER target and ~2 dB for 1% BLER target) at MCS 22 with TDL-A 10 ns.

[5, vivo] compared PUSCH performance of DFT-s-OFDM with different PTRS configurations for 120 kHz SCS. It is observed that for MCS-7, MCS-16 and MCS 22, the performance gain of increasing PTRS chunk number is small (<0.8 dB). The gain is more noticeable for MCS 26 and with large RB allocation (e.g 256). However, a question on the motivation of PTRS enhancement for DFT-s-OFDM is raised in [5, vivo] when it is observed that DFT-s-OFDM is mainly used for UL coverage, it is unlikely that very high MCS, such as MCS 26, is typically used with DFT-s-OFDM.

[12, Ericsson] evaluated the case of 120 kHz SCS, 256 PRBs, and MCS22 for TDL-A channel with 10 ns delay spread. It observed that the BLER performance using the existing Rel-15 PTRS pattern (Ng=8, Ns=4) is on par with the new alternative PTRS pattern (Ng=16, Ns=2). The BLER performance using the new PTRS pattern with increased density (Ng=16, Ns=4) is worse than existing Rel-15 PTRS pattern (Ng=8, Ns=4).

[13, Nokia] evaluated PUSCH performance of DFT-s-OFDM with different PTRS configurations and showed performance improvement of 64QAM with 120 kHz SCS by two different approaches: introducing a PTRS mapping unit in terms of fraction or multiple of DFT-s-OFDM symbols. It proposed increasing number of PTRS groups for DFT-s-OFDM to make high order modulations robust to phase noise when a large number of PRBs is used. It further proposed increasing the number of PTRS groups to 16 by introducing a PTRS mapping unit in terms of fraction (or multiple of) DFTsOFDM symbols, to flexibly control PTRS overhead and allocation.

[17, Intel] evaluated PUSCH performance of DFT-s-OFDM with different PTRS configurations and showed that PUSCH PTRS patterns with only 4 and 8 PTRS groups provide acceptable performance with 120kHz SCS. It also compared two PT-RS patterns with 16 PT-RS groups and observed that (16,2) pattern has better performance for the wider range of the possible allocations.

[22, LG] observed that (Ng=16, Ns=2) or (Ng=16, Ns=4) configurations may provide about 1 dB improvement for MCS 22 and even make this mode feasible for the case of MCS 27. For SCS 960 kHz, these new configurations provide improvement only for higher code-rate scenario, e.g., MCS 27. It also noted that (Ng=16, Ns=2) is almost always better than (Ng=16, Ns=4).

[23, Apple] evaluated the effect of the PTRS parameters on DFT-S-OFDM performance for a 10 nses delay spread channel for 120 kHz and 480 kHz SCSs with a 400 MHz BW. It observed that gains over the baseline are made with Ng = 16, Ns = 2, L = 1 only and only at high SNRs.

[25, Qualcomm] compared PUSCH performance of DFT-s-OFDM with different number of PTRS samples for 120 kHz SCS. It observed that for small RB allocation such as 64 RB, the legacy pattern (Ng = 8, Ns = 4, L = 1) is outperforming the other patterns. It also observed that for 128 RB allocation, the gain from the new pattern (Ng = 16, Ns = 4, L = 1) can be observed at the tail of the BLER curve, while for 256 RB allocation, the gain from the new pattern (Ng = 16, Ns = 4, L = 1) can be observed at both 10% and 1% BLER points (~0.8 dB). In general, it observed that the performances of the legacy pattern (Ng = 8, Ns = 4, L = 1) and the new pattern (Ng = 16, Ns = 2, L = 1) are very close to each other for larger RB allocations 128 and 256 RBs.

Companies’ results showing notable performance gain of new PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled with high MCS are summarized below.

Yes: [1, Huawei], [2, Futurewei], [4, ZTE], [5, vivo], [13, Nokia], [22, LG], [23, Apple]

No: [12, Ericsson], [25, Qualcomm]

Companies’ view to support new PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled are summarized below.

* support (Ng = 16, Ns = 2, L = 1): [1, Huawei], [17, Intel], [22, LG] (if the necessity of using high MCS in DFT-s-OFDM transmission is identified), [23, Apple] (only if need for high MCS for DFT-S-OFDM can be justified)
* support (Ng = 16, Ns = 4, L = 1): [2, Futurewei] (for 64QAM), [5, vivo] (if the motivation of using high MCS in DFT-s-OFDM transmission is identified)
* support Ng = 16: [4, ZTE], [9, Mitsubishi], [13, Nokia]
* NO: [10, CATT], [12, Ericsson], [19, CEWiT], [21, InterDigital], [25, Qualcomm]

Moderator’s comment:

Majority of evaluation results showed some performance gain for large RB allocation and high order MCS. Six companies support to consider PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol. Five companies do not see the need. Three companies are okay to consider if the need for high MCS for DFT-S-OFDM can be justified. In terms of which configuration as the enhancement, companies’ preferences are also split.

On this PTRS enhancement for DFT-s-OFDM, suggest the following for discussion.

##### Proposal 2-4 (high priority)

For NR operation in FR2-2 with DFT-s-OFDM, select one of the following options in RAN1#106b-e.

* Option 1: support (Ng = 16, Ns = 2, L = 1)
* Option 2: support (Ng = 16, Ns = 4, L = 1)
* Option 3: support (Ng = 16, Ns = 2, L = 1) and (Ng = 16, Ns = 4, L = 1)
* Option 4: no new PTRS configuration for DFT-s-OFDM is supported in Rel-17
* Note: Ng number of PT-RS groups, Ns number of samples per PT-RS group, and PTRS every L number of DFT-s-OFDM symbols

Companies are encouraged to provide comments and/or to indicate preference/objection (if any) to above options.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We prefer to not support any new PTRS configuration for DFT-s-OFDM and **support Option 4** |
| Qualcomm | We support Option 4 |
| Intel | We support Option 1. |
| Vivo | Need proponents of option 1~3 to clarify the reason to support high MCS and high SNR with DFT-s-OFDM waveform. |
| LG Electronics | Prefer Option 4.  For low MCS, we did not find any performance improvement due to an increase in the number of PTRS groups in the evaluation results from companies. For high MCS, the motivation for performance optimization is not clear. |
| Nokia/NSB | Based on the results, we prefer option 2 |
| Apple | Given that we have not seen an justification for DFT-S-OFDM at high MCS and high SNR, we support Option 4. |
| CATT | We support Option 4 |
| InterDigital | We support Option 4: no new PTRS configuration for DFT-s-OFDM is supported in Rel-17. |
| Samsung | We hope all the topics related to PTRS are treated fairly, i.e., if there is no consensus, no enhancement is supported. We support Option 4 as in CP-OFDM case. |
| Futurewei | We support Option 4 or Option 2. |
| ZTE, Sanechips | We support Option 3. As shown in our evaluation results, increasing PTRS groups for DFT-s-OFDM waveform can bring benefit to performance. |
| Ericsson | We support Option 4  From our evaluations, we found that the performance of (16,2) is no better than the existing (8,4) pattern. Furthermore, we found a loss of the (16,4) pattern compared to the existing (8,4) pattern. This is because the gain of improved phase noise mitigation with larger overhead does not make up for the loss in coding gain due to larger overhead.  Furthermore, we don't think there is a need to optimize the PTRS pattern for supporting high MCS, since DFT-s-OFDM is intended for coverage scenarios. |
| NTT DOCOMO | We prefer Option 4. |
| CEWiT | We support Option 4 |
| Huawei, HiSilicon | Option 1: support (Ng = 16, Ns = 2, L = 1)  Option 3 is also acceptable, with the understanding that the applicable sets of {BW, MCS} will have to be defined separately for (Ng = 16, Ns = 2, L = 1) and (Ng = 16, Ns = 4, L = 1). |
| Mitsubishi | To avoid further controversy/need for simulations/lengthy discussion on the chunk placement for Ns=4, we have a slight preference for Option 1. Option 4 is the default fallback solution if no consensus on the enhanced pattern. |

[1, Huawei] also brought up another issue of PTRS group placement for PTRS with It observed that due to Rx timing shift, (part of) a PTRS group placed at the tail of the transmitter’s DFT-s-OFDM symbol, may wrap-around to the head of the symbol from the receiver’s perspective, thus deteriorating PN compensation performance. It then proposed for PTRS with , the mapping of last PTRS group should consider potential Rx timing shift and avoid the last X pre-DFT symbol(s). In particular, it proposed that new PTRS location which is in the middle of each interval with same overhead whose last PTRS group won’t be mapped at the tail of the symbol should be supported to solve the influence induced by Rx advance shift especially for high MCS which is larger than MCS22.

[17, Intel] also investigated RX timing shift robust PTRS patterns. It evaluated two PN compensation methods: timing shift aware PN compensation (a circular interpolation process with an arbitrary point of discontinuity) and timing shift agnostic PN compensation (an interpolation process with the fixed point of discontinuity). Two PTRS patterns: edge-aligned (as in NR) and center-aligned are evaluated. It observed that center-aligned patterns have the competing advantage with both possible timing-related types of PN-compensation. It proposed to adopt the center-aligned version of (8,4) pattern and, in case (16,2) pattern will be agreed, adopt it in center-aligned form as well.

Moderator’s comment:

Two companies raised the same issue and made similar proposal. Performance gain for very high MCS (e.g., MCS 25, 26 or 27) is shown with DFT-s-OFDM using centered PTRS group placement when some notable RX timing shift is assumed. There’s no input from other companies on this matter. Formulate the following proposal for discussion. Suggest proponent to clarify whether the wording of proposal is accurate and other companies to provide input.

##### Proposal 2-5

For NR operation in FR2-2 with DFT-s-OFDM, support new PTRS location which is in the middle of each interval with same overhead whose last PTRS group won’t be mapped at the tail of the symbol.

* At least for (Ng = 8, Ns = 4)
* Note: Ng number of PT-RS groups, Ns number of samples per PT-RS group

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | Such pattern was considered in Rel.15 and not adopted. We don’t think it is necessary to consider it now given the performance benefit over legacy Rel.15 pattern is not substantial. |
| LG Electronics | We share the same view with Qualcomm. |
| Nokia/NSB | This issue might provide performance degradation only when high MCS is used. Provided that new PTRS pattern with higher PTRS density is to be added, this will not be an issue anymore, and thus this does not need to be considered. |
| InterDigital | We share same view with Qualcomm, LG, and Nokia. |
| Samsung | This topic was not investigated and interested by many companies, which implies it’s not essentially needed, and should be deprioritized. |
| Futurewei | Ok with the proposal. |
| ZTE, Sanechips | There is no need to consider this topic. |
| Ericsson | We share the same view as Qualcomm and LGE. Furthermore, if the intention is that this could provide some gain at large MCS, it is not clear that this is a valid scenario given that DFT-s-OFDM is typically used for coverage scenarios. |
| Intel | In our view, Rel-15 evaluations relevance is limited because of the lower carrier frequencies used. The evaluations at 60GHz carrier frequency [1][17] show >5dB gain over the legacy pattern when 10% CP timing shift is considered with high MCS.  What is different from Rel-15 is the effect of residual timing misalignment and its impact to phase noise estimation. For Rel-15 the small differences (below TA granularity) did not impact phase noise estimation much for the gNB. However, for 480/960kHz this effect is amplified much more. |
| CEWiT | We share the same view as Qualcomm. |
| Huawei, HiSilicon | By placing the PTRS in the middle of each interval, we can avoid mapping the last PTRS group to the last few samples of the pre-DFT symbol, and thus avoid impact from RX timing shift, which is more severe at 60/70 GHz than what was previously concluded in Rel-15 up even before extending FR2 to 52.6 GHz. With this clarification, the wording of the proposal can be simplified as proposed below:  For NR operation in FR2-2 with DFT-s-OFDM, support new PTRS location in the middle of each interval, with same overhead as legacy PTRS, at least for (Ng = 8, Ns = 4).  Note: Ng number of PT-RS groups, Ns number of samples per PT-RS group |
| Mitsubishi | Unsure about the need of this optimization for the same reasons as expressed by different companies. We should concentrate on whether to support a new 16 chunks pattern as a first priority. |

##### Discussion point 2-6

One contribution mentioned an issues related to PTRS for DFT-s-OFDM.

It is observed in [17, Intel] that due to code block concatenation, unequal distribution of PN estimation error among DFT-s-ODFM samples may lead to systematic unbalance between code blocks’ BLERs. It also showed performance gain from 0.5dB to 1.7dB for code block interlacing within a DFT-s-OFDM symbol at MCS22. It then proposed to consider code block interlacing for PUSCH with transform precoding.

Moderator’s comment:

The same proposal has been made in RAN1#106-e where many companies (other than the proponent) proposed to either de-prioritize or conclude not to consider it during Rel-17 due to concerns on the specification efforts for code block interleaving and considerations of current progress on PTRS itself with limited time for the WI.

Unless there’s a change of company views on this topic in this meeting, moderator’s suggestion is to de-prioritize this discussion.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We believe that this proposal is more related to rate-matching not PTRS enhancements and will require a lot of spec. changes, so we do not support it. |
| Intel | Even though the proposal is not a PTRS enhancement, it substantially improves PN compensation for high MCS and can reduce the need for the dense PTRS pattern (Ng=16) introduction. However, as we don’t see the interest from the companies, we are fine to de-prioritize in order not to repeat the discussion happened at RAN1#106-e. |
| vivo | Agree to de-prioritize this discussion. |
| Nokia/NSB | Agree with the moderator’s suggestion. |
| InterDigital | We agree with the moderator’s suggestion. |
| Samsung | We understand the intention of this proposal but this is out of scope in WI. |
| Futurewei | Ok to de-prioritize this issue. |
| ZTE, Sanechips | We agree with the moderator’s suggestion. |
| Ericsson | Agree to de-prioritize |
| CEWiT | Agree to de-prioritize this discussion. |

## 2.3. DMRS

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | Observation 5: For 480 kHz and 960 kHz, bundling DMRS in one slot per multi-slot outperforms the legacy DMRS pattern mapped per slot.  Proposal 13: Support DMRS mapped on symbol l0 to symbol l0+S\*L-1 within the first PDSCH slot for the multi-slot scheduling, when only front-loaded DMRS is configured, where L is the length and l0 the starting symbol of legacy front-loaded DMRS.  Proposal 14: For 960 kHz SCS, support an RRC configuration of DMRS where the UE is able to assume that FD-OCC is not applied for rank 1 PDSCH with DMRS type-2 in addition to DMRS type-1.   * + FFS: whether applies to 480 kHz. |
| [4, ZTE] | Proposal 14: Support to use the reserved bit of antenna port(s) field in DCI to indicate whether FD-OCC is applied for DMRS Type-1.  Proposal 15: The DMRS configuration to disable FD-OCC is not applied to DMRS type-2.  Proposal 16: If RRC configuration option is selected to indicate FD-OCC off, the corresponding RRC parameter may need to be defined. |
| [5, vivo] | Observation 7: ‘Type-2 no FD-OCC’ has better performance than ‘Type-2 with FD-OCC’ by 1~4 dB, and the gain on SCS-960KHz is higher than the gain on SCS-480KHz.  Proposal 4: For FR2-2, support ‘type-2 no FD-OCC’ for SCS of 480/960 kHz in Rel-17.  Proposal 5: For 480/960 kHz SCS in FR2-2, for rank 1 PDSCH, FD-CDM invalidation should be indicated by RRC ignaling where one new field to indicate a set of values, and only when antenna port(s) field in DCI belongs to this set, UE can assume no FD-CDM from other UE. |
| [10, CATT] | Proposal 15: Additional DMRS enhancement for multi-PDSCH/PUSCH scheduling is not supported.  Proposal 16: The reserved states in the “Antenna port(s)” field can be used to indicate the FD-OCC off state for rank-1. |
| [12, Ericsson] | Proposal 29 Do not support enhancement of DMRS Type-2.  Proposal 30 Support an RRC parameter to indicate that for DMRS Type-1 for a rank-1 PDSCH transmission with 480/960 kHz SCS, the UE can assume that the set of remaining orthogonal antenna ports in a CDM group corresponding to a different FD-OCC are not allocated to another UE. |
| [13, Nokia] | Proposal 17: Support the configuration of rank 1 DMRS without FD-OCC for DMRS type-2.  Proposal 18: Support the RRC configuration for the indication of rank 1 without FD-OCC transmission. |
| [15, Samsung] | Proposal 5: Support DMRS overhead reduction in time domain and DMRS bundling across multiple PDSCH/PUSCHs. |
| [17, Intel] | Proposal 21: Indicate to UE that CDM groups, signaled in scheduling DCI, do not contain potential co-scheduled DMRS ports at least for DMRS Type-1 and maxLength=1.  Proposal 22: Use the reserved codepoints from Tables 7.3.1.2.2-1/1A to signal DMRS port(s) without co-scheduled DMRS ports within the same CDM group as given in Table 1 and Table 2.  Table 1. Updated Table 7.3.1.2.2-1 [2]. Modifications are highlighted with red color.   |  |  |  | | --- | --- | --- | | **One Codeword:**  **Codeword 0 enabled,**  **Codeword 1 disabled** | | | | **Value** | **Number of DMRS CDM group(s) without data** | **DMRS port(s)** | | 0 | 1 | 0 | | 1 | 1 | 1 | | 2 | 1 | 0,1 | | 3 | 2 | 0 | | 4 | 2 | 1 | | 5 | 2 | 2 | | 6 | 2 | 3 | | 7 | 2 | 0,1 | | 8 | 2 | 2,3 | | 9 | 2 | 0-2 | | 10 | 2 | 0-3 | | 11 | 2 | 0,2 | | 12 | 1 | 0, no co-scheduled DMRS ports | | 13 | 2 | 0, no co-scheduled DMRS ports | | 14 | 2 | 2, no co-scheduled DMRS ports | | 15 | Reserved | Reserved |   Table 2. Updated Table 7.3.1.2.2-1A [2]. Modifications are highlighted with red color.   |  |  |  | | --- | --- | --- | | **One Codeword:**  **Codeword 0 enabled,**  **Codeword 1 disabled** | | | | **Value** | **Number of DMRS CDM group(s) without data** | **DMRS port(s)** | | 0 | 1 | 0 | | 1 | 1 | 1 | | 2 | 1 | 0,1 | | 3 | 2 | 0 | | 4 | 2 | 1 | | 5 | 2 | 2 | | 6 | 2 | 3 | | 7 | 2 | 0,1 | | 8 | 2 | 2,3 | | 9 | 2 | 0-2 | | 10 | 2 | 0-3 | | 11 | 2 | 0,2 | | 12 | 2 | 0,2,3 | | 13 | 1 | 0, no co-scheduled DMRS ports | | 14 | 2 | 0, no co-scheduled DMRS ports | | 15 | 2 | 2, no co-scheduled DMRS ports | |
| [18, NTT DOCOMO] | Observation 1: The maximum gain of JCE over multi-PDSCH scheduling is about 0.41dB and 0.63dB in SCS of 480kHz and 960kHz, respectively.  Proposal 5: No need to support JCE for multi-PDSCH scheduling due to no significant gain. |
| [20, Lenovo] | Proposal 7: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, it should be agreed to not support FD-OCC for DMRS type 2 as well.  Proposal 8: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, maximum number of orthogonal DMRS ports are reduced as:   * DMRS type 1:   + 1-symbol: No FD-OCC, maximum # of DMRS ports is 2   + 2-symbol: No FD-OCC, maximum # of DMRS ports is 4 * DMRS type 2:   + 1-symbol: No FD-OCC, maximum # of DMRS ports is 3   + 2-symbol: No FD-OCC, maximum # of DMRS ports is 6 |
| [17, InterDigital] | Observation 1: Antenna port(s) indication based indication method provides dynamic switching between with FD-OCC and without FD-OCC, however, benefits are doubted considering narrow beams and coverage decrease due to the increased DCI payload.  Observation 2: RRC based configuration method provides a simplest solution without DL coverage decrease.  Proposal 1: Support RRC based configuration for rank 1 PDSCH transmission without FD-OCC. |
| [22, LG] | Proposal #23: If antenna port(s) field in a DCI scheduling PDSCH is agreed to indicate whether FD-OCC is turned on or off, reserved rows in antenna port(s) field are used to indicate FD-OCC is turned off. FFS: if reserved rows lack to indicate FD-OCC off.  Proposal #24: If RRC configuration is agreed to indicate whether FD-OCC is turned on or off, consider to additionally configure a MCS threshold so that UE can recognize FD-OCC is turned off only if indicated MCS level is no less than the MCS threshold. |
| [23, Apple] | Proposal 6: To account for transmission with large SCSs in low coherence BW channels,   * dynamically turn on or off the FD-OCC based on the scenario the channel is in * for 480 kHz and/or 960 kHz SCS, we support a configuration of the DMRS, indicated by the antenna port(s) field in the scheduling DCI, where the UE is able to assume that FD-OCC is not applied * This should be applicable to DMRS type-1 and DMRS type-2.   Proposal 7: Deprioritize the study of DMRS bundling and DMRS overhead reduction for Rel-17 NR above 52.6 GHz operation. |
| [25, Qualcomm] | Proposal 4: For DMRS enhancements, we support   * Using antenna port(s) field in DCI scheduling the rank 1 PDSCH to indicate to the UE whether FD-OCC is ON/OFF * Applying the same behavior for DMRS type-2 |

### Summary on DMRS

#### FD-OCC

The following was agreed in RAN1#106-e meeting.

Agreement:

* For 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH at least with DMRS type-1, support a configuration of DMRS where the UE is able to assume that FD-OCC is not applied.
  + Note: “FD-OCC is not applied” refers to the UE may assume that a set of remaining orthogonal antenna ports are not associated with the PDSCH to another UE, wherein the set of remaining orthogonal antenna ports are within the same CDM group and have different FD-OCC
  + FFS whether applies to DMRS type-2
  + Down select between the following options for the indication to UE
    - RRC configuration
    - antenna port(s) field in DCI scheduling the rank 1 PDSCH

The following contributions discussed and expressed their views with respect to the remaining issues of FD-OCC.

[1, Huawei] observed that for DMRS type2 the distance between two Res or subcarriers of 960 kHz for FD-OCC is the same as for DMRS type1 of 480 kHz. So [1, Huawei] proposed that FD-OCC disabling could also be applied for DMRS type2 of 960 kHz. For 480 kHz, [1, Huawei] thought FD-OCC off could be applied if the signaling is anyway defined for 960 kHz. [1, Huawei] also proposed that RRC configuration to indicate FD-OCC on/off.

[4, ZTE] support to use the reserved bit of antenna port(s) field in DCI to indicate whether FD-OCC is applied for DMRS Type-1. It also argued that it’s not meaningful to enable FD-OCC off for DMRS type 2 given DMRS type-2 has lower frequency density and is mainly used for more Ues multiplexing.

[5, vivo] compared PDSCH BLER performance of type-1 and type-2 DMRS with and without FD-OCC for 480KHz and 960 KHz SCS with 64QAM. Similar to type-1 DMRS, it observed performance gain of FD-OCC off (> 1 dB) for type-2 DMRS. Therefore, it proposed to support FD-OCC off for type-2 DMRS as well. Regarding UE indication, [5, vivo] compared multiple options of DCI and RRC indication. It observed that reusing the values with ‘reserved’ states in antenna port(s) filed in DCI may not be practical due to no or very limited number of ‘reserved’ states in some case (*dmrs-Type*=1, *maxLength*=2, one codeword). Considering the trade-off between flexibility and overhead, it then proposed that an RRC configuration indicating a set of values, and only when antenna port(s) field in DCI belongs to this set, UE can assume no FD-CDM from other UE.

[10, CATT] proposed that the reserved states in the “Antenna port(s)” field can be used to indicate the FD-OCC off state for rank-1.

[12, Ericsson] proposed to not support FD-OCC off for type-2 DMRS arguing that DMRS type 2 suffers from poor channel estimate interpolation when channel delay spread is large in 480 kHz and 960 kHz SCS and DMRS Type-2 is mainly designed for user multiplexing which is less relevant for NR operation beyond 52.6 GHz. It further observed that there may not be sufficient number of reserved values in all tables to cover all the relevant rank-1 transmission scenarios. In contrast, use of an RRC parameter can apply to all rank-1 transmission scenarios in the existing tables, and is thus most flexible.

Regarding to the applicability to DMRS type-2, [13, Nokia] proposed to extend the agreement in DMRS type-1 into DMRS type-2. Regarding to signaling option for the functionality, [13, Nokia] prefer RRC configuration rather than antenna port field in DCI.

[17, Intel] observed that for DMRS Type-1 and maxLength=2, corresponding Tables 7.3.1.2.2-2/2A have only one and zero reserved codepoints, respectively, which make reusing reserved codepoints not possible. It argued that the configuration of DMRS Type-1 and maxLength=2 is typically used to provide higher order MIMO transmission with up to 8 layers which seems to be not the main usage mode of NR extension from 52.6 GHz up to 71 GHz where the most usual MIMO scheme assumes up to 2 layers. [17, Intel] also argued that for DMRS Type-2, the issue with channel selectivity and OCC de-spreading is less pronounced because the DMRS Res within the same OCC are close to each other and are not separated by another RE as in DMRS Type-1 where comb-2 pattern is used. [17, Intel] proposed indicating to UE that CDM groups, signaled in scheduling DCI with the reserved codepoints, do not contain potential co-scheduled DMRS ports at least for DMRS Type-1 and maxLength=1.

[20, Lenovo] argued that the same performance issues are prevalent for DMRS type 2 and therefore turning off FD-OCC should be agreed for DMRS type 2 as well. Furthermore, it proposed to limit the maximum number of DMRS ports.

[21, InterDigital] observed that the benefits of antenna port(s) indication based indication method are doubted considering narrow beams and coverage decrease due to the increased DCI payload. It also observed that RRC based configuration method provides a simplest solution without DL coverage decrease and hence proposed to support RRC based configuration.

[22, LG] proposed to use reserved states to indicate FD-OCC off if antenna port(s) field in a DCI scheduling PDSCH is agreed to indicate whether FD-OCC is turned on or off. It also identified the issue of lack of reserved states in some cases. [22, LG] also proposed to additionally configure a MCS threshold so that UE can recognize FD-OCC is turned off only if indicated MCS level is no less than the MCS threshold if RRC configuration is agreed to indicate whether FD-OCC is turned on or off.

Both [23, Apple] and [25, Qualcomm] proposed to use antenna port(s) field in DCI scheduling the rank 1 PDSCH to indicate to the UE whether FD-OCC is ON/OFF. Both of them also support applying FD-OCC off for type-2 DMRS.

Companies views on whether to support FD-OCC off for type-2 DMRS are summarized below.

No: [4, ZTE], [12, Ericsson], [17, Intel]

Yes: [1, Huawei] (at least for 960 kHz SCS), [5, vivo], [13, Nokia], [20, Lenovo], [23, Apple], [25, Qualcomm]

Moderator’s comment:

Regarding whether apply FD-OCC off to DMRS type-2, the opposing arguments from companies are:

* for DMRS Type-2, the issue with channel selectivity and OCC de-spreading is less pronounced;
* DMRS Type-2 is mainly designed for user multiplexing which is less relevant for NR operation beyond 52.6 GHz.

Counter arguments are provided from proposing companies where significant performance gain of disabling FD-OCC for DMRS type-2 was shown. From specification development point of view, there’s little extra effort if the same UE signaling for type-1 DMRS is used for type-2 DMRS. It also seems no need for the specification to restrict the usage of type-2 DMRS in this deployment scenario. Given majority of companies want to extend FD-OCC off to type-2 DMRS in addition to type-1 DMRS, formulate the following proposal.

##### Proposal 3-1 (high priority)

* For 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH with type-1 or type-2 DMRS, support a configuration of DMRS where the UE is able to assume that FD-OCC is not applied.
  + Note: “FD-OCC is not applied” refers to the UE may assume that a set of remaining orthogonal antenna ports are not associated with the PDSCH to another UE, wherein the set of remaining orthogonal antenna ports are within the same CDM group and have different FD-OCC
  + Note: the same UE indication method is used for both type-1 and type-2 DMRS

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We **support the proposal** |
| Qualcomm | We support the proposal |
| Intel | We support Proposal 3-1 |
| vivo | We support the proposal. |
| LG Electronics | If the performance degradation due to FD-OCC in using DMRS Type-2 is observed, we think that the FD-OCC off function is needed for Type-2 as well. There seems to be no reason that a function applied to Type-1 cannot be applied to Type-2 unless there is a critical issue in using Type-2 for NR beyond 52.6 GHz. |
| Nokia/NSB | Support the proposal. |
| Apple | Support the proposal |
| CATT | Ok |
| InterDigital | We are fine with the proposal |
| Futurewei | We support Proposal 3-1. |
| ZTE, Sanechips | We think the FD-OCC off for DMRS type1 is enough for 52.6G~71GHz. DMRS type-2 has lower frequency density and is mainly used for more UEs multiplexing. But for the sake of progress, we are ok to compromise. |
| Ericsson | We support the proposal for DMRS Type-1  For DMRS Type-2 since the REs of the same CDM group are spaced further apart in frequency compared to Type-1, DMRS Type-2 suffers from worse channel estimate interpolation when the subcarrier spacing is large (480/960 kHz). Hence, we think that DMRS Type-2 is not well suited to operation beyond 52.6 GHz. Furthermore, DMRS Type-2 is designed for larger user multiplexing which is also less relevant for operation beyond 52.6 GHz.  That being said, if the majority really wants the same mechanism for Type-2 we can live with it, but only if RRC is used as the indication method. Otherwise, we will not have time to finish given the large number of port combinations in the DMRS port configuration tables. |
| NTT DOCOMO | We support the Proposal 3-1. |
| Huawei, HiSilicon | Support proposal 3-1 |

Companies’ views on how to indicate FD-OCC off to UE are summarized below.

Antenna port(s) field in DCI: [4, ZTE], [10, CATT], [17, Intel], [23, Apple], [25, Qualcomm]

RRC parameter: [1, Huawei], [5, vivo], [12, Ericsson], [13, Nokia], [21, InterDigital],

Companies’ views on the details of DCI signaling:

Only use the reserved states in the antenna port(s) field in DCI: [4, ZTE], [10, CATT], [17, Intel], [22, LG]

Adding 1 bit to the antenna port(s) field in DCI:

Companies’ views on the details of RRC signaling:

RRC indicate a set of values (UE assumes no FD-CDM from other UE only when the value indicated by antenna port(s) field in DCI belongs to this set): [5, vivo]

RRC indicate a flag (FD-OCC on/off applies to all DMRS ports):

RRC to additionally configure a MCS threshold so that UE can recognize FD-OCC is turned off only if indicated MCS level is no less than the MCS threshold: [22, LG]

Moderator’s comment:

On the high level principle of UE indication method, companies’ views are evenly split. Pros and cons of each method are stated by the companies. Antenna port(s) filed in DCI may provide dynamic switching between FD-OCC on and off. RRC based configuration is easier in terms of specification effort and can support all cases of rank-1 transmission scenarios.

Among the companies support DCI indication, two options were identified: adding 1 bit or reuse reserved states. It seems most companies only want to use the reserved states in the antenna port(s) field in DCI (so not to increase DCI payload) for FD-OCC off indication. However, multiple companies have identified an issue where there’s no or only 1 reserved state for some case (*dmrs-Type*=1, *maxLength*=2, one codeword). Per previous agreement, FD-OCC off should apply to all rank-1 transmission at least with type-1 (both single and double symbol) DMRS. Unless reverting previous agreement and restricting to only type-1 DMRS with *maxLength*=1, it seems not possible to only use reserved states in the antenna port(s) field in DCI for FD-OCC off indication.

Among the companies support RRC based indication, not every company provided details of RRC signaling. It seems there are multiple options for RRC signaling as well: a flag or a set of DMRS configurations/antenna ports. Several companies [5, 22] argued that the former may not be preferred from a flexible scheduling point of view. Furthermore, [22] proposed an additional MCS threshold in RRC for FD-OCC off.

Formulate the following alternative proposals regarding the UE indication method for FD-OCC off and one of them should be chosen.

##### Proposal 3-2 (high priority)

Alt1:

* Support an RRC indicator to UE where the UE is able to assume that FD-OCC is not applied to all the antenna port(s) for DMRS.
  + Note: “FD-OCC is not applied” refers to the UE may assume that a set of remaining orthogonal antenna ports are not associated with the PDSCH to another UE, wherein the set of remaining orthogonal antenna ports are within the same CDM group and have different FD-OCC

Alt2:

* Support an RRC configuration of a set of antenna ports for DMRS where the UE is able to assume that FD-OCC is not applied to the antenna port(s) indicated by this RRC configuration.
  + FFS the set of antenna port indices by RAN1#106b-e
  + Note: “FD-OCC is not applied” refers to the UE may assume that a set of remaining orthogonal antenna ports are not associated with the PDSCH to another UE, wherein the set of remaining orthogonal antenna ports are within the same CDM group and have different FD-OCC

Alt3:

* Support to use reserved states in antenna port(s) field in DCI scheduling PDSCH to indicate antenna port(s) for DMRS where UE is able to assume that FD-OCC is not applied to the antenna port(s)
  + For *dmrs-Type*=1, only support *maxLength*=1
  + FFS the set of antenna port indices
  + Note: “FD-OCC is not applied” refers to the UE may assume that a set of remaining orthogonal antenna ports are not associated with the PDSCH to another UE, wherein the set of remaining orthogonal antenna ports are within the same CDM group and have different FD-OCC

Alt4:

* Support to add 1bit to antenna port(s) field in DCI scheduling PDSCH to indicate antenna port(s) for DMRS where UE is able to assume that FD-OCC is not applied to the antenna port(s)
  + Note: “FD-OCC is not applied” refers to the UE may assume that a set of remaining orthogonal antenna ports are not associated with the PDSCH to another UE, wherein the set of remaining orthogonal antenna ports are within the same CDM group and have different FD-OCC

Companies are encouraged to provide comments and to indicate preference/objection (if any) to the above alternatives.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | In our view, the most straightforward solution with minimum spec impact is Alt 1. For Alt 2, 3 and 4, we don’t see the need to introduce indication for certain antenna ports.  Therefore, we **support Alt 1**. |
| Qualcomm | We support Alt 3 as it provides more scheduling flexibility and will not increase the DCI size. |
| Intel | Our first preference is Alt3.  Our second preference is Alt4. |
| vivo | Alt 3 can’t support FD-OCC off for *dmrs-Type*=1 with *maxLength*=2;  Alt 4 increases DCI size;  Our first preference is Alt 2 and can accept Alt 1. |
| LG Electronics | We believe Alt2 is the most flexible method at least among 4 alternatives. As a next step, RAN1 should further discuss on which set of antenna port indices to apply FD-OCC off. In addition, FD-OCC off should be applied only to high MCS in order to avoid unnecessary reduction of multiplexing capability since the performance degradation due to FD-OCC is less sensitive in low MCS. To this end, an MCS threshold in RRC should be used so that this functionality is applied only for high MCS.  Regarding Alt1, it will reduce the scheduling flexibility. Only with a simple RRC flag, it is not possible to specify the exact condition (i.e., antenna port index and high MCS) in which FD-OCC should not applied.  Regarding Alt3, restricting to maxLength=1 is not a complete solution. FD-OCC off for rank1 transmission should also be configured when there are two FL DMRS symbols.  Regarding Alt4, it would be the least preferred method because it can increase the signaling overhead. |
| Nokia/NSB | We are fine with Alt 1 and Alt 2. |
| Apple | We support Alt-3. 2nd preference Alt-4. |
| CATT | We support Alt 3 |
| InterDigital | We support Alt 1. |
| Samsung | We prefer RRC based signaling, i.e., Alt1/2. To be clear, “all antenna port(s)” in Alt 1 here should be all the antenna port(s) satisfying the condition we agreed in the last meeting: for rank 1 PDSCH with type-1 [or type-2 DMRS], and should not be understood as all the antenna ports. |
| Futurewei | We support Alt 1 and Alt 2. |
| ZTE, Sanechips | We prefer the Alt3 and Alt4 is also acceptable. If the RRC configuration is used to indicate whether FD-OCC is applied, the flexibility can not be guaranteed. |
| Ericsson | We support Alt-1  We agree with Samsung that "all antenna port(s)" needs to be clarified according to the condition that we agreed last meeting.  We share the view with Lenovo that Alt-1 is the most straightforward solution with minimum spec impact, and minimum discussion time required. We don't have time to consider the fine details about different behavior for different port numbers. |
| NTT DOCOMO | Alt4 is not preferred as it increases unnecessary DCI overhead. Our best preference is Alt1, while still open to discuss among Alt1, Alt2 and Alt3, |
| Huawei, HiSilicon | We think RRC configuration is sufficient, and Alt1 is a complete solution, which is preferable rather than introducing more FFS points (e.g. in Alt2). Otherwise, a complete proposal should preferably be proposed for Alt2 in terms of which antenna ports can be disabled for FD-OCC. |

#### DMRS for multi-PDSCH/PUSCH scheduling

[1, Huawei] compared two DMRS patterns in time domain: Rel-15 DMRS pattern (with individual channel estimation per slot), and a bundling DMRS pattern where DMRS symbols are concentrated at the beginning of the scheduled multi-slot PDSCHs/PUSCHs (with joint channel estimation based on all the consecutive DMRS symbols). It observed about 0.2dB~0.6dB gain of the bundling DMRS pattern. [1, Huawei] then proposed that DMRS mapped on symbol l0 to symbol l0+S\*L-1 within the first PDSCH slot for the multi-slot scheduling, when only front-loaded DMRS is configured, where L is the length and l0 the starting symbol of legacy front-loaded DMRS.

[10, CATT] argued that given the channel estimation filter at the UE is usually optimized with fixed filter length based on current DMRS pattern, DMRS bundling will increase the UE implementation complexity since the enhancement depends on the receiver algorithm in UE implementation. With that, it proposed not to support potential DMRS enhancement for multi-PDSCH/PUSCH scheduling.

[15, Samsung] proposed for multiple PDSCHs/PUSCHs with contiguous time domain resource, DMRS time domain density can be lower than one DMRS per PUSCH/PDSCH to reduce DMRS overhead and DMRS bundling of multiple PUSCHs/PDSCHs can be applied to improve channel estimation performance.

[18, NTT DOCOMO] evaluated joint channel estimation (JCE) for multi-PDSCH scheduling and observed that the maximum gain of JCE over multi-PDSCH scheduling is about 0.41dB and 0.63dB in SCS of 480kHz and 960kHz, respectively. Furthermore, it argued that some restrictions will be required at transmitter side, which will cause less flexibility on the operation and a certain amount of specification impact. It proposed not to support JCE for multi-PDSCH scheduling.

[23, Apple] also argued that given there is current work on joint channel estimation for PUSCH in the Rel-17 coverage enhancement Work Item, to avoid duplication of effort between work items, the discussion on DMRS bundling and DMRS overhead reduction should be de-prioritized.

Companies’ view to support DMRS enhancement for multi-PDSCH/PUSCH scheduling are summarized below.

Yes: [1, Huawei], [15, Samsung]

No: [10, CATT], [18, NTT DOCOMO], [23, Apple] (deprioritize)

Moderator’s comment:

Looking at the available evaluation results and views expressed from contributions, it’s clear that companies have split views on whether to consider DMRS enhancement for multi-PDSCH/PUSCH scheduling in Rel-17.

Compared to previous meetings, there has not been a shift in company positions to form a majority for any of the proposed schemes. With that, moderator suggest companies continue discussion to see if any new aspects/arguments can be identified in this meeting. Otherwise, it’d be better to conclude and close the discussion considering limited remaining time of this WI.

##### Discussion point 3-3

Companies are encouraged to provide comments and/or suggestions on agreeable proposals if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We don’t see a need to consider further DMRS enhancements for multi-PDSCH/PUSCH scheduling due to very limited remaining time.  Also, we expect that the enhancements for PUSCH in coverage enhancements WI would be applicable to at least multi-PUSCH scheduling.  Also, we must note that no new DMRS patterns were adopted for PUSCH coverage enhancements |
| Qualcomm | We do not support discussing DMRS bundling for PDSCHs in Rel. 17, for multi-PUSCH grant, any enhancements made in coverage enhancement WI can be applied to the higher band. |
| vivo | Suggest to de-prioritize this discussion. |
| Nokia/NSB | We don’t support any new DMRS pattern. But we can consider UE assumption that all PDSCHs of multi-PDSCH scheduling are transmitted by the same precoder. |
| Apple | Discussion should be de-prioritized to avoid duplication of effort between work items. |
| InterDigital | Due to time limitation, we don’t see the need to further consider DMRS enhancements for multi-PDSCH/PUSCH scheduling. |
| Samsung | At least for PUSCHs scheduled by a single DCI or multiple DCIs, joint channel estimation feature introduced in Rel-17 CovEnh WI can be used for FR2-2. |
| Futurewei | Agree that the joint channel estimation feature introduced in Rel-17 CovEnh WI can be used for FR2-2. |
| ZTE, Sanechips | We do not support considering DMRS enhancement for multi-PDSCH/PUSCH scheduling in Rel-17. |
| Ericsson | Discussion should be de-prioritized. Regarding the work in the CovEnh WI, transport block over multiple slots (TBoMS) was considered which is different than multi-PUSCH scheduling, especially when the latter can have slot gaps. |
| NTT DOCOMO | We do not see this issue essential for Rel-17 design. Thus at least we should deprioritize this. Furthermore, looking at the gain, we do not think this should be supported. |
| Huawei, HiSilicon | Although we saw some gains of optimizing the DMRS patterns in particular for reducing the HARQ delay, we can accept the conclusion at this meeting. We would like to note, though, that if HARQ delay is not deemed critical to optimize, then the same criterion should apply to other discussions including on the UE (and gNB) processing timelines. |

## 2.4. Other issue(s)

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [20, Lenovo] | Observation 1: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, the selection of SCS value should not limited based on the frequency range. Other factors of channel conditions such as phase noise, ICI, Doppler, CQI, etc. plays an important role in determining the SCS value:   * For DL channel, UE has all the required estimates related to channel, receiver phase noise and other impairments, etc.   Proposal 10: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, UE assistance for SCS/BWP selection should be supported to take in to account all the channel measurements and receiver impairments that are more prominent at higher frequency range   * CSI reporting should be enhanced to report back suitable subcarrier spacing value based on measurements and receiver characteristics at UE |
| [25, Qualcomm] | Proposal 5: Introduce new TRS configuration with higher frequency densities, 6 or 12 tones per RB to increase the TTL pull-in range when SCS of SSB is lower than the SCS of the data transmission. |

### UE-assisted SCS adaptation

It is observed in [20, Lenovo] that for supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, the selection of SCS value should not limited based on the frequency range. Other factors of channel conditions such as phase noise, ICI, Doppler, CQI, etc. plays an important role in determining the SCS value. It further argued that UE is in a better position compared to gNB to make corresponding decision on which SCS value is more suitable given the UE estimates DL channel conditions such as phase noise, ICI, Doppler, CQI etc., and some other impairments based on the supported receiver algorithm. It then proposed that CSI reporting should be enhanced to report back suitable subcarrier spacing value based on measurements and receiver characteristics at UE.

Moderator’s comment:

Right now, it is a single company proposal. The proposal itself seems suggesting a UE recommendation of SCS value in the CSI report. It’s not clear about whether gNB will always follow that UE recommendation or the corresponding gNB behavior. Suggest the proponent company to clarify and other companies to provide input for discussion.

##### Discussion point 4-1

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | In our proposal, it is UE’s recommendation to use a certain SCS, however, the decision will be up to gNB to accordingly update the SCS or not.  In our view, the main motivation is that the receiver side has more accurate information in terms determining the appropriate SCS and therefore, it makes sense for UE to include it in the reporting. |
| Nokia/NSB | We don’t see critical reason for enhancement. |
| Huawei, HiSilicon | Dynamically switching SCS based on link adaptation seems like a whole WI in itself. This is not a simple optimization. |

### TRS enhancements

In [25, Qualcomm], it is observed that for PDSCH with high SCS (e.g., 960 kHz), the time tracking loop (TTL) may not be able to correct the typical timing error resulted from the 120kHz SSB detection as it may be out of its pull-in range. It then proposed to introduce new TRS configuration with higher frequency densities, 6 or 12 tones per RB to increase the TTL pull-in range when SCS of SSB is lower than the SCS of the data transmission.

Moderator’s comment:

Right now, it is a single company proposal. Suggest other companies to provide input for discussion.

##### Discussion point 4-2

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | We believe that this enhancement will be crucial when having mixed numerologies for SSB and PDSCH and will not require large specification efforts. |
| Intel | We are open to discuss the issue. If tracking issues are identified, we are supportive of providing features that will resolve the problem. |
| Nokia/NSB | TRS sequence still can manage the problem. We don’t see need for TRS enhancement. |
| Huawei, HiSilicon | We are open to investigating the issue, but it seems late for RAN1 to handle this task. It may be left for RAN4 to investigate when defining performance requirements, and if indeed an issue is found than RAN4 could ask RAN1 to provide specification support for solving the issue. |
|  |  |

# Conclusion

TBD

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