TSG RAN Working Group 1 (Radio layer 1) Beijing (China), 18-21 January 2000

Agenda Item: Ad-hoc 5
Source: Alcatel

Title: CR 25.212-043 and CR 25.222-020: Improvement of convolutional

coding scheme for very low code block sizes

**Document for:** Decision

#### Introduction

A slight modification of the current convolutional coding scheme was proposed in [1] to improve it for very low code block sizes (< 10 bits). This contribution includes the related CRs for 25.212 and 25.222.

#### References

[1] 3GPP R1-00-0095, "Improvement of convolutional coding scheme for very low code block size", January 2000, Alcatel

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# Document R1-00-0153 e.g. for 3GPP use the format TP-99xxx or for SMG, use the format P-99-xxx

CHANGE REQUEST  Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.							
	<b>25.212 CR 043</b> Current Version:	3.1.0					
GSM (AA.BB) or 3G (AA.BBB) specification number↑ ↑ CR number as allocated by MCC support team							
For submission to: TSG-RAN #7  List expected approval meeting # here  for information for info							
Form: CR cover sheet, version 2 for 3GPP and SMG  The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc  Proposed change affects: (at least one should be marked with an X)  The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc  WE X UTRAN / Radio X Core Network							
Source:	Alcatel <u>Date:</u> 2	2000-01-18					
Subject:	Improvement of convolutional coding for low code block sizes						
Work item:							
(only one category Shall be marked	A Corresponds to a correction in an earlier release B Addition of feature C Functional modification of feature D Editorial modification	hase 2 elease 96 elease 97 elease 98 elease 99 elease 00					
Reason for change:	The current convolutional coding included in the specifications is not we low code block sizes. This CR proposes to slightly modify it in order to in low code block sizes (by decreasing the number of tail bits)						
Clauses affected: 4.2.3							
Other specs affected:							
Other comments:							
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### 4.2.3 Channel coding

Code blocks are delivered to the channel coding block. They are denoted by  $o_{ir1}, o_{ir2}, o_{ir3}, \ldots, o_{irK_i}$ , where i is the TrCH number, r is the code block number, and  $K_i$  is the number of bits in each code block. The number of code blocks on TrCH i is denoted by  $C_i$ . After encoding the bits are denoted by  $y_{ir1}, y_{ir2}, y_{ir3}, \ldots, y_{irY_i}$ . The encoded blocks are serially multiplexed so that the block with lowest index r is output first from the channel coding block. The bits output are denoted by  $c_{i1}, c_{i2}, c_{i3}, \ldots, c_{iE_i}$ , where i is the TrCH number and  $E_i = C_i Y_i$ . The output bits are defined by the following relations:

$$c_{ik} = y_{i1k} k = 1, 2, ..., Y_i$$

$$c_{ik} = y_{i,2,(k-Y_i)} k = Y_i + 1, Y_i + 2, ..., 2Y_i$$

$$c_{ik} = y_{i,3,(k-2Y_i)} k = 2Y_i + 1, 2Y_i + 2, ..., 3Y_i$$
...
$$c_{ik} = y_{i,C_i,(k-(C_i-1)Y_i)} k = (C_i - 1)Y_i + 1, (C_i - 1)Y_i + 2, ..., C_iY_i$$

The relation between  $o_{irk}$  and  $y_{irk}$  and between  $K_i$  and  $Y_i$  is dependent on the channel coding scheme.

The following channel coding schemes can be applied to TrCHs:

- Convolutional coding
- Turbo coding
- No channel coding

The values of  $Y_i$  in connection with each coding scheme:

- Convolutional coding,  $\frac{1}{2}$  rate:  $Y_i = 2 \times (K_i + N_i^{(tail)}) + 6$ ;  $\frac{1}{3}$  rate:  $Y_i = 3 \times (K_i + N_i^{(tail)}) + 24$
- Turbo coding, 1/3 rate:  $Y_i = 3*K_i + 12$
- No channel coding,  $Y_i = K_i$

CPCH, DCH, DSCH, FACH

where  $N_i^{(tail)}$  is the number of tail bits for the convolutional coding and is defined in section 4.2.3.1.

Transport channel type

BCH
PCH

RACH

Convolutional code

Coding scheme

Coding rate

1/2

1/3, 1/2

Turbo Code
No coding

**Table 1: Error Correction Coding Parameters** 

If no code blocks are input to the channel coding ( $C_i = 0$ ), no bits shall be output from the channel coding, i.e.  $E_i = 0$ .

1/3

#### 4.2.3.1 Convolutional coding

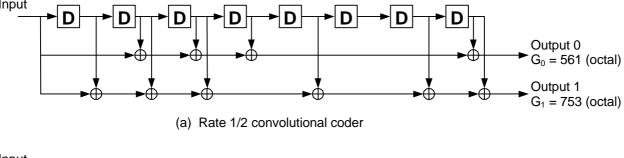
Convolutional codes with constraint length 9 and coding rates 1/3 and 1/2 are defined.

The configuration of the convolutional coder is presented in figure 3.

Output from the rate 1/3 convolutional coder shall be done in the order output0, output1, output2, output0, output1, output 2, output 0,...,output 2. Output from the rate 1/2 convolutional coder shall be done in the order output 0, output 1, output 0, output 1, output 0, ..., output 1.

 $\frac{8-N_i^{(tail)}}{2}$  tail bits with binary value 0 shall be added to the end of the code block before encoding, where  $N_i^{(tail)}$  is the minimum value of 8 and  $K_i$ .

The initial value of the shift register of the coder shall be "all 0" when starting to encode the input bits.



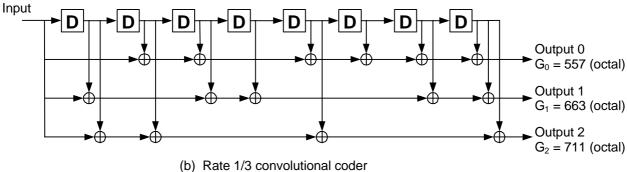


Figure 3: Rate 1/2 and rate 1/3 convolutional coders

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GSM (AA.BB) or 3	BG (AA.BBE	3) specification i	number↑		1	CR number	as allocated by MCC	support team	
For submission to: TSG-RAN #7 for approval for information Strategic for information TSG-RAN #7 for approval for information Strategic for informati							nly)		
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Source:	Alca	tel					Date:	2000-01-18	
Subject:	Impr	ovement of	convolution	al coding	for low	code blo	ck sizes		
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Other comments:									
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where  $N_i^{(tail)}$  is the number of tail bits for the convolutional coding and is defined in section 4.2.3.1.

**Table 1: Error Correction Coding Parameters** 

Transport channel type	Coding scheme	Coding rate			
ВСН					
PCH		1/2			
	Convolutional code				
RACH	Convolutional code				
CPCH, DCH, DSCH, FACH		1/3, 1/2			
	Turbo Code	1/3			
	No coding				

If no code blocks are input to the channel coding ( $C_i = 0$ ), no bits shall be output from the channel coding, i.e.  $E_i = 0$ .

#### 4.2.3.1 Convolutional coding

Convolutional codes with constraint length 9 and coding rates 1/3 and 1/2 are defined.

The configuration of the convolutional coder is presented in figure 3.

 $G_2 = 711 \text{ (octal)}$ 

Output from the rate 1/3 convolutional coder shall be done in the order output0, output1, output2, output0, output1, output 2, output 0,...,output 2. Output from the rate 1/2 convolutional coder shall be done in the order output 0, output 1, output 0, output 1, output 0, ..., output 1.

The initial value of the shift register of the coder shall be "all 0

 $8N_i^{(tail)}$  tail bits with binary value 0 shall be added to the end of the code block before encoding, where  $N_i^{(tail)}$  is the minimum value of 8 and  $K_i$ . "when starting to encode the input bits.

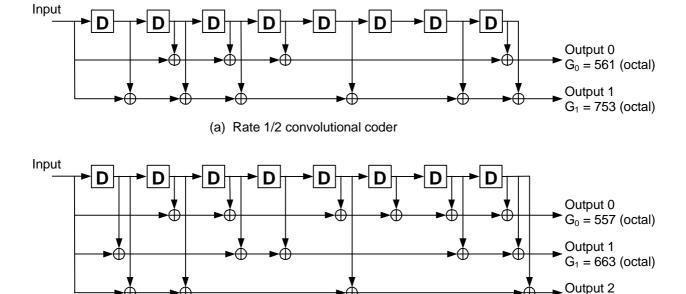


Figure 3: Rate 1/2 and rate 1/3 convolutional coders

(b) Rate 1/3 convolutional coder