Agenda Item:	Ad Hoc 14
Source:	Samsung Electronics Co.
Title:	Proposed Text for Gated DPCCH Transmission in 25.214
Document for	Discuss and approve

1. Introduction

The issue of Gated DPCCH transmission has been studied and discussed by WG1, which has agreed on the advantages it can provide to both the UE and UTRAN. Those advantages are:

- Increase of battery life

- capacity increase due to interference reduction

In this document, we present the proposed text for gated DPCCH transmission for the technical specification document 25.214. The following issues are addressed and described: the issue of random gating pattern, mandatory/optional status of gating, gating in compressed mode, and the procedures in one-way (downlink only gating) operation.

2. References

[1] TSGR2#9(99)g88, "Draft minutes of WG2 meeting #8" Cheju, Korea, 2-5, Nov. 1999.

[2] TSGR1#9(99)i27 (TSGR2#8(99)g67), "Response (to TSG-RAN WG1, TSG-RAN WG4) to LS on Gated DPCCH transmission," WG2, Cheju, 2-5 Nov. 1999.

[3] TSGR4#8(99)779, "Report of the 8th TSG-RAN WG4 meeting (Draft report)," Sophia Antipolis, 26-29, Oct. 1999.

[4] TSGR4#8(99)751, "Proposed Response to Liaison Statement on impact of gated DPCCH at cell boundaries," Sophia Antipolis, 26 - 29 Oct 1999.

[5] 3GPP RAN TS 25.214 v1.3.0(1999-09)

[6] TSGR1#8(99)f43, "Reducing EMC problem in uplink DPCCH Gated mode," Mitsubishi, New York, 12-15 Oct. 1999.

[7] TSGR1#8(99)g54, "Revised Random Pattern for DPCCH Gated Transmission (Rev. of R1-99f80)," Samsung, New York, 12-15, Oct. 1999.

[8] TSGR1#9(99)j51, "Random Pattern for Gated DPCCH transmission," Dresden, 30 Nov. – 3 Dec. 1999

================= START OF TEXT PROPOSAL ==================

7.2　Gated DPCCH Transmission in Packet Transmission Mode

7.2.1　General

In packet transmission mode, UE and UTRAN stop transmission of DPDCH if there is no data to transmit while continue transmission of DPCCH. If the gated transmission is enabled, then DPCCH shall be gated-on in specified time slots to reduce the transmission rate of Pilot, TPC, TFCI, and FBI (uplink only) while it will be gated-off during all other time slots. The UE shall report the capability of gating such as gating rate, gating pattern, and direction of gating to UTRAN when needed, then UTRAN shall determine appropriate gating parameter values. As a result, for the UTRAN, the gated DPCCH transmission is an option in both uplink and downlink while, for the UE, it is an option in the uplink and mandatory in the downlink. The combinations of parameters need to be negotiated between UTRAN and the UE are given in 7.2.2. In addition 7.2.2 describes the required operations of the UE when the gating operation is used only in the downlink. It is possible to transmit DPDCH during gated operation, directed by higher layer. When only the DPCCH is transmitted in gated transmission mode, the UTRAN and the UE shall gate-off all time slots other than the time slots specified in 7.2.3. During transmission of DPDCH in gating mode, all of the corresponding physical layer control information (DPCCH) shall be transmitted while the gating mode is maintained, and the receiver shall ignore the invalid part of DPCCH according to the appropriate gating pattern. In this case, TFCI and Pilot bits shall not be ignored because it provides the physical information of DPDCH. In the compressed mode, the gated DPCCH transmission shall be stopped through the higher layer signaling between the UE and UTRAN.

7.2.2　Combination of Gating Operation Mode

UTRAN and the UE negotiate the combination of gating operation parameters when needed. These parameters are:

Gating Rate	1	1/3	1/5

Gating Pattern	Random	Regular

Direction	Downlink Only	Uplink and Downlink

If the gating transmission is disabled (i.e., gating rate = 1), then no gating pattern will be used. In the case where gated DPCCH transmission is used only for the downlink, then the UE will transmit the DPCCH in every time slots, and the UE will:
- adjust the transmit power in response to the valid downlink TPC, where valid downlink TPC means the downlink TPC transmitted at the gated-on slots
- ignore any downlink TPC that is received during the gated off slot, and the downlink transmit power shall remain constant
- generate and transmit uplink TPC based on the downlink symbols if the time slot is associated with the downlink gate-on slot
- repeat the previous uplink TPC if the time slot is associated with the downlink gate-off slot

7.2.3　Gated DPCCH Transmission

7.2.3.1　DPCCH Random Gating Pattern Generation

If the gated DPCCH transmission is enabled with random gating pattern, the downlink and uplink gating pattern shall be determined based on the parameters shown in Table 1.

Table 1. Parameters for Random Gating Pattern

Parameter	Value
CFN	0, 1, …, 255 (8bits)
gating rate	1/3 or 1/5
Number of gating group(N_G)	5,　　　if gating rate is 1/3 3,　　　if gating rate is 1/5
Gating group size (S_G)	3,　　　if gating rate is 1/3 5,　　　if gating rate is 1/5

| A=(a_0,a_1,...,a_18) | 1011010011011101001 (19bits) |

CFN is a frame counter ranged from 0 to 255. N_G represents the number of gating groups in a frame whileeach gating group consists of S_G (gating group size) consecutive time slots. Let i and j be the CFN of the frame (i=0,1,...,255) and the jth gating group, respectively, then the allocated time slot, s(i,j), shall be given by

$$s(i,j) = \begin{cases} (A_j \oplus C_i)_{10} \bmod (S_G - 1) + 1, & j = 0 \\ (A_j \oplus C_i)_{10} \bmod S_G, & j = 1,...,N_G - 2 \\ S_G - 1, & j = N_G - 1 \end{cases}, \quad i = 0,1,...,255$$

where $A_j = (a_j, a_{j+1},...,a_{j+15})$, j=0,1,...,$N_G$-2, is a 16bit sequence constructed from sequence A in Table 1, and $C_i = ((CFN)_2, (CFN)_2)$ is a 16bits sequence consisting of repeated binary representation of 8 bits CFN, where $(x)_m$ represents the m-ary representation of x. Note that the first time slot (slot #0) shall never be allocated to s(i,j) whichis the case of j=0., On the other hand the last time slot (slot #14) shall always be allocated to s(i,j) which is the case of j=N_G-1. Figure 1 describes the method of calculation s(i,j).
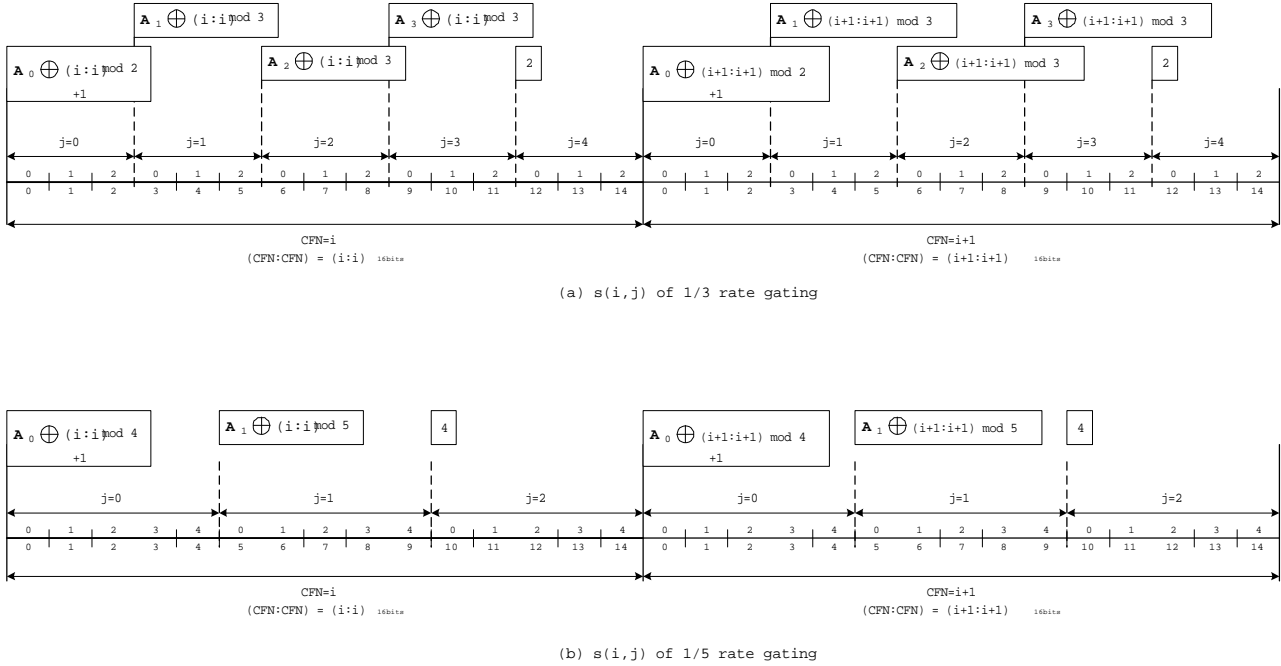

(a) s(i,j) of 1/3 rate gating

(b) s(i,j) of 1/5 rate gating

Figure 1. Calculation of s(i,j): (a) 1/3 rate (b) 1/5 rate

7.2.3.2 Gated-on Slot Allocation in Gated DPCCH Transmission

When the gated transmission mode is enabled in the downlink and uplink, UTRAN and the UE shall transmit the DPCCH in the time slots specified in Table 2 and Table 3. Only one slot per each gating group shall be gated-on.

Table 2 : Downlink DPCCH gate on time slot allocations during gated transmission mode enabled

Gating Pattern	Gating Rate	Downlink DPCCH gate on time slot allocation	
		Pilot	TPC, TFCI
Regular Pattern	1	every time slots (0~14)	every time slots (0~14)
Regular Pattern	1/3	$j \times 3$	$1 + j \times 3$
	1/5	$1 + j \times 5$	$2 + j \times 5$
Random Pattern	1/3	$j \times S_G + s(i,j) - 1$	$j \times S_G + s(i,j)$
	1/5	(defined in 7.2.3.1)	(defined in 7.2.3.1)

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number. (defined in 7.2.3.1)

Table 3 : Uplink DPCCH gate on time slot allocations during gated transmission mode enabled

Gating Pattern	Gating Rate	Uplink DPCCH gate on time slot allocation
		Pilot, TFCI, FBI, TPC
Regular Pattern	1	every time slots (0~14)
Regular Pattern	1/3	$2 + j \times S_G$
	1/5	$4 + j \times S_G$
Random Pattern	1/3	$j \times S_G + s(i, j)$
	1/5	(defined in 7.2.3.1)

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number. (defined in 7.2.3.1)

The relative timings of the downlink and uplink DPCCH transmission with random and regular gating pattern which are summarised in Table 2 and Table 3 are depicted in Figure 2, Figure 3, respectively.
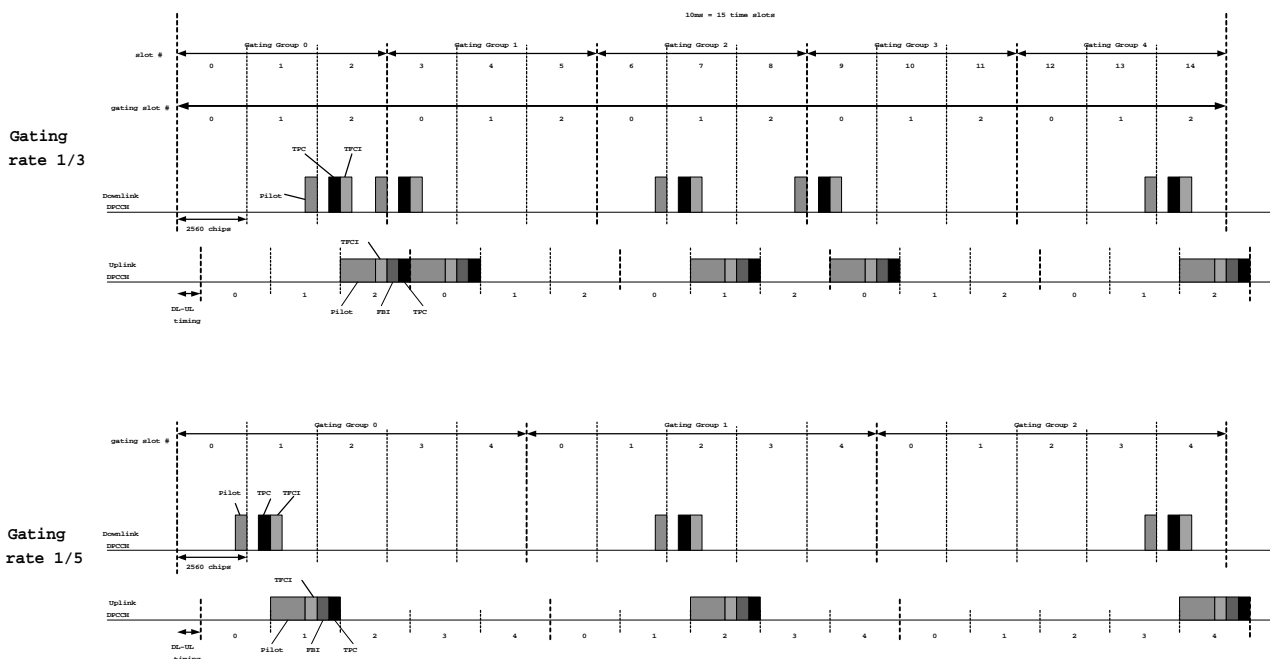

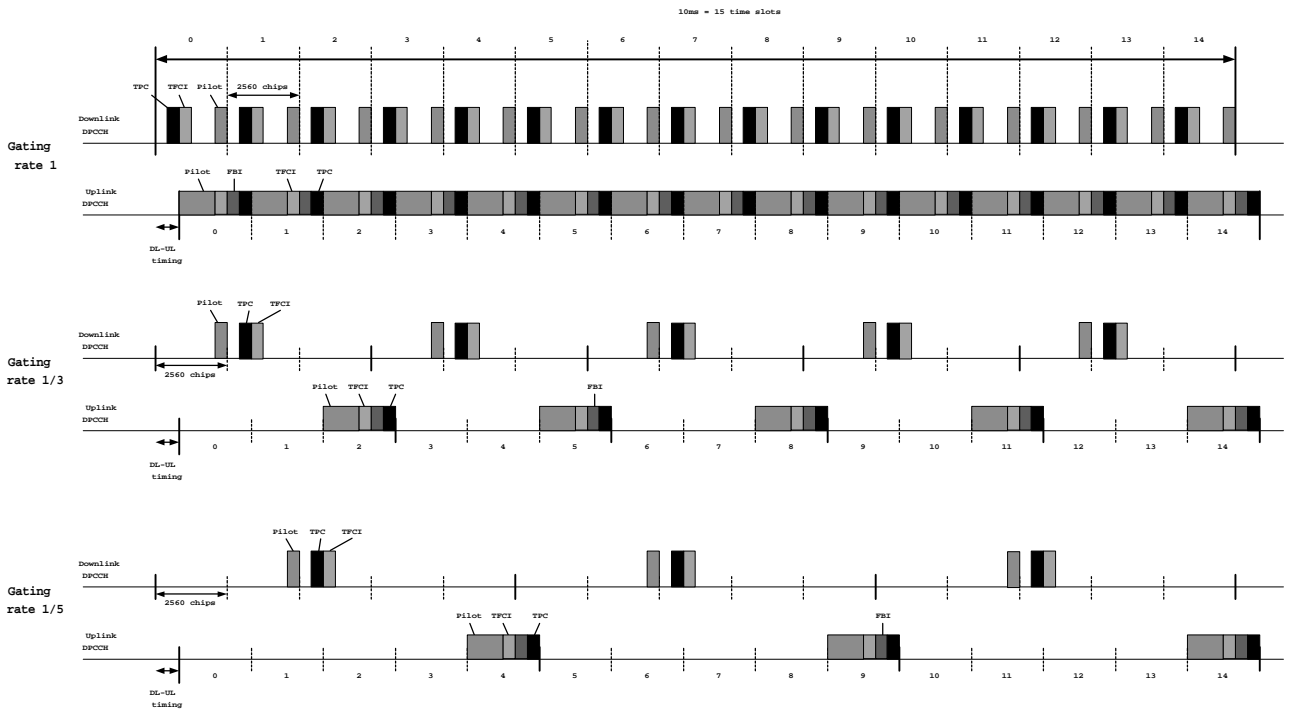**Figure 2. Downlink and uplink DPCCH transmission with random gating pattern (example)**

Figure 3 : Downlink and uplink DPCCH transmission timing with regular gating pattern

======================== END OF TEXT PROPOSAL ========================