TSG-RAN Working Group 1 meeting #10
Beijing, China
January 18 – 21, 2000

TSGR1#10(00)0100

Agenda item:

Source: Ericsson

Title: Timing of PDSCH

Document for: Approval

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1 Introduction

In TS 25.211, section 7.5, the DPCH/PDSCH relative timing is specified. The frame of the PDSCH, which shall be received by the UE, begins between 1 slot ahead of the associated frame of the DPCH until 14 slots after this frame starts. The TFCI that is giving the transport format combination information of the PDSCH is thereby always received after the reception of the PDSCH frame has started.

This contribution shows that this will lead to unnecessary high buffering and processing requirements. By changing the timing, both buffering and processing can be reduced.

2 Concerns about the DPCH/PDSCH timing

The TFCI information on the DPCH includes information about the spreading factor and channelisation code of the shared PDSCH. Since the timing is according to Figure 1 these parameters are not known when the PDSCH is received. According to TS 25.213, the shared channel occupies one subtree of the channelisation codes. Therefore the data must be stored with the minimum spreading factor that is supported by that UE. Then these samples must be combined to the actual rate when the actual spreading factor and channelisation code is known.

The timing between the PDSCH frame and the associated DPCH frame leads to high additional complexity in the UE using the PDSCH due to the partial despreading and to an additional large buffer that must be implemented in the UE.

A function must be implemented doing the partial despreading and final combination with the correct spreading factor and channelisation code. This is the only downlink channel where the spreading factor is unknown when receiving the frame, so special functionality is needed to cope with the PDSCH.

Furthermore the UE has to be designed to store more data at minimum spreading factor due to the extra delay in the reception of the TFCI in the UE. In worst case the TFC information is complete a slot after the PDSCH frame is completely received. It can not start to process the data in one frame until the TFC information is received and this leads to an extra delay in the UE that has to be buffered at minimum spreading factor.

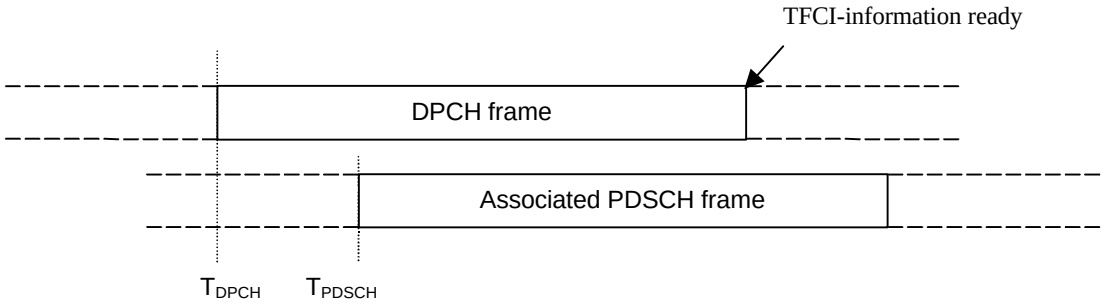

Figure 1: Association between DPCH and PDSCH frames

3 Proposal

Having a time delay between the end of the DPCH frame and the beginning of the associated PDSCH frame means that the spreading factor and the channelisation code is known when receiving the PDSCH frame. Thereby the PDSCH do not require any additional hardware in the UE compared with receiving other physical downlink channels. Further, the extra buffering needed is avoided, leading to reduced memory requirements in the UE. Actually, the extra buffering is reduced as soon as the PDSCH is not allowed to start before the start of the associated PDCH frame.

Hence, we propose a modified timing between DPCH frame and the associated PDSCH frame, where the PDSCH frame may start between 0 and 15 slot after the end of the DPCH frame. Since the TFCI is placed in the first half of the slot, this will give some time (600 μs as a minimum) to process the TFCI before the PDSCH frame arrives at the UE.

The proposed change will lead to a significant reduction in UE complexity with no corresponding drawbacks. The only possible concern we can see would be that delay is increased somewhat (10.7 ms on the average) for the data that is transmitted on the DSCH. However, since the DSCH is anyway used for delay insensitive packet services, with no real-time constraints, this is not seen as a drawback.

3GPP TSG RAN WG1 Meeting #10
Beijing, China, Jan 18 – 21, 2000

***Document* ???99???**
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	028	Current Version:	3.1.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to: TSG-RAN #7 *list expected approval meeting # here ↑*

for approval [X] for information [ ]

strategic [ ] non-strategic [ ] *(for SMG use only)*

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Ericsson **Date:** 2000-01-14

Subject: Timing of PDSCH

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	[ ]
A	Corresponds to a correction in an earlier release	[ ]
B	Addition of feature	[ ]
C	Functional modification of feature	[X]
D	Editorial modification	[ ]

Release:

Phase 2	[ ]
Release 96	[ ]
Release 97	[ ]
Release 98	[ ]
Release 99	[X]
Release 00	[ ]

Reason for change: The relative timing between the start of a DPCH frame and the associated PDSCH frame should be increased in order to lower the complexity of the terminal.

Clauses affected: 7.5

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 28.

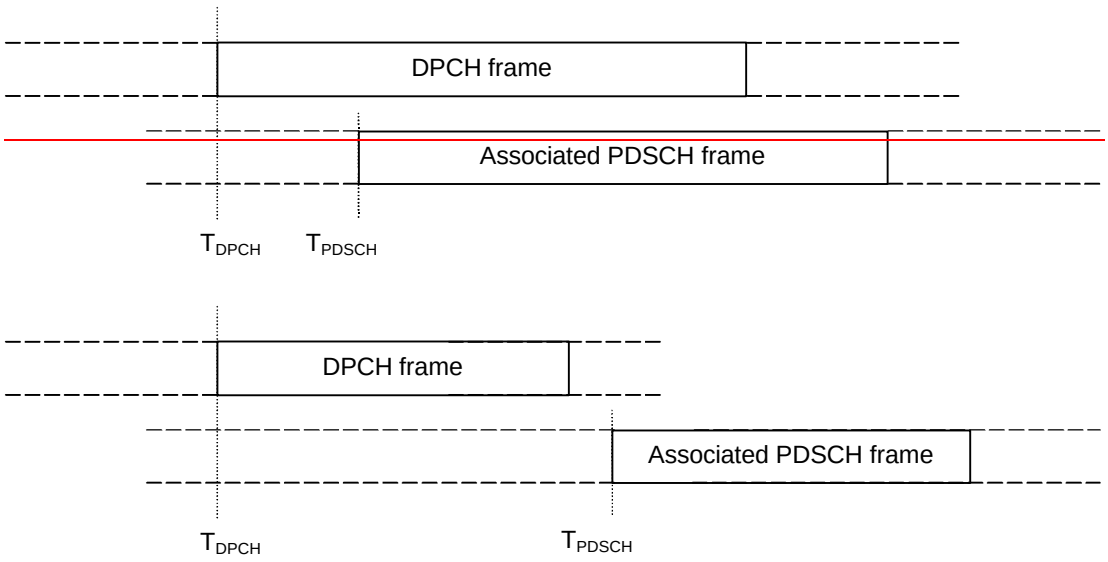

Figure 28: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation ~~35840 chips < T_{DPCH} - T_{PDSCH} ≤ 2560 chips~~ 38400 chips ≤ T_{PDSCH} - T_{DPCH} < 76800 chips, i.e. the associated PDSCH frame starts anywhere between the end of the DPCH frame~~1 slot before or~~ up to 15~~4~~ slots behind the end of the DPCH frame.