TSG-RAN Working Group 1 meeting #10 **TSGR1#10(00)0092**

Beijing, China, January 18-21, 2000

**Agenda Item:** 9
**Source:** CWTS
**To:** TSG RAN WG1
**Title:** Frame Structure for low chip rate TDD option
**Document for:** Approval

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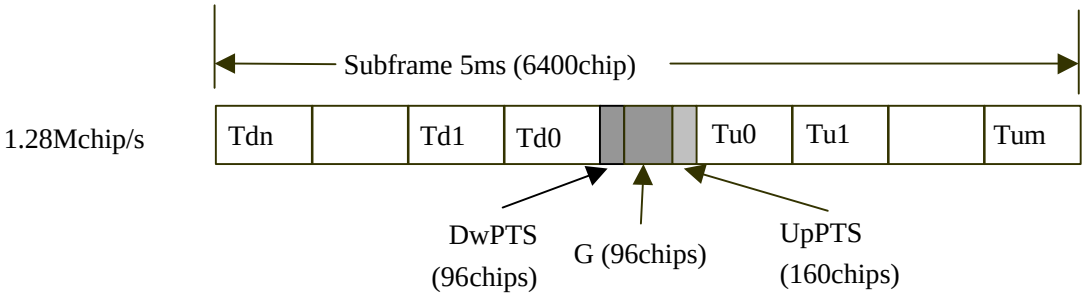
## Introduction

In 3GPP, there are two options for TDD mode. They are high chip rate option (3.84Mcps) and low chip rate option (1.28Mcps). The current specifications for TDD mode are mainly suitable for the high chip rate option. Due to the difference of the chip rate, a new frame structure for low chip rate TDD option will be proposed in this proposal. To enable the low chip rate with it's specific features and properties, other proposals will also be proposed later on by CWTS.

## Frame structure for low chiprate option

For both high chip rate option and low chip rate option, the frame length is 10ms. And for low chip rate option, this 10ms frame is divided into 2 sub-frames of 5ms to allow the fast update of power control and smart antenna beamforming. The frame structure for each sub-frame in the 10ms frame length is the same.

The frame structure for each sub-frame is shown in Figure 1.




Where n+m+2=7

Figure 1 Frame structure for low chip rate option

Tdn: the nth normal downlink time slot, 864 chips duration;
Tun: the nth normal uplink time slot, 864 chips duration;
DwPTS: downlink pilot time slot, 96 chips duration;
UpPTS: uplink pilot time slot, 160 chips duration;
G: main guard period for TDD operation, 96 chips duration;

In Figure 1, the total number of normal traffic time slot for uplink and downlink is 7, and the length for each normal time slot is 864 chips duration. Between the downlink time slot and uplink time slot, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for low chip rate option, there is only one

switching point.

Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by shift the position of the switching point. It should be noted that in asymmetric operation mode, at least one normal uplink time slot and one downlink time slot will be allocated for traffic. The guard period G of 96 chips can support the cell radius more than 10km for macro-, micro- and pico- cell operation.

## Burst structure for low chip rate option

In correspond to the frame structure described above, the burst structures for Tdn, Tun, DwPTS and UpPTS are proposed.

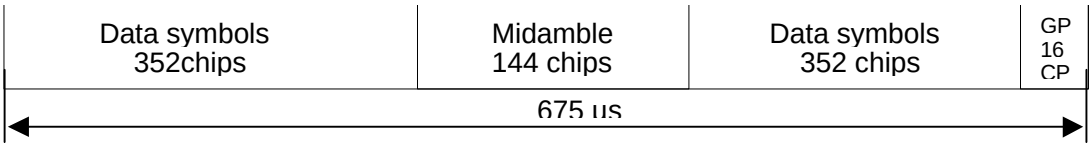



Figure 2 Burst structure for normal traffic time slot

The GP field in Figure 2 for each time slot is used for protection between time slots to avoid the long delay multi-path interference.

The structure for UpPTS and DwPTS is described in Figure 3 and Figure 4.

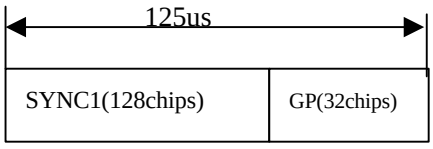



Figure 3 Structure for UpPTS

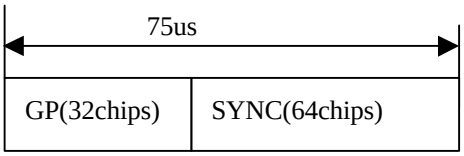



Figure 4 Structure for DwPTS

In DwPTS and UpPTS, the content of SYNC and SYNC1 field are used for downlink and uplink pilot. The GP fields are used to separate the downlink (uplink) pilot from the normal downlink (uplink) time slot.

The proposed frame structure and the related burst structure for low chip rate option can full fill the requirements for 3rd generation services and can provide the data services up to 2Mbps in a single 1.6MHz carrier. And the proposed frame structure can support all the environments of macro-, micro- and pico- cells. In vehicular environment, the speed can be more than 120km/h. Also in the proposed frame structure, some specific properties for low chip rate option such as smart antenna technology, uplink synchronisation, beamforming, etc can be well supported.

## Conclusion

The low chip rate TDD option of 1.28Mcps has already included in the specification. Based on the descriptions above and to enable the low chip rate with it's specific properties, it's proposed to include this new frame structure for low chip rate TDD option in new clause 5.1.2 of TS 25.221.

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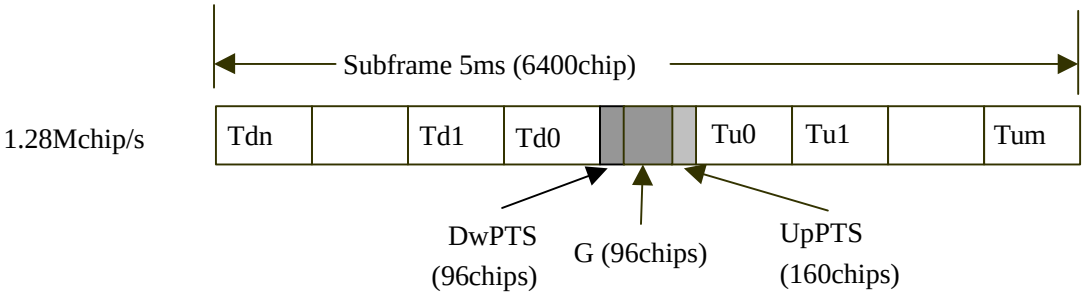
5.1.1 Frame structure for high chip rate option

5.1.2 Frame structure for low chip rate option

For low chip rate option, the 10ms frame is divided into 2 sub-frames of 5ms. The frame




Where n+m+2=7

structure for each sub-frame in the 10ms frame length is the same and is shown in Figure 5:

Figure 5 Frame structure for low chip rate option

Tdn: the nth normal downlink time slot, 864 chips duration;
Tun: the nth normal uplink time slot, 864 chips duration;
DwPTS: downlink pilot time slot, 96 chips duration;
UpPTS: uplink pilot time slot, 160 chips duration;
G: main guard period for TDD operation, 96 chips duration;

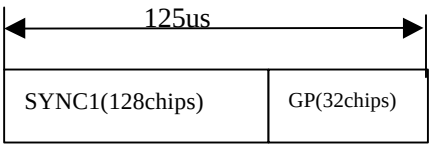



Figure 6 Structure of UpPTS

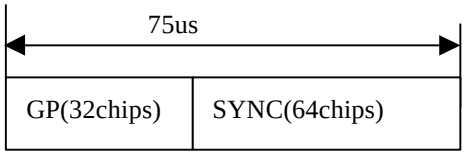
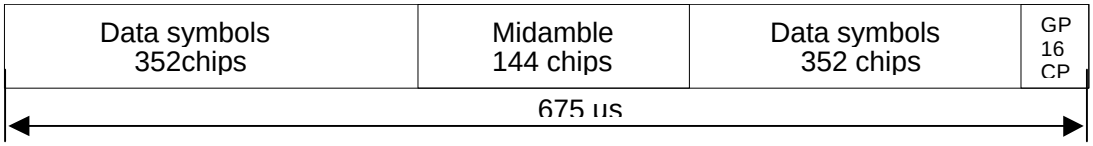



Figure 7 Structure of DwPTS

In DwPTS (see Figure 6) and UpPTS (see Figure 7), the content of SYNC and SYNC1 field are used for downlink and uplink pilot. The length for SYNC sequence is 64 chips and the length for SYNC1 is 128chips. The GP fields are used to separate the downlink (uplink) pilot from the normal downlink (uplink) time slot and the length for both GP are 32 chips.

Figure 8 Burst sturecture for Tdn and Tun




In burst structure (see Figure 8), the GP field has the length of 16chips for protection between time slots. The midamble used for channel estimation has the length of 144chips and the data fields in each side of the midamble field has the payload of 352chips.

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