TSG-RAN Working Group 1 meeting #10
Beijing, China
18 – 21 Jan, 2000

TSGR1#10(00)087

Agenda item: AH 10

Source: Siemens

Title: CR 25.213-021:Downlink signal flow corrections
and CR 25.213-022: Uplink signal flow corrections

Document for: Decision

As has been pointed out on the WG1 reflector the signal flows between the block diagrams in TS 25.213 are not completely correct. Also the notation of the scrambling code for the downlink DPDCH/DPCCH is not consistent with the scrambling code notation for PCPCH which can now take either long or short constituent codes.

The CRs 021 and 022 aim to correct these errors.

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Beijing, China, 18-21 Jan 2000

Document R1-00087
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

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25.213	CR	021	Current Version:	3.1.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN#7	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source: Siemens **Date:** 12-Jan-2000

Subject: Downlink signal flow corrections

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X	**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: Correction of erroneous indication of signal flow between downlink block diagrams.

Clauses affected: 5.1 ,5.3.2

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

<--------- double-click here for help and instructions on how to create a CR.

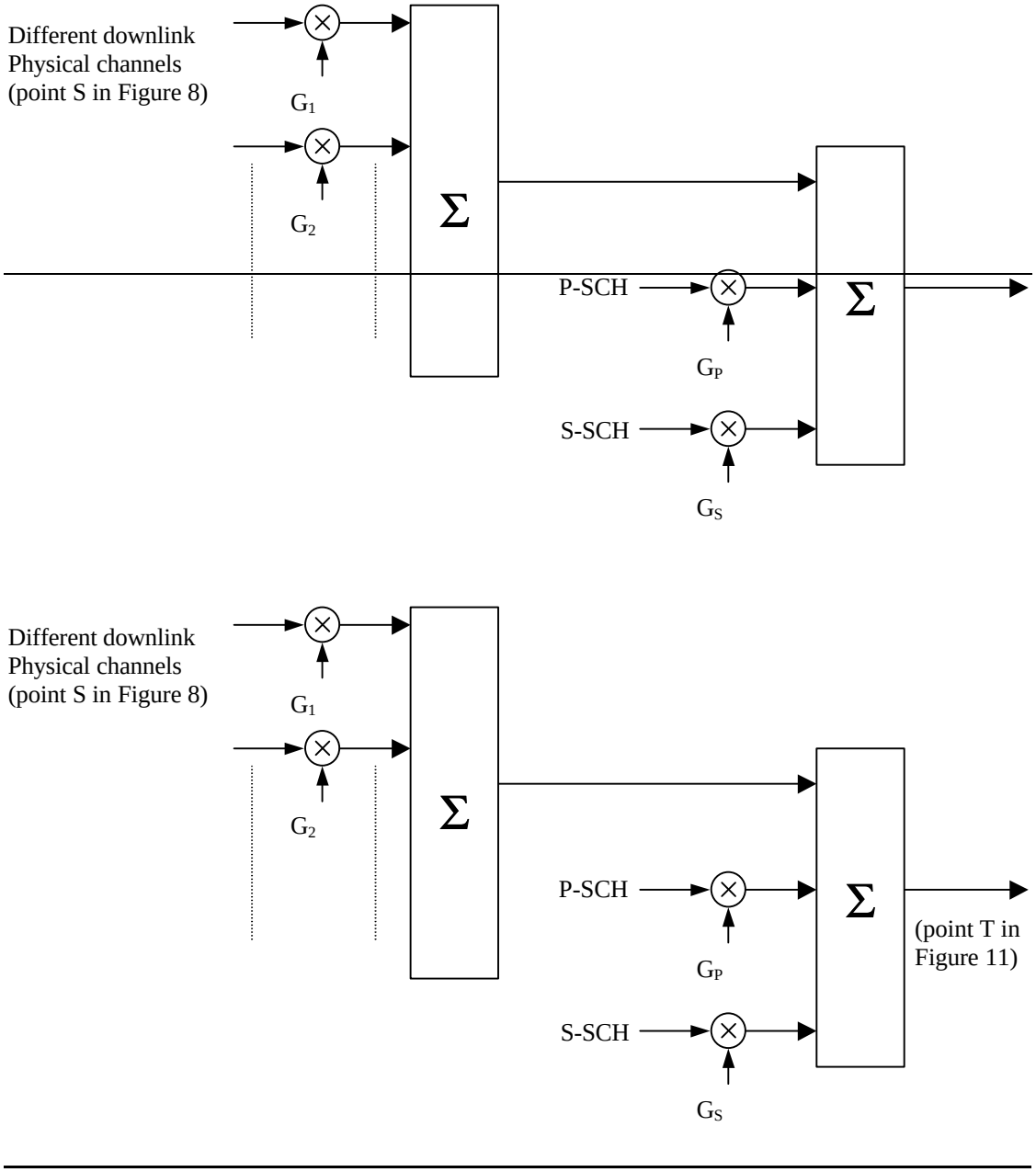

Figure 9: Spreading and modulation for SCH and P-CCPCH

5.3.2 Modulation

In the downlink, the complex-valued chip sequence generated by the spreading process is QPSK modulated as shown in Figure 11 below.

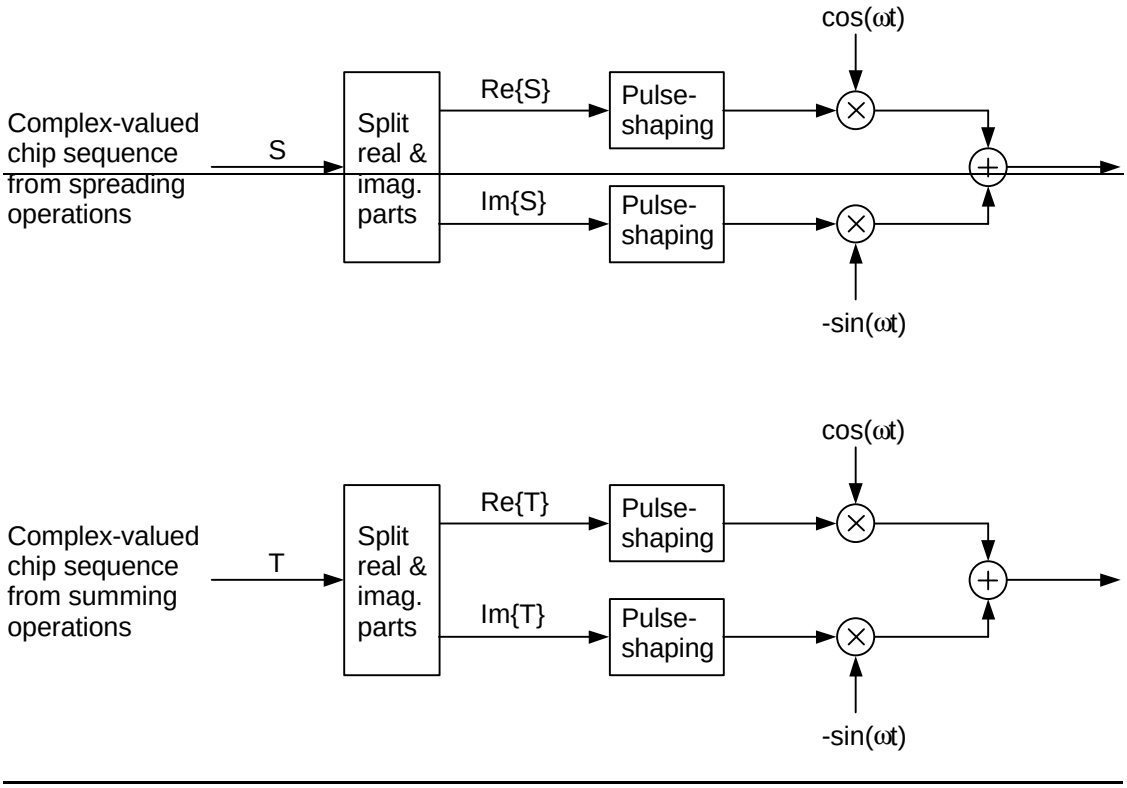

Figure 11: Downlink modulation.

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CHANGE REQUEST

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25.213	CR	022	Current Version:	3.1.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	RAN#7	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Siemens **Date:** 12-Jan-2000

Subject: Uplink signal flow corrections

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	X
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: Clarification of indication of signal flow between uplink block diagrams.
Change of notation for DPCH scrambling code to align with PCPCH notation which can also take long or short constituent codes.

Clauses affected: 3.2, 4.2, 4.2.2.2, 4.2.3.2, 4.3.2.4

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

<--------- double-click here for help and instructions on how to create a CR.

3.2 Symbols

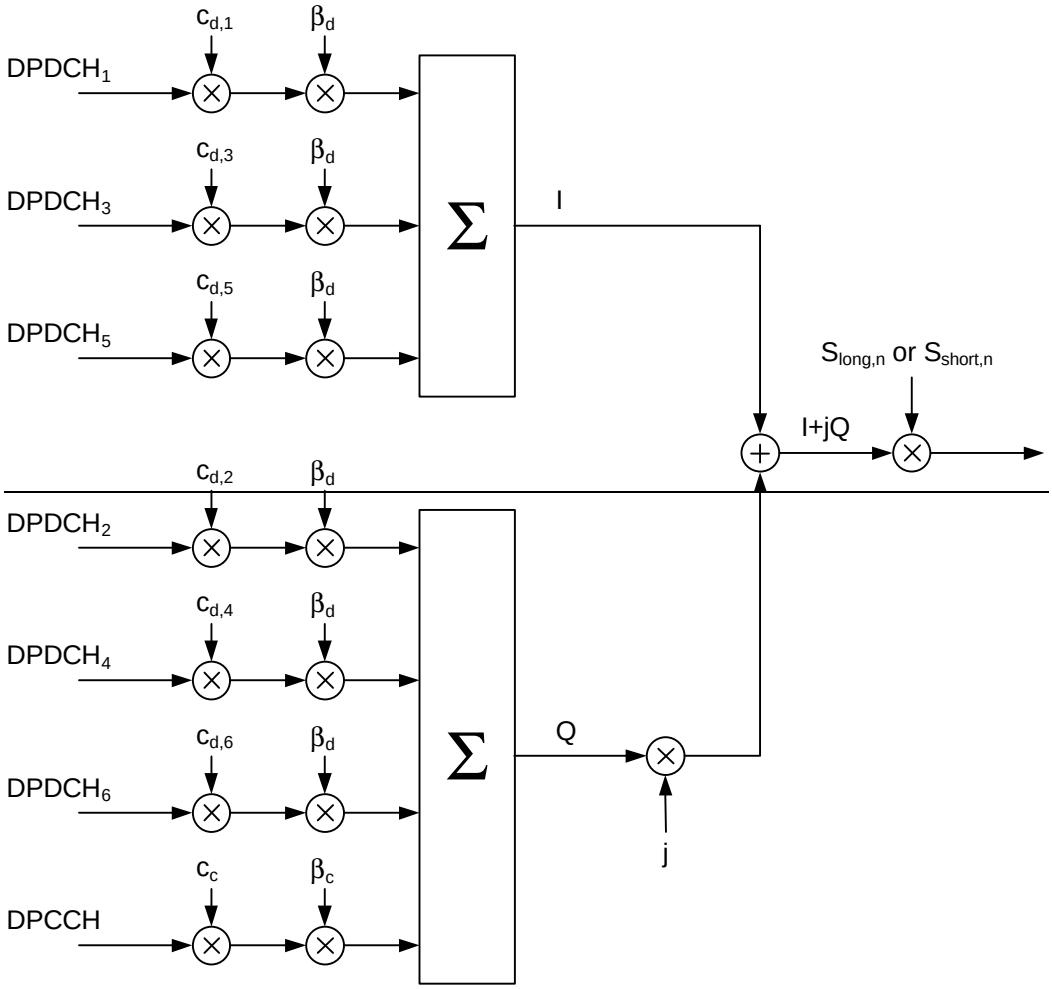
For the purposes of the present document, the following symbols apply:

$C_{ch,SF,n}$:	n:th channelisation code with spreading factor SF
$C_{pre,n,s}$:	PRACH preamble code for *n*:th preamble scrambling code and signature *s*
$C_{c\text{-}acc,n,s}$:	PCPCH access preamble code for *n*:th preamble scrambling code and signature *s*
$C_{c\text{-}cd,n,s}$:	PCPCH CD preamble code for *n*:th preamble scrambling code and signature *s*
$C_{sig,s}$:	PRACH/PCPCH signature code for signature *s*
$S_{dpch,n}$:	*n*:th DPCCH/DPDCH uplink scrambling code
~~$S_{long,n}$~~:	~~*n*:th DPCCH/DPDCH long uplink scrambling code~~
~~$S_{short,n}$~~:	~~*n*:th DPCCH/DPDCH short uplink scrambling code~~
$S_{r\text{-}pre,n}$:	*n*:th PRACH preamble scrambling code
$S_{r\text{-}msg,n}$:	*n*:th PRACH message scrambling code
$S_{c\text{-}acc}$:	*n*:th PCPCH access preamble scrambling code
$S_{c\text{-}cd}$:	*n*:th PCPCH CD preamble scrambling code
$S_{c\text{-}msg,n}$:	*n*:th PCPCH message scrambling code
$S_{dl,n}$:	DL scrambling code
C_{psc}:	PSC code
$C_{ssc,n}$:	n:th SSC code

4.2 Spreading

4.2.1 DPCCH/DPDCH)

Figure 1 illustrates the principle of the uplink spreading of DPCCH and DPDCHs. The binary DPCCH and DPDCHs to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The DPCCH is spread to the chip rate by the channelization code c_c, while the *n*:th DPDCH called $DPDCH_n$ is spread to the chip rate by the channelization code $c_{d,n}$. One DPCCH and up to six parallel DPDCHs can be transmitted simultaneously, i.e. $0 \le n \le 6$.


$c_{d,1}$
β_d
DPDCH$_1$
$c_{d,3}$
β_d
DPDCH$_3$
$c_{d,5}$
β_d
DPDCH$_5$
Σ
I
$S_{long,n}$ or $S_{short,n}$
I+jQ
$c_{d,2}$
β_d
DPDCH$_2$
$c_{d,4}$
β_d
DPDCH$_4$
$c_{d,6}$
β_d
DPDCH$_6$
c_c
β_c
DPCCH
Σ
Q
j

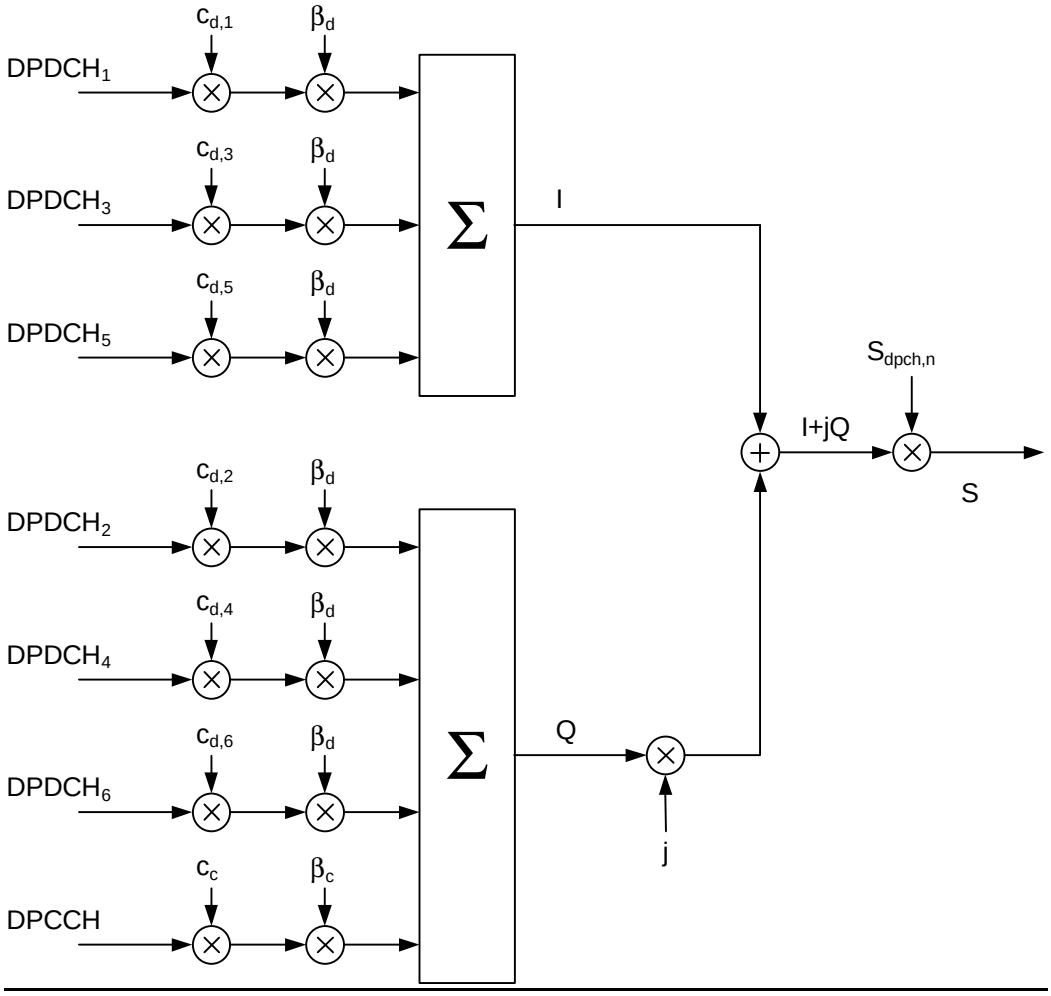


Figure 1: Spreading for uplink DPCCH and DPDCHs

After channelization, the real-valued spread signals are weighted by gain factors, β_c for DPCCH and β_d for all DPDCHs.

At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in table 1.

Table 1: The quantization of the gain parameters

Signalling values for β_c and β_d	Quantized amplitude ratios β_c and β_d
15	1.0
14	0.9333
13	0.8666
12	0.8000
11	0.7333
10	0.6667
9	0.6000
8	0.5333
7	0.4667
6	0.4000
5	0.3333
4	0.2667
3	0.2000
2	0.1333
1	0.0667
0	Switch off

After the weighting, the stream of real-valued chips on the I- and Q-branches are then summed and treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{longdpch,n}$ ~~or $S_{short,n}$, depending on if long or short scrambling codes are used~~. The scrambling code is applied aligned with the radio frames, i.e. the first scrambling chip corresponds to the beginning of a radio frame.

4.2.2 PRACH

4.2.2.1 PRACH preamble part

The PRACH preamble part consist of a complex-valued code, described in section 4.3.3.

4.2.2.2 PRACH message part

Figure 2 illustrates the principle of the spreading and scrambling of the PRACH message part, consisting of data and control parts. The binary control and data parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The control part is spread to the chip rate by the channelization code c_c, while the data part is spread to the chip rate by the channelization code c_d.

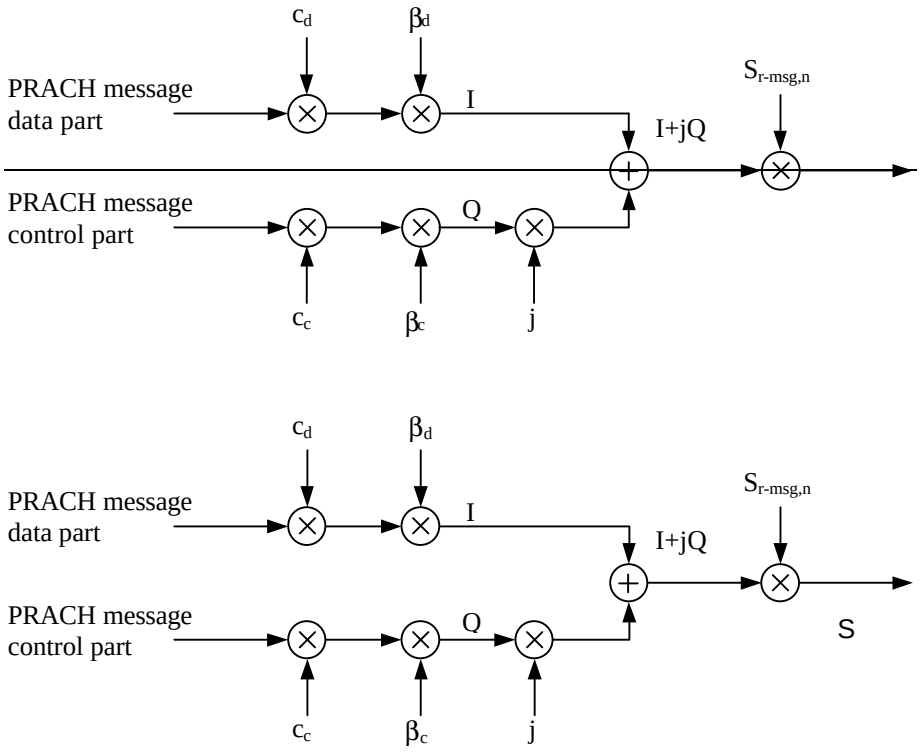


Figure 2: Spreading of PRACH message part

After channelization, the real-valued spread signals are weighted by gain factors, β_c for the control part and β_d for the data part. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in section 4.2.1.

After the weighting, the stream of real-valued chips on the I- and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{r\text{-}msg,n}$. The 10 ms scrambling code is applied aligned with the 10 ms message part radio frames, i.e. the first scrambling chip corresponds to the beginning of a message part radio frame.

4.2.3 PCPCH

4.2.3.1 PCPCH preamble part

The PCPCH preamble part consist of a complex-valued code, described in section 4.3.4.

4.2.3.2 PCPCH message part

Figure 3 illustrates the principle of the spreading of the PCPCH message part, consisting of data and control parts. The binary control and data parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The control part is spread to the chip rate by the channelization code c_c, while the data part is spread to the chip rate by the channelization code c_d.

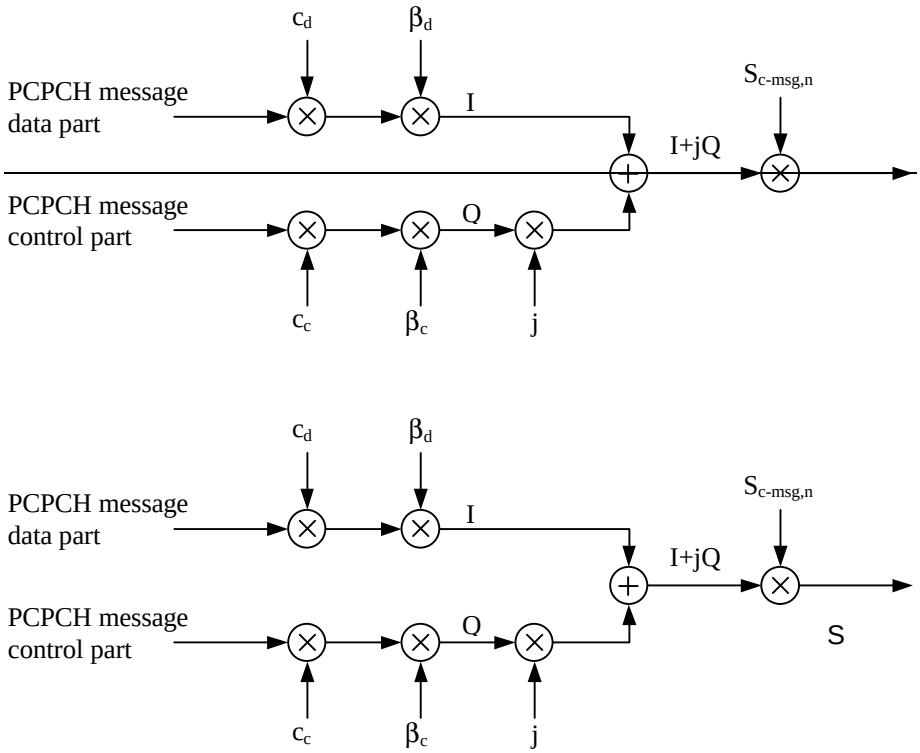


Figure 3: Spreading of PCPCH message part

After channelization, the real-valued spread signals are weighted by gain factors, β_c for the control part and β_d for the data part. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in section 4.2.1.

After the weighting, the stream of real-valued chips on the I- and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{c\text{-}msg,n}$. The 10 ms scrambling code is applied aligned with the 10 ms message part radio frames, i.e. the first scrambling chip corresponds to the beginning of a message part radio frame.

4.3.2.4 DPCCH/DPDCH scrambling code

The code used for scrambling of the uplink DPCCH/DPDCH may be of either long or short type. When the scrambling code is formed, different consituent codes are used for the long and short type as defined below.

The *n*:th ~~long~~ uplink scrambling code for DPCCH/DPDCH, denoted $S_{\text{~~long~~dpch},n}$, is defined as

$S_{\text{~~long~~dpch},n}(i) = C_{\text{long},n}(i)$, $i = 0, 1, \ldots, 38399$, when using long scrambling codes,

where the lowest index corresponds to the chip transmitted first in time and $C_{\text{long},n}$ is defined in section 4.3.2.2.

The *n*:th ~~short~~ uplink scrambling code for DPCCH/DPDCH, denoted $S_{\text{~~short~~dpch},n}$, is defined as

$S_{\text{~~short~~dpch},n}(i) = C_{\text{short},n}(i)$, $i = 0, 1, \ldots, 38399$, when using short scrambling codes,

where the lowest index corresponds to the chip transmitted first in time and $C_{\text{short},n}$ is defined in section 4.3.2.3.