3GPP TSG RAN WG1 ***TSGR1#10(00)0061***

January 18 – 21, 2000, Beijing, China

Source: **Philips**

To: **WG2**

Title: **Draft LS on Timing Parameters**

WG1 has identified 4 parameters in the Release '99 layer 1 specifications which need to be provided by higher layers for the purpose of defining timing and synchronisation requirements for the initialisation of Dedicated Channels.

These parameters are:

N_{offset_2} This is a UE-specific parameter which is an integer number of frames greater than or equal to zero, which allows higher layers to set the delay between the start of the downlink DPCCH and the start of the uplink DPCCH. N_{offset_2} is also described in section 7.7 of TS25.211.

S_{RU} This is an integer number of frames greater than or equal to zero, which must be less than or equal to N_{offset_2}. It allows higher layers to specify the number of frames which must be found to be frame synchronised before the UE reports Frame Synchonisation to higher layers using the Frame Synchronisation Word. This is described in CR25211-052, attached below.

S_{RN} This is an integer number of frames greater than or equal to zero. It allows higher layers to specify the number of frames which must be found to be frame synchronised before the UTRAN reports Frame Synchonisation to higher layers using the Frame Synchronisation Word. This is also described in CR25211-052.

N_{pcp} This is a UE-specific parameter which is used to signal a DPCCH power control preamble. It can take one of two values to signal a power control preamble of either 0 or 8 slots in length. It may be particularly useful for DCH packet transmission, when it is desirable to ensure that the inner-loop power control converges rapidly prior to the transmission of data on the data channel. N_{pcp} is described in section 7.7 of TS25.211 and section 5.1.2.4 of TS25.214, which is also attached below.

WG1 would like to ask WG2 to verify that its specifications provide for the communication of these parameters to layer 1.

Also, it is currently assumed that the parameters S_{RU} and S_{RN} are not UE specific, but this could be changed. Does WG2 have a view on this?

WG1 would also like to draw WG2's attention to the layer 1 parameter N_{offset_1} , which affects the delay between the end of the FACH frame relevant to the initialisation of the channel and the start of the downlink DPCCH, and which is derived from the activation time set by higher layers. However, section 7.7 of TS25.211 (attached below) specifies certain restrictions on the possible values of N_{offset_1}, in order to allow the UE time to decode the FACH frame. This therefore places restrictions on the useful range for the activation times set by higher layers.

WG1 thanks WG2 for their attention to this matter.

7.7 Timing relations for initialisation of channels

Figure 27 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be $T_{B\text{-}min}$ = 38400 chips (i.e.15 slots).

The downlink DPCCH shall commence at a time T_B after the end of the relevant FACH frame, where $T_B \geq T_{B\text{-}min}$ according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset\_1} \times 38400 \text{ chips}$$, where:

N_{pcp} is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], section 5.1.2.4).

N_{offset_1} is a parameter derived from the activation time set by higher layers. In order that $T_B \geq T_{B\text{-}min}$, N_{offset_1} shall be an integer number of frames such that:

$$N_{offset\_1} \geq \begin{cases} 1 \text{ when } T_n - T_k \geq \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 2 \text{ when } \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \leq T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 150 \\ 3 \text{ when } T_n - T_k < \frac{T_{B-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see section 7.1). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T_C after the end of the relevant FACH frame, where

$T_C = T_B + T_0 + N_{offset\_2} \times 38400$ chips, where T_0 is as in section 7.6.3 and N_{offset_2} is a UE-specific higher-layer parameter which shall be an integer number of frames greater than or equal to zero.

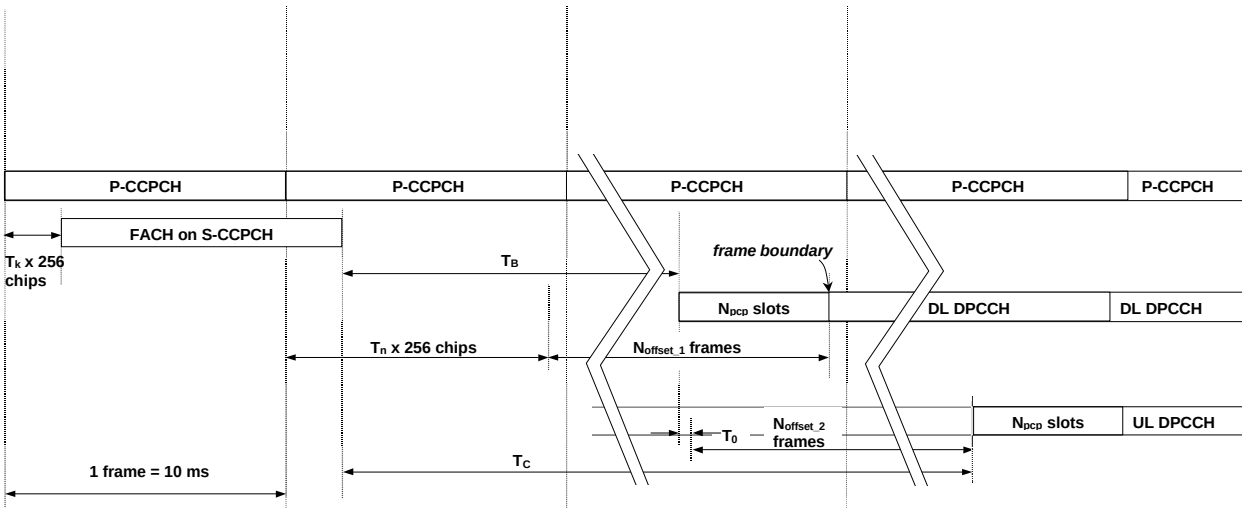

Figure 27: Timing for initialisation of DCH.

The data channels shall not commence before the end of the power control preamble.

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e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.214	CR	052	Current Version:	3.1.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #7	for approval	X	strategic		*(for SMG use only)*
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Philips **Date:** 2000-01-11

Subject: Synchronisation procedure

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction		**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature			Release 97	
C	Functional modification of feature	X		Release 98	
D	Editorial modification			Release 99	X
				Release 00	

Reason for change: Clarification of details relating to undefined S_r parameter.

Clauses affected: 4.3.2 "No existing uplink dedicated channel"
4.3.3 "With existing uplink dedicated channel"

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

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4 Synchronisation procedures

4.1 Cell search

During the cell search, the UE searches for a cell and determines the downlink scrambling code and common channel frame synchronisation of that cell. How cell search is typically done is described in Annex C.

4.2 Common physical channel synchronisation

The radio frame timing of all common physical channels can be determined after cell search. The P-CCPCH radio frame timing is found during cell search and the radio frame timing of all common physical channel are related to that timing as described in 25.211.

4.3 DPCCH/DPDCH synchronisation

4.3.1 General

The synchronisation of the dedicated physical channels can be divided into two cases:

- when a downlink dedicated physical channel and uplink dedicated physical channel shall be set up at the same time;
- or when a downlink dedicated physical channel shall be set up and there already exist an uplink dedicated physical channel.

The two cases are described in subclauses 4.3.2 and 4.3.3 respectively.

4.3.2 No existing uplink dedicated channel

The assumption for this case is that a DPCCH/DPDCH pair shall be set up in both uplink and downlink, and that there exist no uplink DPCCH/DPDCH already. This corresponds to the case when a dedicated physical channel is initially set up on a frequency.

The synchronization establishment procedures of the dedicated physical channel are described below. The synchronization establishment flow is shown in figure 1.

a) UTRAN starts the transmission of downlink DPCCH/DPDCHs. The DPDCH is transmitted only when there is data to be transmitted to the UE.

b) The UE establishes downlink chip synchronization and frame synchronization based on the CPICH timing and timing offset information notified from UTRAN. Frame synchronization can be confirmed using the Frame Synchronization Word. Successful frame synchronization ~~is~~ shall be confirmed and reported to the higher layers ~~when~~ if the first S_{RU} successive frames ~~have been~~are confirmed to be frame synchronized, where S_{RU} is a higher-layer parameter and S_{RU} N_{offset_2} (see subclause 7.7 in [1]). Frame synchronisation shall also be reported to higher layers in any case if $S_{RU} = 0$. Otherwise, frame synchronization failure ~~is~~ shall be reported to the higher layers.

c) The UE starts the transmission of the uplink DPCCH/DPDCHs at a frame timing exactly T_0 chips after the frame timing of the received downlink DPCCH/DPDCH. The DPDCH is transmitted only when there is data to be transmitted. The UE immediately starts inner-loop power control as described in sections 5.1.2 and 5.2.1, i.e. the transmission power of the uplink DPCCH/DPDCH follows the TPC commands generated by UTRAN, and the UE performs SIR estimation to generate TPC commands transmitted to UTRAN.

d) UTRAN establishes uplink channel chip synchronization and frame synchronization. Frame synchronization can be confirmed using the Frame Synchronization Word. Successful frame synchronization ~~is~~ shall be confirmed and reported to the higher layers ~~when~~ if the first S_{RN} successive frames ~~have been~~are confirmed to be frame synchronized, where S_{RN} is a higher-layer parameter. Frame synchronisation shall also be reported to higher layers in any case if $S_{RN} = 0$. Otherwise, frame synchronization failure ~~is~~ shall be reported to the higher layers.

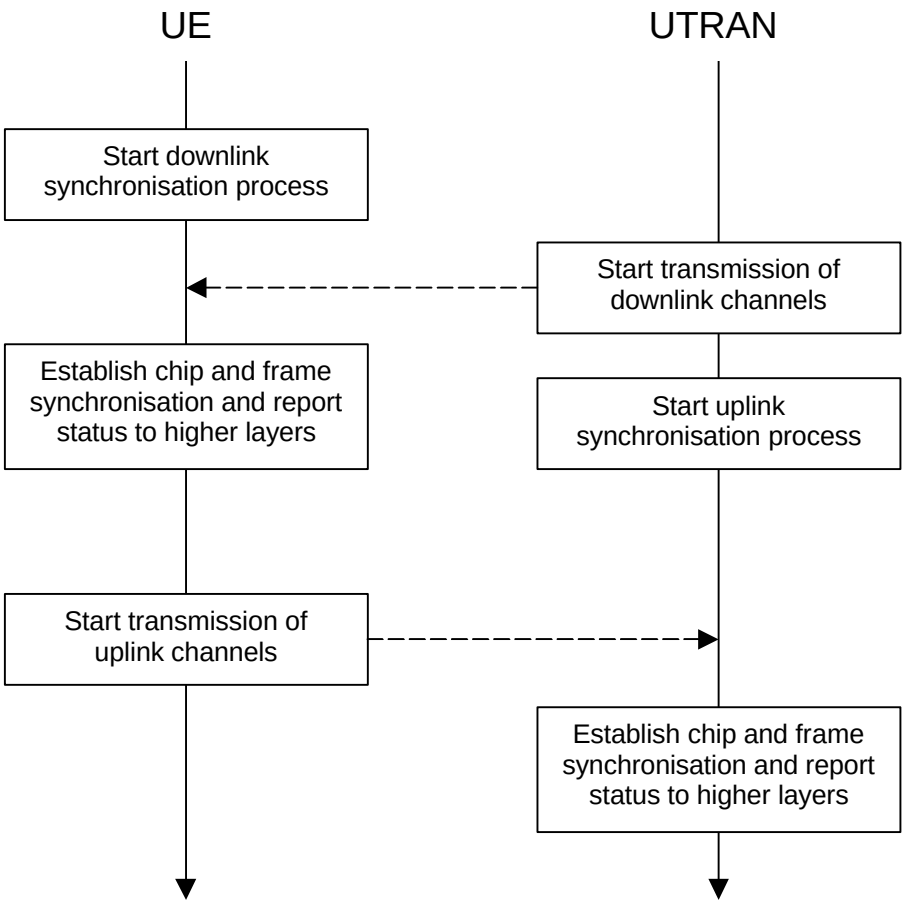

Figure 1: Synchronisation establishment flow for dedicated channels: uplink dedicated channel not existing

4.3.3 With existing uplink dedicated channel

The assumption for this case is that there already exist DPCCH/DPDCHs in the uplink, and a corresponding dedicated physical channel shall be set up in the downlink. This corresponds to the case when a new cell has been added to the active set in soft handover and shall begin its downlink transmission.

At the start of soft handover, the uplink dedicated physical channel transmitted by the UE, and the downlink dedicated physical channel transmitted by the soft handover source cell continues transmitting as usual.

The synchronisation establishment flow is described in figure 2.

a) The UE starts the chip synchronisation establishment process of downlink channels from the handover destination. The uplink channels being transmitted shall continue transmission as before.

b) UTRAN starts the transmission of the downlink DPCCH/DPDCH at a frame timing such that the frame timing received at the UE will be within $T_0 \pm 148$ chips prior to the frame timing of the uplink DPCCH/DPDCH at the UE. UTRAN then starts the synchronization establishment process of the uplink DPCCH/DPDCH transmitted by the UE. Frame synchronization can be confirmed using the Frame Synchronization Word. Successful frame synchronization ~~is~~ shall be confirmed and reported to the higher layers ~~when~~ if the first S_{RN} successive frames ~~have been~~are confirmed to be frame synchronized, where S_{RN} is a higher-layer parameter. Frame synchronisation shall also be reported to higher layers in any case if $S_{RN} = 0$. Otherwise, frame synchronization failure ~~is~~ shall be reported to the higher layers.

c) Based on the handover destination CPICH reception timing, the UE establishes chip synchronisation of downlink channels from handover destination cell. Frame synchronization can be confirmed using the Frame Synchronization Word. Successful frame synchronization ~~is~~ shall be confirmed and reported to the higher layers ~~when~~ if the first S_{RU} successive frames ~~have been~~are confirmed to be frame synchronized, where S_{RU} is a higher-layer parameter and S_{RU}

(see subclause 7.7 in [1]). Frame synchronisation shall also be reported to higher layers in any case if S_{RU} = 0. Otherwise, frame synchronization failure ~~is~~ shall be reported to the higher layers.

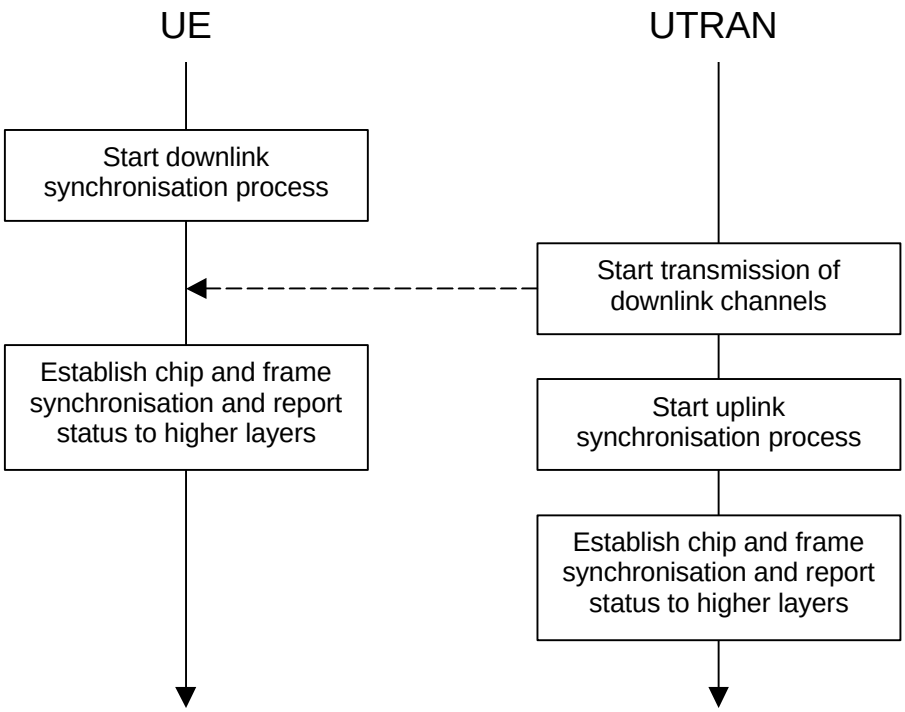

Figure 2: Synchronisation establishment flow for dedicated channels: uplink dedicated channel already existing

4.3.4 Transmission timing adjustments

During a connection the UE may adjust its DPDCH/DPCCH transmission time instant.

If the receive timing for any downlink DPCCH/DPDCH in the current active set has drifted, so the time between reception of the downlink DPCCH/DPDCH in question and transmission of uplink DPCCH/DPDCH lies outside the valid range, L1 shall inform higher layers of this, so that the network can be informed of this and downlink timing can be adjusted by the network.

NOTE: The maximum rate of uplink TX time adjustment, and the valid range for the time between downlink DPCCH/DPDCH reception and uplink DPCCH/DPDCH transmission in the UE is to be specified by RAN WG4.

5 Power control

5.1 Uplink power control

5.1.1 PRACH

5.1.1.1 General

The power control during the physical random access procedure is described in clause 6. The setting of power of the message control and data parts is described in the next sub-clause.

5.1.2.4 Transmit power control in DPCCH power control preamble

A power control preamble may be used for initialisation of a DCH. Both the UL and DL DPCCHs shall be transmitted during the uplink power control preamble. The UL DPDCH shall not commence before the end of the power control preamble.

The length of the power control preamble is a UE-specific parameter signalled by the network, and can take the values 0 slots or 8 slots.

The inner power control loop acts on the UL DPCCH during the preamble in the same way as described in section 5.1.2.2.1.

The initial power control step size used in the power control preamble differs from that used after the preamble in the following way. If algorithm 1 is to be used after the preamble to calculate the value of TPC_cmd, then the initial step size in the power control preamble is $\Delta_{TPC\text{-}init}$, where $\Delta_{TPC\text{-}init}$ is equal to the minimum value out of 3 dB and $2\Delta_{TPC}$. If algorithm 2 is to be used after the preamble to calculate the value of TPC_cmd, then initially in the power control preamble algorithm 1 is used with a step size of 2dB. In either case, the power control algorithm and step size revert to those used for the main part of the transmission as soon as the sign of TPC_cmd reverses for the first time, or at the end of the power control preamble if the power control preamble ends first.