TSG-RAN Working Group 1 meeting #10
Beijing, China
January 18 – 21, 2000

TSGR1#10(00)038

Agenda item:

Source: Ericsson

Title: CR 25.211-026: Minor corrections to timing section

Document for: Decision

There are two minor corrections needed in the timing section of TS 25.211 V3.1.0:

- In section 7.1, in figure 23, it says "PICH for n:th S-CCPCH". Since the corresponding S-CCPCH is called "k:th S-CCPCH", it is more correct to write "PICH for k:th S-CCPCH".

- In section 7.3, the preamble-to-message distance is incorrectly denoted $\tau_{p\text{-}a}$. The correct notation is $\tau_{p\text{-}m}$.

This CR updates the text in TS 25.211.

3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, Nov 30 -Dec 3, 1999

Document ????99???
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	026	Current Version:	3.1.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG-RAN #7	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source: Ericsson **Date:** 2000-01-12

Subject: Minor corrections to timing section

Work item:

Category: *(only one category shall be marked with an X)*			**Release:**	
F	Correction	X	Phase 2	
A	Corresponds to a correction in an earlier release		Release 96	
B	Addition of feature		Release 97	
C	Functional modification of feature		Release 98	
D	Editorial modification		Release 99	X
			Release 00	

Reason for change:
- In section 7.1, in figure 23, it says "PICH for n:th S-CCPCH". Since the corresponding S-CCPCH is called "k:th S-CCPCH", it is more correct to write "PICH for k:th S-CCPCH".
- In section 7.3, the preamble-to-message distance is incorrectly denoted $\tau_{p\text{-}a}$. The correct notation is $\tau_{p\text{-}m}$.

Clauses affected: 7.1, 7.3

Other specs affected:			
Other 3G core specifications		→ List of CRs:	
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

Other comments:

7 Timing relationship between physical channels

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 22 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Timing for uplink physical channels is given by the downlink timing, as described in the following sections.

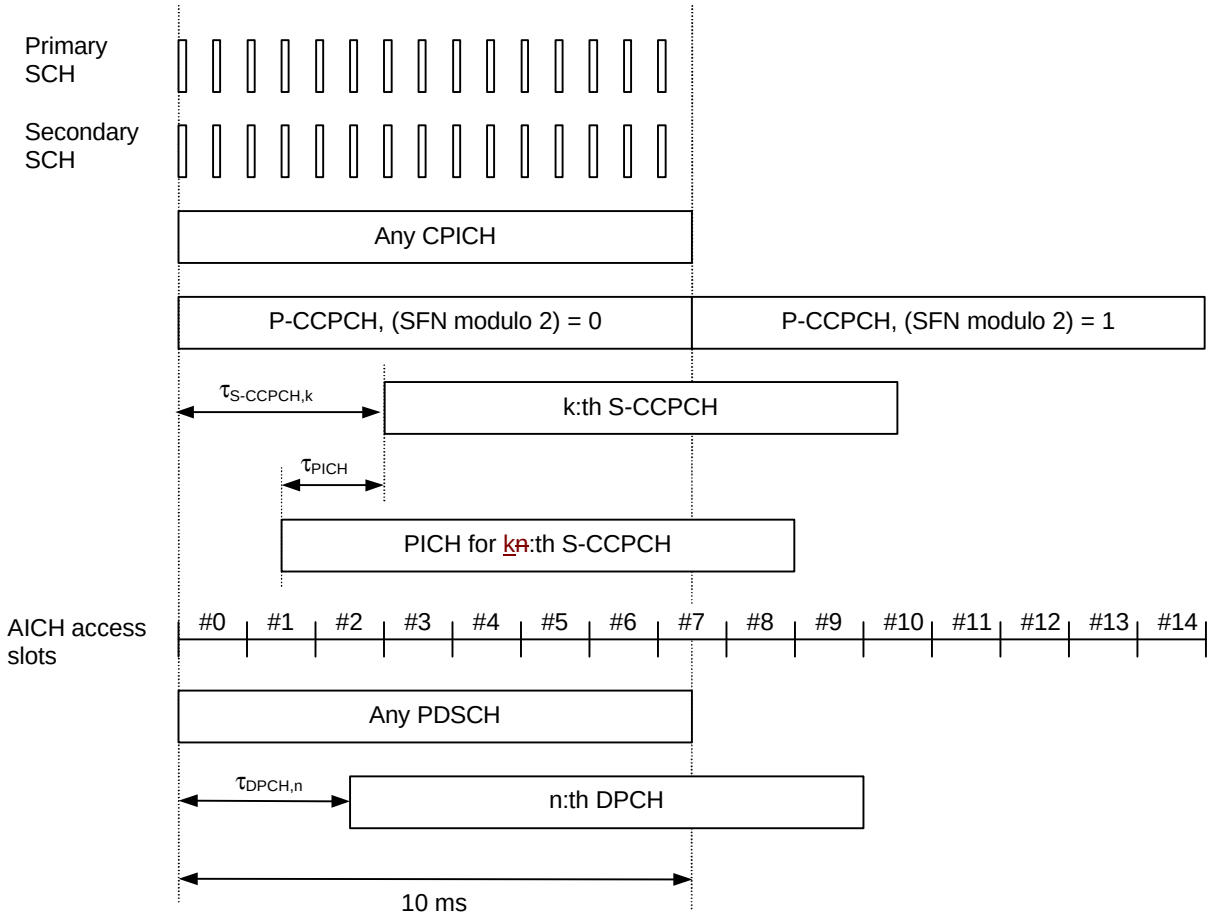

Figure 22: Frame timing and access slot timing of downlink physical channels

In figure 22 the following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.
- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{S\text{-}CCPCH,k} = T_k \times 256$ chip, $T_k \in \{0, 1, \ldots, 149\}$.
- The PICH timing is $\tau_{PICH} = 7680$ chips prior to its corresponding S-CCPCH frame timing. The PICH timing relation to the S-CCPCH is described more in section 7.2.
- The AICH access slot #0 starts the same time as a P-CCPCH frame with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in sections 7.3 and 7.4 respectively.
- The PDSCH timing relative the DPCH timing is described in section 7.5.

- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{DPCH,n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in section 7.6.

7.2 PICH/S-CCPCH timing relation

Figure 23 illustrates the timing between a PICH frame and its associated S-CCPCH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting τ_{PICH} chips after the transmitted PICH frame. τ_{PICH} is defined in section 7.1.

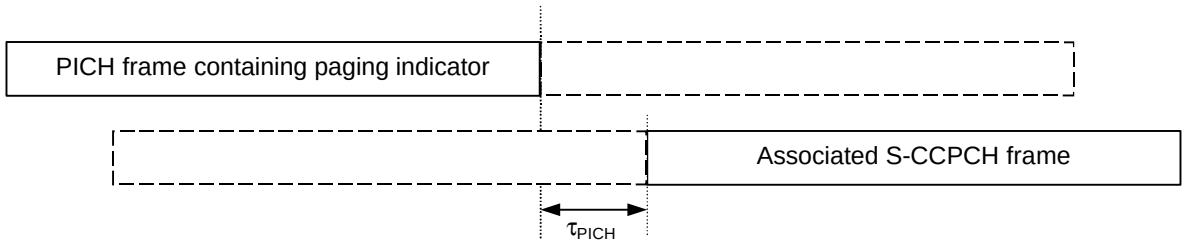

Figure 23: Timing relation between PICH frame and associated S-CCPCH frame

7.3 PRACH/AICH timing relation

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in section 7.1.

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number *n* is transmitted from the UE $\tau_{p\text{-}a}$ chips prior to the reception of downlink access slot number *n*, *n* = 0, 1, …, 14.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure 24.

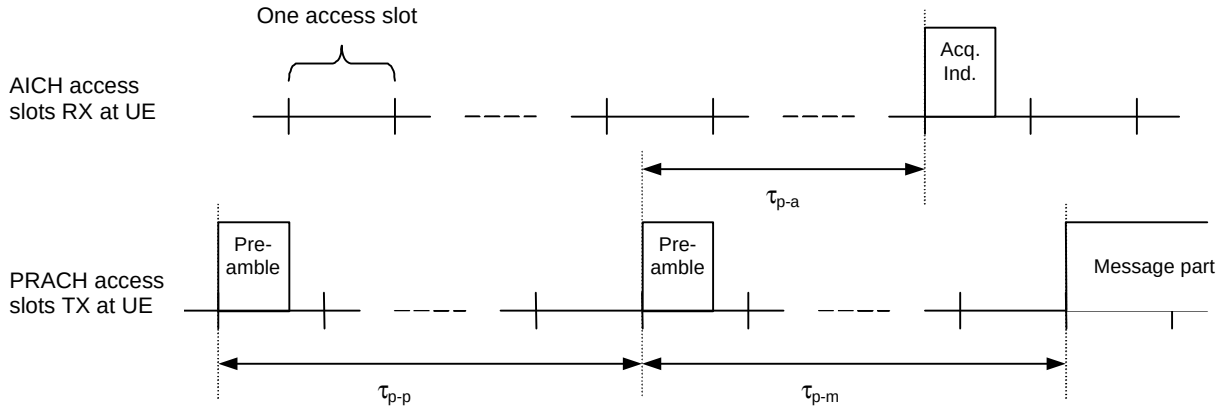

Figure 24: Timing relation between PRACH and AICH as seen at the UE

The preamble-to-preamble distance $\tau_{p\text{-}p}$ shall be larger than or equal to the minimum preamble-to-preamble distance $\tau_{p\text{-}p,min}$, i.e. $\tau_{p\text{-}p} \geq \tau_{p\text{-}p,min}$.

In addition to $\tau_{p\text{-}p,min}$, the preamble-to-AI distance $\tau_{p\text{-}a}$ and preamble-to-message distance $\tau_{p\text{-}m}$ are defined as follows:

- when AICH_Transmission_Timing is set to 0, then

  $\tau_{p\text{-}p,min}$ = 15360 chips (3 access slots)

  $\tau_{p\text{-}a}$ = 7680 chips

  $\tau_{p\text{-}m}$ = 15360 chips (3 access slots)

- when AICH_Transmission_Timing is set to 1, then

  $\tau_{p\text{-}p,min}$ = 20480 chips (4 access slots)

  $\tau_{p\text{-}a}$ = 12800 chips

  $\tau_{p\text{-}m}$ = 20480 chips (4 access slots)