TSGR1#9(99)j78

TSG-RAN Working Group 1 meeting #9 Dresden, Germany

Agenda item:	AH16
Source:	NTT DoCoMo
Title:	A scheme to measure quality for outer loop TPC during DPDCH OFF
Document for:	Decision

1. Introduction

It was accepted in the WG1 that physical channel BER on DPCCH is used for outer loop TPC during DPDCH OFF. This document explained that physical channel BER on DPCCH is not suitable for outer loop TPC, and proposes to transmit parity bits for error detection during DPDCH OFF.

2. The problem in the physical channel BER on DPCCH for outer loop TPC

Figure 1 shows correspondences between the physical channel BER on DPCCH and BER after decoding. The number of path is a parameter in figure 1. Simulation conditions are as following:

- Antenna space diversity: 2-branch
- Rake combining: n-finger/branch
- Channel estimation: 3-slot averaging with power weighting i.e. 0.4:1:0.4
- Channel coding: Turbo coding (R=1/3, k=4)
- Transmit Power Control (TPC): Slot base closed loop power control (1-slot control delay, 1dB step size, no-control command error)
- Channel model: N-path Rayleigh fading channel (each path with equal average power).

As figure 1 shows, correspondences between the physical channel BER on DPCCH and BER after decoding are not stable against the number of path. This means that the outer loop TPC using the physical channel BER on DPCCH cannot follow fluctuation of the number of paths. Consequently, the physical channel BER on DPCCH seems not to be appropriate as a quality indication for outer-loop TPC. Other quality indication for outer loop TPC, which can be measured in short time, is needed.

3. Proposal

This document proposes to delete the physical channel BER on DPCCH and to add a feature to transmit parity bits during DPDCH OFF. The parity bits attachment is done instead of CRC bits attachment before encoding. During DPDCH OFF, BLER can be measured using proposed parity bits.

In each transport channel, length of the parity bits is same as length of CRC bits used during DPDCH ON.

Transport channels, which are not applied outer loop TPC, should be considered, e.g. a transport channel to transmit very infrequent traffic. Therefore, higher layer signalling should designate UE use of proposed parity bits for each transport channel.

Error detection results of proposed parity bits in node B are transmitted to RNC on the field of CRC check results in Iub interface instead of CRC check results.

4. Conclusion

In this document, simulation results of correspondences between the physical channel BER on DPCCH and BER after decoding is presented. From these results, this document explains that the physical channel BER on DPCCH is not appropriate for outer loop TPC during DPCCH OFF. Instead of the physical channel BER on DPCCH, transmission of parity bits during DPDCH OFF is proposed to measure BLER during DPDCH OFF.

In attached text proposal, it is proposed to add parity bits patterns in TS25.212.

A LS to R2 is needed to inform R2 of the necessity of additional signaling to designate UE use of parity bits during DPCCH OFF for each transport channel.

A LS to R3 is needed to inform R3 that a field for results of CRC checksum is used for parity check results during DPDCH OFF, also.

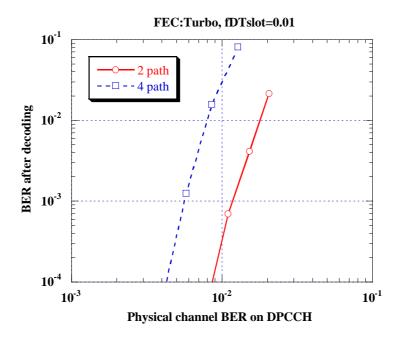


Figure 1: Correspondences between the physical channel BER on DPCCH and BER after decoding

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4.2.1 Error detection

Error detection is provided on transport blocks through a Cyclic Redundancy Check. The CRC is 24, 16, 12, 8 or 0 bits and it is signalled from higher layers what CRC length that should be used for each TrCH.

4.2.1.1 CRC Calculation

The entire transport block is used to calculate the CRC parity bits for each transport block. The parity bits are generated by one of the following cyclic generator polynomials: $g_{CRC24}(D) = D^{24} + D^{23} + D^6 + D^5 + D + 1$

$$\begin{split} g_{CRC16}(D) &= D^{16} + D^{12} + D^5 + 1 \\ g_{CRC12}(D) &= D^{12} + D^{11} + D^3 + D^2 + D + 1 \\ g_{CRC8}(D) &= D^8 + D^7 + D^4 + D^3 + D + 1 \end{split}$$

Denote the bits in a transport block delivered to layer 1 by $a_{im1}, a_{im2}, a_{im3}, \dots, a_{imA_i}$, and the parity bits by

 $p_{im1}, p_{im2}, p_{im3}, \dots, p_{imL_i}$. A_i is the length of a transport block of TrCH *i*, *m* is the transport block number, and L_i is 24, 16, 12, 8, or 0 depending on what is signalled from higher layers. The encoding is performed in a systematic form, which means that in GF(2), the polynomial

 $a_{im1}D^{A_i+23} + a_{im2}D^{A_i+22} + \ldots + a_{imA_i}D^{24} + p_{im1}D^{23} + p_{im2}D^{22} + \ldots + p_{im23}D^1 + p_{im24}$ yields a remainder equal to 0 when divided by $g_{CRC24}(D)$, polynomial

 $a_{im1}D^{A_i+15} + a_{im2}D^{A_i+14} + \dots + a_{imA_i}D^{16} + p_{im1}D^{15} + p_{im2}D^{14} + \dots + p_{im15}D^{1} + p_{im16}$

yields a remainder equal to 0 when divided by $g_{CRC16}(D)$, polynomial $a_{im1}D^{A_i+11} + a_{im2}D^{A_i+10} + ... + a_{im4}D^{12} + p_{im1}D^{11} + p_{im2}D^{10} + ... + p_{im11}D^1 + p_{im12}$

yields a remainder equal to 0 when divided by g_{CRC12}(D) and polynomial

 $a_{im1}D^{A_i+7} + a_{im2}D^{A_i+6} + \ldots + a_{imA_i}D^8 + p_{im1}D^7 + p_{im2}D^6 + \ldots + p_{im7}D^1 + p_{im8}$

yields a remainder equal to 0 when divided by $g_{CRC8}(D)$.

4.2.1.1.1 Parity bits for zero length transport block

The parity attachment when no bits in a transport block ($A_i = 0$) are input to the CRC attachment is as follows. If the execution of the error detection for zero length transport block is signaled from higher layer, fixed bit patterns indicated in Table X are used as the parity bit pattern for each parity length. These parity bit patterns are same as CRC parity bit pattern for all "1" bit sequence which length is L_i . Otherwise no parity bits are attached in CRC attachment, i.e. B_i (see 4.2.1.1.2) = 0.

Number of CRC parity bits L _i	Parity bit pattern $\{p_{im1}, p_{im2}, p_{im3}, K, p_{imL_3}\}$
<u>8</u>	$\{0,1,1,1,1,0,1,1\}$
<u>12</u>	$\{0,0,0,0,0,0,1,1,1,0,1,0\}$
<u>16</u>	$\{0,0,0,1,1,1,0,1,0,0,0,0,1,1,1,1\}$
<u>24</u>	$\underline{\{1,0,0,0,0,0,0,0,0,0,0,0,1,1,1,1,1,1,1,0,0,0,1,1\}}$

Table X: Parity bit pattern for zero length transport block

4<mark>.2.1.1.1<u>4.2.1.1.2</u> Check</mark>

Relation between input and output of the Cyclic Redundancy

The bits after CRC attachment are denoted by $b_{im1}, b_{im2}, b_{im3}, \dots, b_{imB_i}$, where $B_i = A_i + L_i$. The relation between a_{imk} and b_{imk} is:

 $b_{imk} = a_{imk} \qquad k = 1, 2, 3, ..., A_i$ $b_{imk} = p_{im(L_i+1-(k-A_i))} \qquad k = A_i + 1, A_i + 2, A_i + 3, ..., A_i + L_I$