3GPP TSG-RAN WG1#9
Dresden, Germany, 30 Nov.-3 Dec. 1999

TSGR1#9(99)J68

Agenda Item:

Source: Samsung Electronics Co.

Title: Text Proposal of Gated DPCCH Transmission in 25.214

Document for Discuss and approve

1. Introduction

1.1 In last WG2#8 Cheju meeting[1], gated DPCCH transmission was accepted as it is proposed for Release 99 as an option in case of up link for UE and UTRAN with limitations such that the gated transmission should never be used in cases where the UEs operate at maximum power (near the cell edge). A liaison response was sent to WG1[2].

1.2 In WG4#8 Sophia Antipolis meeting[3], WG4 understood that gated DPCCH transmission has some benefits of UL/DL interference reduction, UL/DL capacity increase and UE battery life expansion in case of packet transmission, and WG4 decided to await the decision of WG1 on gated DPCCH and to adopt it if this gated DPCCH transmission is agreed in WG1[4].

1.3 In WG1#7 Hannover meeting[5] the gated DPCCH concept became working assumption. Since then, the only remaining concern regarding gated DPCCH is the EMC effects to the hearing aid apparatus. In WG1#7bis Kyongju meeting, Mitsubishi[6] has shown the possibility of random gating concept to avoid the EMC effects, and Samsung[7] proposed a specific random gating pattern generation method, but it was not approved at the meeting because the algorithm was not presented quite well. In WG1#9 Dresden meeting, Samsung[8] will revise the random gating pattern generation method.

2. References

[1] TSGR2#9(99)g88, “Draft minutes of WG2 meeting #8” Cheju, Korea, 2-5, Nov. 1999.

[2] TSGR1#9(99)i27 (TSGR2#8(99)g67), “Response (to TSG-RAN WG1, TSG-RAN WG4) to LS on Gated DPCCH transmission,” WG2, Cheju, 2-5 Nov. 1999.

[3] TSGR4#8(99)779, “Report of the 8th TSG-RAN WG4 meeting (Draft report),” Sophia Antipolis, 26-29, Oct. 1999.

[4] TSGR4#8(99)751, “Proposed Response to Liaison Statement on impact of gated DPCCH at cell boundaries,” Sophia Antipolis, 26 - 29 Oct 1999.

[5] 3GPP RAN TS 25.214 v1.3.0(1999-09)

[6] TSGR1#8(99)f43, “Reducing EMC problem in uplink DPCCH Gated mode,” Mitsubishi, New York, 12-15 Oct. 1999.

[7] TSGR1#8(99)g54, “Revised Random Pattern for DPCCH Gated Transmission (Rev. of R1-99f80),” Samsung, New York, 12-15, Oct. 1999.

[8] TSGR1#9(99)j51, “Random Pattern for Gated DPCCH transmission,” Dresden, 30 Nov. – 3 Dec. 1999

3. Contact Persons

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***Document* R1-99J68**
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.214 **CR** **028** Current Version: v3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to: RAN #6 *list expected approval meeting # here ↑*

for approval [X] for information [ ]

strategic [ ] non-strategic [ ] *(for SMG use only)*

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)* (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]

Source: Samsung **Date:** 1 Dec 1999

Subject: Text Proposal of Gated DPCCH Transmission in 25.214

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	X
C	Functional modification of feature	
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: In packet transmission mode, gated DPCCH transmission can increase the UE battery life and downlink/uplink capacity.

Clauses affected: 7.2

Other specs affected:

Other 3G core specifications	[ ]	→ List of CRs:
Other GSM core specifications	[ ]	→ List of CRs:
MS test specifications	[ ]	→ List of CRs:
BSS test specifications	[ ]	→ List of CRs:
O&M specifications	[ ]	→ List of CRs:

Other comments:

<--------- double-click here for help and instructions on how to create a CR.

7.2 Gated DPCCH Transmission in Packet Transmission Mode

7.2.1 General

In packet transmission mode, UE and UTRAN stop transmission of DPDCH frame if there is no data to transmit while continuing transmission of DPCCH. If the gated transmission is enabled, then DPCCH frame shall be gated-on in specified time slots to reduce the transmission rate of Pilot, TPC, TFCI, and FBI (uplink only). UE shall report the capability of gating such as gating rate, gating pattern, and direction of gating to UTRAN when needed, then UTRAN shall determine appropriate gating parameter values. The combinations of parameters needed to be negotiated between UTRAN and UE are given in 7.2.2. In 7.2.2, the required operations of UE when the gating operation is permitted only for downlink are also described. When there is urgent signalling messages, for example, handover control or measurement message etc., to be transmitted during gated transmission, the signalling message is transmitted on DPDCH without returning to non-gating mode. When only the DPCCH is transmitted in packet transmission mode, the UTRAN and UE shall gate off all time slots other than the specific time slots defined in 7.2.3. When transmitting DPDCH during gated transmission mode, the UTRAN and UE shall gate off time slots other than specific time slots defined in 7.2.4.

7.2.2 Combination of Gating Operation Mode

UTRAN and UE negotiate the combination of gating operation parameters when needed. The parameters required to be negotiated are gating rate, gating pattern, and direction as follows.

Gating Rate	1	1/3	1/5

Gating Pattern	Random	Regular

Direction	Downlink Only	Uplink and Downlink

If the gating transmission is disabled (i.e., gating rate = 1), then the regular gating pattern shall be used. In the case where gated DPCCH transmission is used only for the downlink, then UE shall transmit the DPCCH in every time slots, and UE shall:

- adjust the transmit power in response to the valid downlink TPC, where valid downlink TPC means the downlink TPC transmitted at the gated-on slots
- ignore any downlink TPC that are received during the gated off slot, and the downlink transmit power shall remain constant
- generate and transmit uplink TPC based on the downlink symbols if the time slot is associated with the downlink gate-on slot
- repeat the previous uplink TPC if the time slot is associated with the downlink gate-off slot

7.2.3 Gated DPCCH Transmission

7.2.3.1 DPCCH Random Gating Pattern Generation

If the gated DPCCH transmission is enabled with random gating pattern, the downlink and uplink gating pattern shall be determined based on the parameters in Table 1.

Table 1. Parameters for Random Gating Pattern

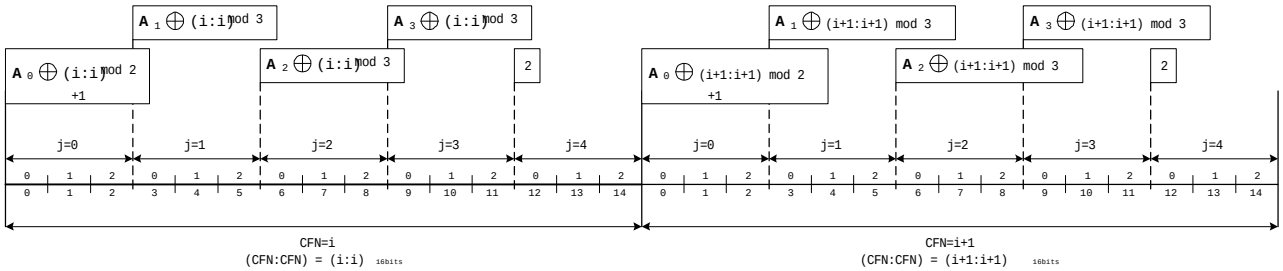
Parameter	Value
CFN	0, 1, …, 255 (8bits)
gating rate	1/3 or 1/5
number of gating group(N_G)	5, if gating rate is 1/3 3, if gating rate is 1/5
gating group size (S_G)	3, if gating rate is 1/3 5, if gating rate is 1/5
A=(a_0,a_1,…,a_{18})	1011010011011101001 (19bits)

CFN is a frame counter ranged from 0 to 255. The number of gating group (N_G) represents the number of gating groups in a frame. Each gating group consists of S_G (gating group size) consecutive time slots, which is the number of slots in a gating group. Let i be the CFN of the frame (i=0,1,…,255) and j be the j^{th} gating group, respectively, then the allocated

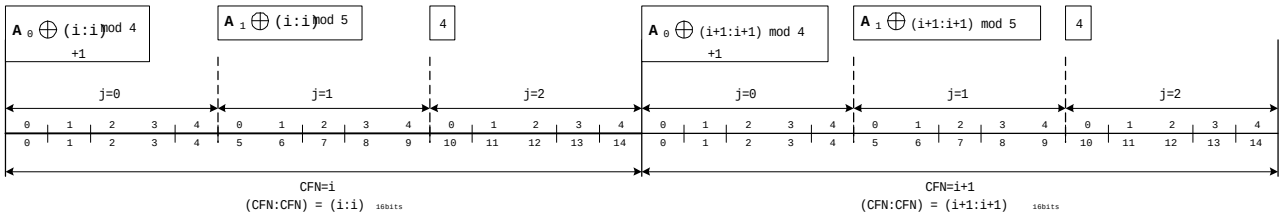
time slot, s(i,j), shall be given by

$$s(i,j)=\begin{cases}(A_j \oplus C_i)_{10} \bmod (S_G-1)+1, & j=0\\ (A_j \oplus C_i)_{10} \bmod S_G, & j=1,\cdots,N_G-2\\ S_G-1, & j=N_G-1\end{cases}\Bigg\}, \quad i=0,1,\cdots,255$$

where $A_j=(a_j, a_{j+1},...,a_{j+15})$, j=0,1,...,$N_G$-2, is a 16bit sequence constructed from sequence A in Table 1, and $C_i=((CFN)_2, (CFN)_2)$ is a 16bits sequence consists of repeated binary representation of 8 bits CFN, where $(x)_m$ represents the m-ary representation of x. Note that the first time slot (slot #0) shall never be allocated to s(i,j) (the case of j=0), and the last time slot (slot #14) shall always be allocated to s(i,j) (the case of j=N_G-1). Figure 1 describes the method of calculation s(i,j).



(a) s(i,j) of 1/3 rate gating



(b) s(i,j) of 1/5 rate gating

Figure 1. Calculation of s(i,j): (a) 1/3 rate (b) 1/5 rate

7.2.3.2 Gated-on Slot Allocation in Gated DPCCH Transmission

When the gated transmission mode is enabled in downlink and uplink, the UTRAN and UE shall transmit the DPCCH in the time slots specified in Table 2 and Table 3. When the random gating pattern is used, the gate-on time slots shall be allocated as specified in 7.2.3.1. Only one slot per each gating group shall be permitted to be gated-on.

Table 2 : Downlink DPCCH gate on time slot allocations during gated transmission mode enabled

Gating Pattern	Gating Rate	Downlink DPCCH gate on time slot allocation	
		Pilot	TPC, TFCI
Regular Pattern	1	every time slots (0~14)	every time slots (0~14)
Regular Pattern	1/3	$j\times 3$	$1+j\times 3$
	1/5	$1+j\times 5$	$2+j\times 5$
Random Pattern	1/3	$j\times S_G+s(i,j)-1$ (defined in 7.2.3.1)	$j\times S_G+s(i,j)$ (defined in 7.2.3.1)
	1/5		

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number. (defined in 7.2.3.1)

Table 3 : Uplink DPCCH gate on time slot allocations during gated transmission mode enabled

Gating Pattern	Gating Rate	Uplink DPCCH gate on time slot allocation
		Pilot, TFCI, FBI, TPC

Regular Pattern	1	every time slots (0~14)
Regular Pattern	1/3	$2+j\times S_G$
	1/5	$4+j\times S_G$
Random Pattern	1/3	$j\times S_G+s(i,j)$ (defined in 7.2.2.1)
	1/5	

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number. (defined in 7.2.3.1)

The relative timings of the downlink and uplink DPCCH transmission with random and regular gating pattern are depicted in Figure 2, Figure 3, respectively.

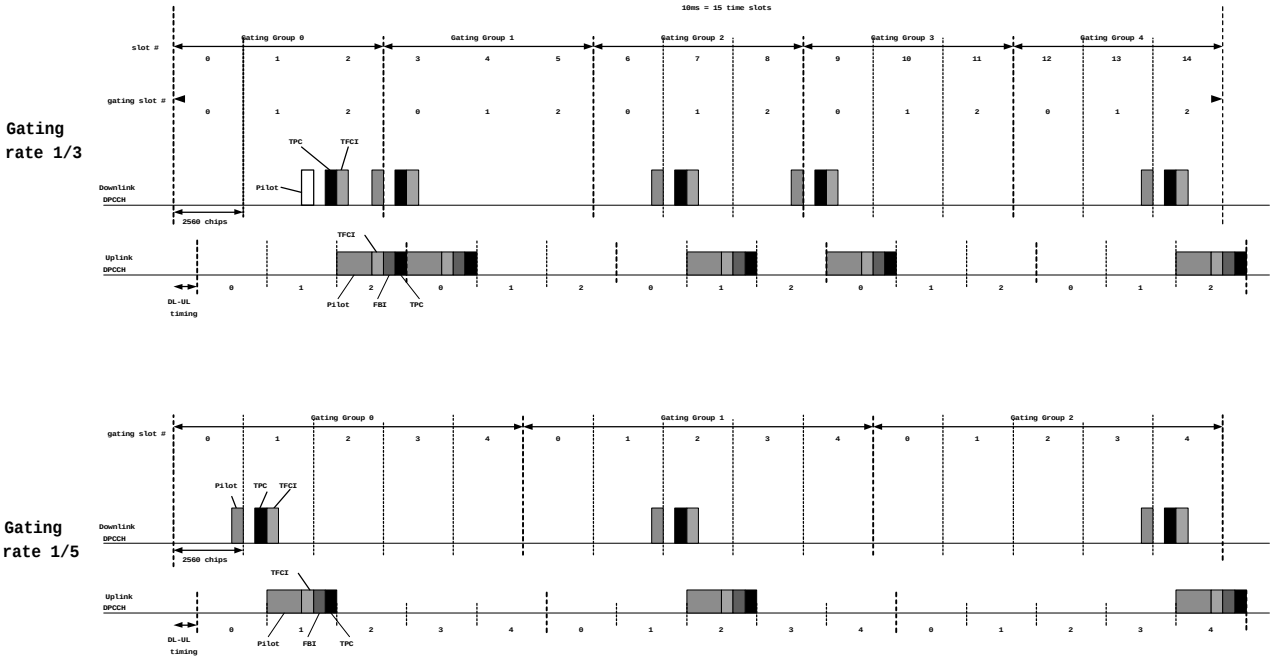


Figure 2. Downlink and uplink DPCCH transmission with random gating pattern (example)

[Note: Downlink slot structure in Figure 1 is based on the figure agreed through e-mail discussion between WG1#8 and WG1#9 meetings.]

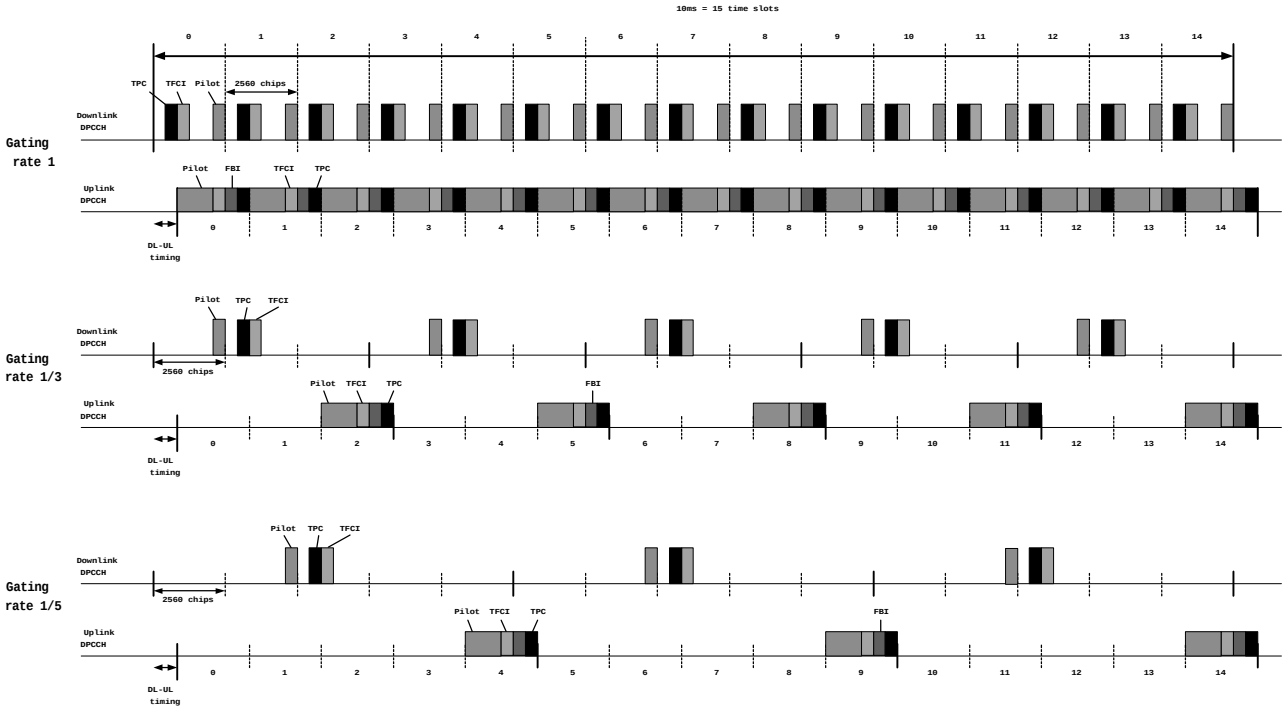


Figure 3 : Downlink and uplink DPCCH transmission timing with regular gating pattern

[Note: Downlink slot structure in Figure 1 is based on the figure agreed through e-mail discussion between WG1#8 and WG1#9 meetings.]

7.2.4 Gated DPCCH Transmission with Signalling Messages

When the downlink and uplink signalling message is transmitted during gated transmission in packet transmission mode, the gating patterns are specified in Table 4 and Table 5. Note that during downlink signalling message transmission, the TFCI and Pilot shall be transmitted in every time slots, but TPC shall be gated on only for specific time slots as specified in Table 4. During uplink signalling message transmission, the Pilot, TFCI, and FBI shall be transmitted in every time slots, but TPC shall be gated on only for specific time slots as specified in Table 5.

Table 4 : Downlink DPCCH gate on time slot allocations during signalling message transmission

Gating Pattern	Gating Rate	Downlink DPCCH gate on time slot allocation	
		TFCI, Pilot	TPC
Regular Pattern	1	every time slots (0~14)	every time slots (0~14)
Regular Pattern	1/3	every time slots (0~14)	$1+j\times 3$
	1/5	every time slots (0~14)	$2+j\times 5$
Random Pattern	1/3	every time slots (0~14)	$j\times S_G + s(i,j)$ (defined in 7.2.3.1)
	1/5	every time slot (0~14)	

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number. (defined in 7.2.3.1)

Table 5 : Uplink DPCCH gate on time slot allocations during signalling message transmission

Gating Pattern	Gating Rate	Uplink DPCCH gate on time slot allocation	
		Pilot, TFCI, FBI	TPC
Regular Pattern	1	every time slots (0~14)	every time slots (0~14)
Regular Pattern	1/3	every time slots (0~14)	$2 + j \times 3$
	1/5	every time slots (0~14)	$4 + j \times 5$
Random Pattern	1/3	every time slots (0~14)	$j \times S_G + s(i, j)$ (defined in 7.2.3.1)
	1/5	every time slots (0~14)	

* Note: i=0,1,...,255 denotes the CFN and j=0,1,2,3,4 if gating rate is 1/3, j=0,1,2 if gating rate is 1/5 denotes the gating group number. (defined in 7.2.3.1)

The DPCCH gating during signalling message transmission for downlink and uplink are depicted in Figure 4 and Figure 5, respectively, when the regular gating pattern is used.

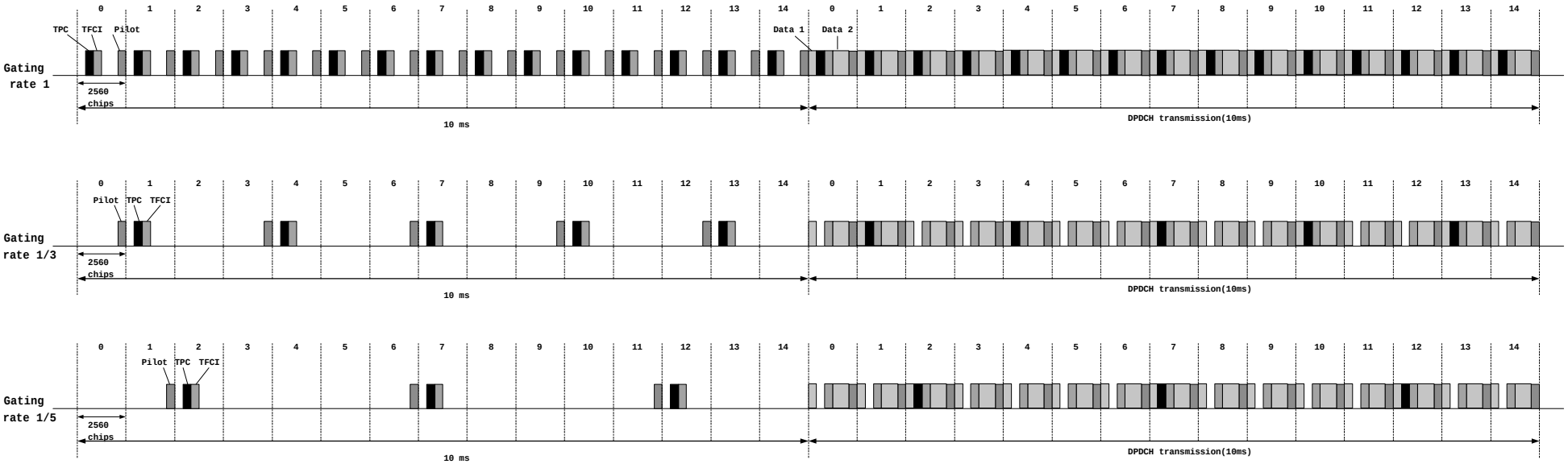


Figure 4 : Downlink DPCCH gating with regular gating pattern during signalling message transmission

[Note: Downlink slot structure in Figure 1 is based on the figure agreed through e-mail discussion between WG1#8 and WG1#9 meetings.]

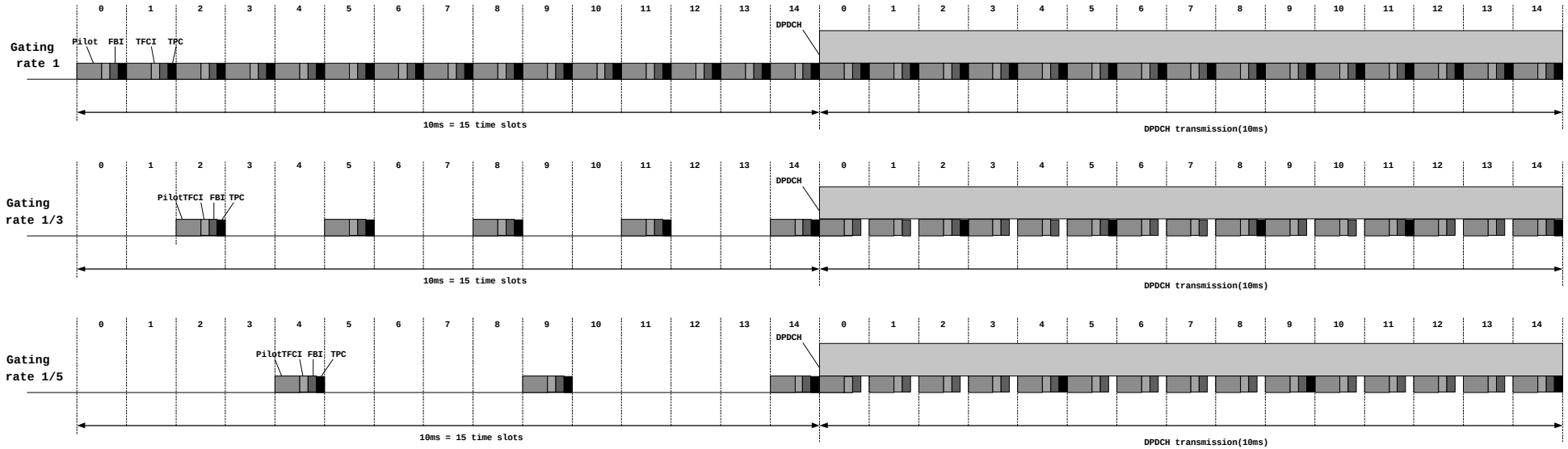


Figure 5 : Uplink DPCCH gating with regular gating pattern during signalling message transmission