3GPP TSG RAN WG1 *TSGR1#9(99)i17*
November 30 –December 3, 1999, Dresden, Germany

Agenda item: **Ad hoc 14**

Source: **Philips**

Title: **Text Proposal for Timing for Initialisation Procedures**

Document for: **Decision**

Introduction

The aim of this text proposal is to clarify the timing requirements for initialisation of DCHs and DSCHs.

The relative timing between the frame boundaries on the different channels is defined already in section 7 of TS25.211. However, this does not specify the absolute timing of the commencement of channels, which it is necessary to specify in WG1 in order to avoid blind detection in the receivers.

It has been proposed that the information in section 7 of TS25.214 ("Procedures in Packet Data Transfer"), which currently describes a procedure for initialisation of DCHs and DSCHs, should be cleaned up by deleting unnecessary information. The remainder of the information (notably the text on power control, as contained in the text proposal in R1-99h04 which was agreed in the adhoc 14 meeting in New York, and which is available for WG1#9 as R1-99i12) is proposed to be moved to more appropriate parts of the Specification in a separate Change Request, CR25214-015 in R1-99i13. The text proposal in this document is designed to supersede and clarify the timing information given in section 7 of TS25.214.

The key feature of this text proposal is that it is necessary to specify the amount of time which will be available to the UE to decode the FACH before commencement of the related channels. This time is referred to as $T_{1\text{-min}}$. We suggest that $T_{1\text{-min}}$ should be set to 15 slots, being the maximum length of time which could be required by a low-rate terminal. This is consistent with the current assumptions about the time taken to decode TPC bits.

The exact frame boundary at which the related channels will commence can then be determined in terms of T_n and T_k (which define the relative frame timings in section 7 of TS25.211) and $T_{1\text{-min}}$. Depending on the values of T_n and T_k it is necessary to add a number of frames offset, N_{offset}, before the channels can commence.

The time between the end of the relevant FACH frame and the start of the DL DPCCH is shown in figures 3 – 5 as T_1. We aim to find the earliest possible starting time for the DL DPCCH consistent with the specified value of $T_{1\text{-min}}$ and the prevailing values of T_n and T_k.

T_1 can be written as:

$T_1 = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset} \times 38400$ chips , where N_{pcp} is a higher layer parameter and represents the length of the power control preamble in slots. (N_{pcp} is defined to be able to take values of 0 or 8 in CR25214-015 in R1-99i13.) N_{pcp} x 2560 is therefore equal to the number of chips in the power control preamble. T_n and T_k are defined in TS25.211 as having units of $^1/_{10}$ slot, and can take integer values in the range 0 … 149.

The value of N_{offset} depends on whether the prevailing values of T_n and T_k result in a value of T_1 which is greater than or less than $T_{1\text{-min}}$:

$$N_{offset} = \begin{cases} 1 \text{ when } (T_n - T_k) \times 256 - N_{pcp} \times 2560 + 38400 \geq T_{1-\min} \\ 2 \text{ when } (T_n - T_k) \times 256 - N_{pcp} \times 2560 + 38400 < T_{1-\min} \\ \qquad \text{and } (T_n - T_k) \times 256 - N_{pcp} \times 2560 + 2 \times 38400 \geq T_{1-\min} \end{cases}$$

3 when $(T_n - T_k) \times 256 - N_{pcp} \times 2560 + 2 \times 38400 < T_{1-\min}$

These equations can be rearranged (as in the following text proposal) to indicate more clearly the ranges of values of T_n which result in particular delays in initiating the DCH or DSCH.

Figures 3 – 5 show the FACH frame which contains information pertinent to the setting up of the DCH or DSCH. The timing reference is given by the P-CCPCH, from which the FACH frames are offset by T_k x 256 chips. The power control preamble on the DL DPCCH commences at the time T_1 after the end of the FACH frame, such that the frame boundary after N_{pcp} slots is offset by T_n x 256 chips from the P-CCPCH frame boundaries. T_1 must be greater than $T_{1\text{-min}}$. The UL DPCCH starts at a time T_0 after the start of the DL DPCCH, where T_0 is defined to be 1024 chips in section 7.6.3 of TS25.211.

The PDSCH frame boundaries, as shown in figure 3, are aligned to the P-CCPCH frame boundaries. The first frame on the PDSCH commences as close as possible to the first frame boundary on the DL DPCCH, subject to the stipulation (in section 7.5 of TS25.211) that it must commence between 1 slot before the DL DPCCH frame boundary and 14 slots after the the DL DPCCH frame boundary.

In figure 4, the DL DPDCH starts at the first frame boundary on the DL DPCCH, i.e. at the end of the power control preamble on the DL DPCCH.

In figure 5, the UL DPDCH starts at the first frame boundary on the UL DPCCH, i.e. at the end of the power control preamble on the UL DPCCH, or T_0 after the first frame boundary on the DL DPCCH.

3GPP TSG RAN WG1 Meeting #9
Dresden, Germany, 30 Nov – 3 Dec 1999

Document R1-99i17
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

3G25.214	CR	018	Current Version:	3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to:	TSG RAN #6	for approval	X	strategic		(for SMG use only)
list expected approval meeting # here ↑		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: (U)SIM [ ] ME [X] UTRAN / Radio [X] Core Network [ ]
(at least one should be marked with an X)

Source: Philips **Date:** 1999-11-11

Subject: Timing for intialisation procedures

Work item:

Category: *(only one category shall be marked with an X)*

F	Correction	
A	Corresponds to a correction in an earlier release	
B	Addition of feature	
C	Functional modification of feature	X
D	Editorial modification	

Release:

Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	X
Release 00	

Reason for change: Current timing relationships for initialisation of dedicated channels are unclear, and the time available to the UE for decoding the FACH is not specified.

Clauses affected: 7 Procedures in Packet Data Transfer

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

help.doc

<--------- double-click here for help and instructions on how to create a CR.

7 Procedures in Packet Data Transfer

7.1 Rapid Initialization of DCH for Packet Data Transfer

A rapid initialization procedure for establishing a DCH is defined to support bursting packet data transfer. The rapid initialization may be invoked for downlink packet data transfer on the DSCH or uplink packet data transfer on the DCH. The procedure may also be invoked to resume a recently discontinued DCH connection.

7.1.1 Rapid Initialization of DCH for Packet Data Transfer using DSCH

The synchronization of the DSCH/DCH pair may be expedited so that data transmission using DSCH can commence in slightly over 10 ms following the FACH burst assigning the TFCI using DCH. Figure 3shows the timing diagram of RACH/FACH to DCH/DCH+DSCH state transition. The parameter T_A specifies the RACH/FACH response time. The parameters T_B, T_C and T_D are referenced relative to the FACH frame. T_B specifies the time period when the downlink DPCCH is started. The parameter T_C specifies the period at which the UE will start the uplink DPCCH. Finally, T_D specifies the period that the DCH will be stable and the first frame of data may arrive. The parameters T_B, T_C, and T_D have the following relationship:

$$T_B < T_C << T_D$$

$$T_D = T_B + N_{slots}*0.666$$

where N_{slots} is a positive integer.

In order to initialise fast uplink link power control loop, searcher and channel estimator at the Node B, the UE will adhere to the following:

- The transmission of uplink link DPCCH will start at N_{slots} slots (1 to 15 slots) prior to the scheduled downlink packet data transmission using DSCH.
- The DPCCH will be transmitted with an additional negative power offset P_{offset} from the computed open loop estimate.
- The initial power control step size for transmitting the DPCCH will be set at P_{step} (typically: 2dB).
- The UE will revert back to the normal power control (PC) step size upon the receipt of the first down power control command during the uplink DPCCH transmission phase,
- The step size always goes back to its nominal setting in the beginning of DSCH transmission

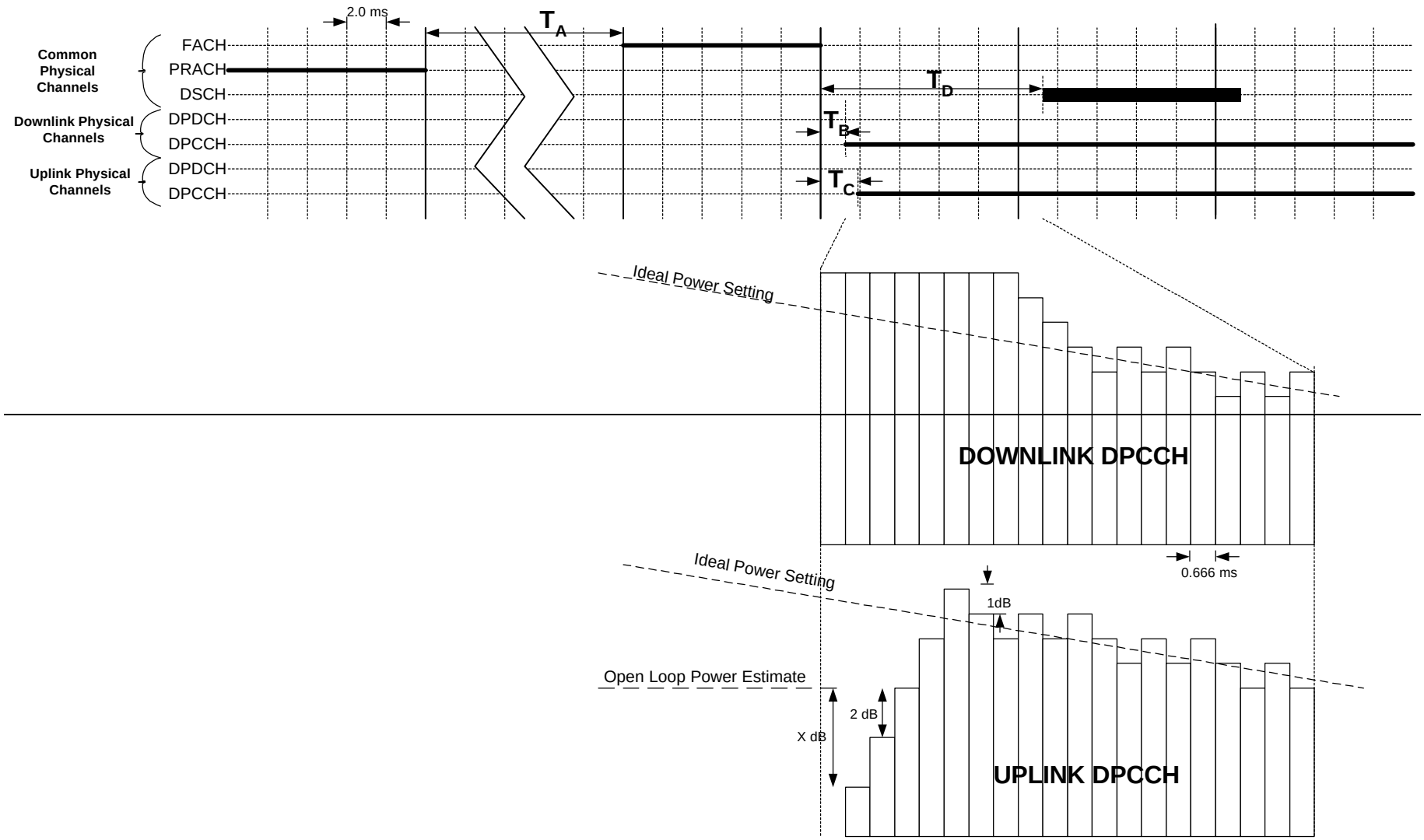
The parameters T_B, T_C, T_D, N_{slots}, P_{offset} and P_{step} may be negotiated with each individual UE or broadcast by the system so that the transition from RACH/FACH to DCH/DCH+DSCH sub-state is optimised.

7.1.2 Rapid Initialization of DCH for Uplink Packet Data Transfer

The synchronization of the DCH may also be expedited for the transfer of uplink packet data.. Figure 4 shows the same parameters T_B, T_C, and T_D applied to an uplink packet data transfer. The UE, upon detecting data in its queue, transmits a RACH with measurement report. After the UTRAN assigns the DCH via the FACH message, the downlink DPCCH is started after a time period T_B. The UE then begins transmission of the uplink DPCCH for reasons as outlined in section 7.3.4 at time period T_C. T_C is measured relative to the FACH transmit timing. Finally, the UE begins transmitting the data on the DPDCH after the period. The procedure for starting the uplink DPCCH transmission will be similar to Section 7.3.4.1

7.1.3 Resumption of DCH for Downlink or Uplink Packet Data Transfer

The synchronization of the DCH technique may be used to resume a DCH/DCH+DSCH connection that has been dropped for a short period.. This is applicable for packet data transfer using DSCH or uplink DPDCH or bi-directional data transfer using DSCH/Uplink DPDCH. Figure 5 shows the case where the DCH has been discontinued based on an inactivity timer T_E. The UTRAN, upon detecting data in the queue, may resume the DCH operation provided the period T_E has not elapsed. Typically T_E is set to 1000msec.



~~Figure 3: Rapid Initialization of DCH for packet data transfer over the DSCH~~

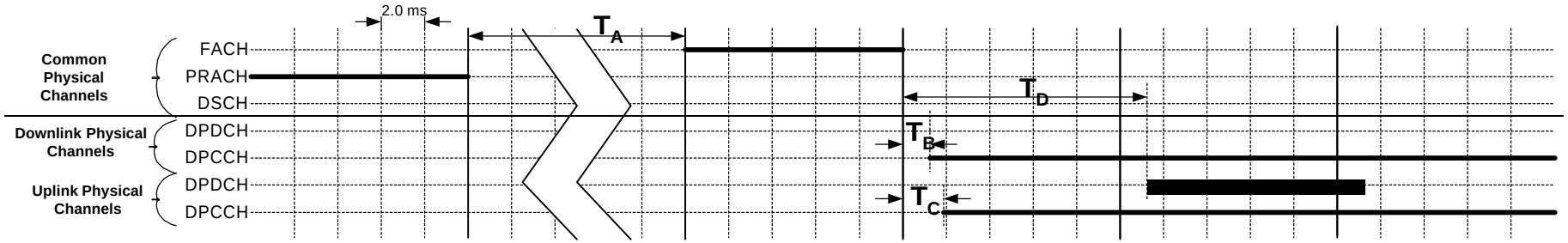


Figure 4: Rapid initialization of the DCH for transfer of uplink packet data

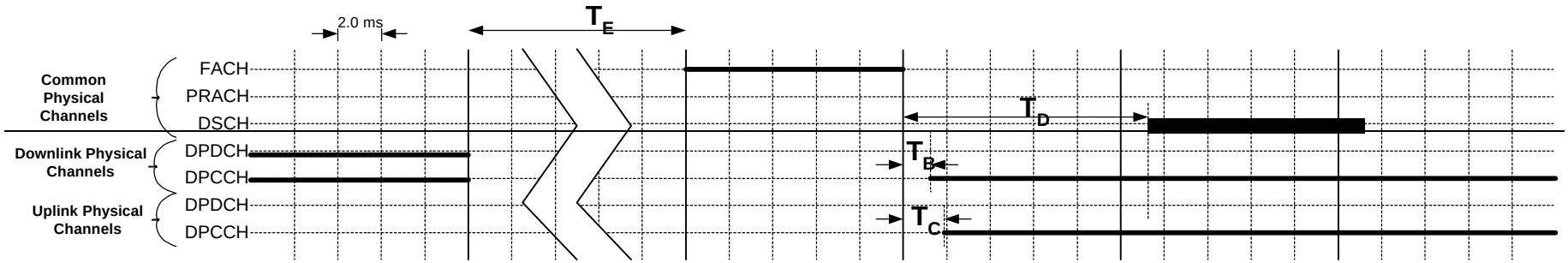


Figure 5: Resumption of the DCH for transmission of downlink packet data

7 Timing relations for initialisation of channels

7.1 Initialisation of DSCH

Figure 3 shows the timing relationships between the physical channels involved in the initialisation of a DSCH. The downlink DPCCH shall commence at a time T_1 after the end of the relevant FACH frame, where

$T_1 = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset} \times 38400$ chips , where:

N_{pcp} is a higher layer parameter set by the network, and represents the length of the power control preamble in slots;

$$N_{offset} = \begin{cases} 1 \text{ when } T_n - T_k \geq \frac{T_{1-\min}}{256} + 10N_{pcp} - 150 \\ 2 \text{ when } \frac{T_{1-\min}}{256} + 10N_{pcp} - 300 \leq T_n - T_k < \frac{T_{1-\min}}{256} + 10N_{pcp} - 150 \\ 3 \text{ when } T_n - T_k < \frac{T_{1-\min}}{256} + 10N_{pcp} - 300 \end{cases}$$

$T_{1\text{-min}}$ = 38400 chips (i.e.15 slots), and is the maximum time permitted for the UE to decode the FACH frame before the first frame of the DPCCH is received;

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see section 7.1 of TS25.211). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T_0 (see section 7.6.3 of TS25.211) after the start of the downlink DPCCH.

The PDSCH shall commence at the nearest P-CCPCH frame boundary to the end of the DL DPCCH power control preamble, subject to the restrictions in section 7.5 of TS25.211.

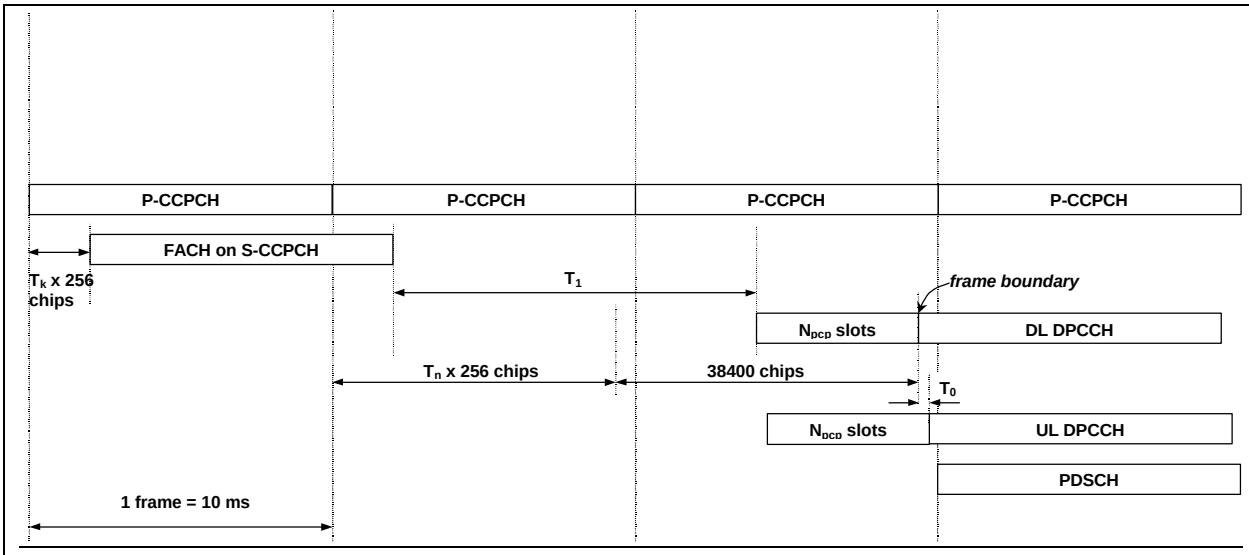


Figure 3: Timing of initialisation of DSCH

7.2 Initialisation of downlink DCH

Figure 4 shows the timing relationships between the physical channels involved in the initialisation of a downlink DCH. The definitions of T_1, N_{pcp}, N_{offset}, $T_{1\text{-}min}$, T_n, T_k and T_0 are as in section 7.1.

The downlink DPDCH shall commence at a time T_2 after the end of the relevant FACH frame, where

$T_2 = T_1 + N_{pcp}$ x 2560 chips.

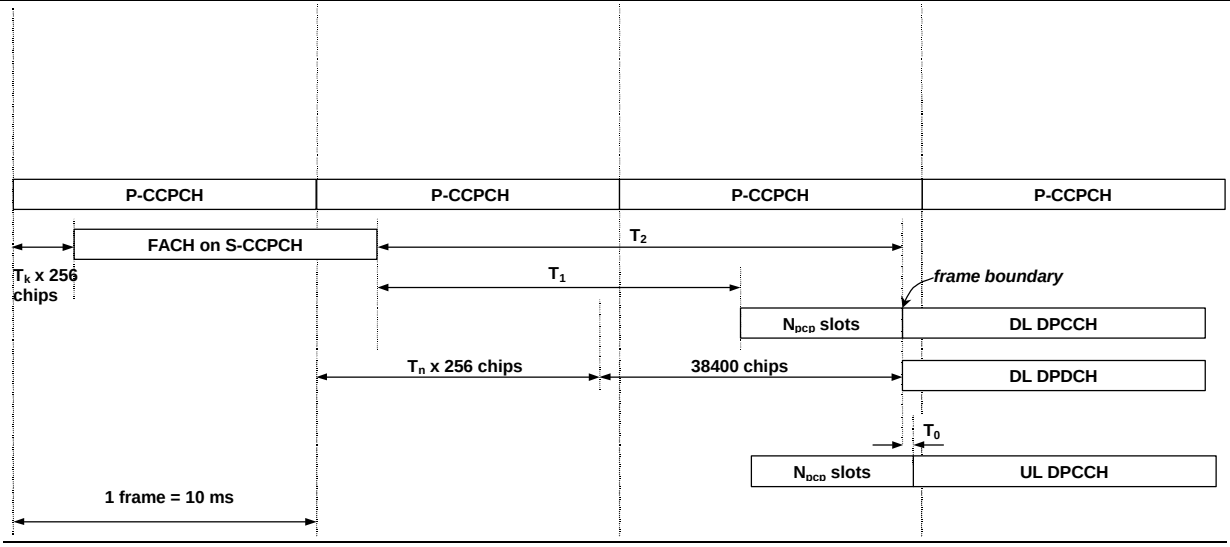


Figure 4: Timing of initialisation of DL DCH

7.3 Initialisation of uplink DCH

Figure 5 shows the timing relationships between the physical channels involved in the initialisation of an uplink DCH. The definitions of T_1, N_{pcp}, N_{offset}, $T_{1\text{-}min}$, T_n, T_k and T_0 are as in section 7.1.

The uplink DPDCH shall commence at a time T_3 after the end of the relevant FACH frame, where

$T_3 = T_1 + T_0 + N_{pcp}$ x 2560 chips.

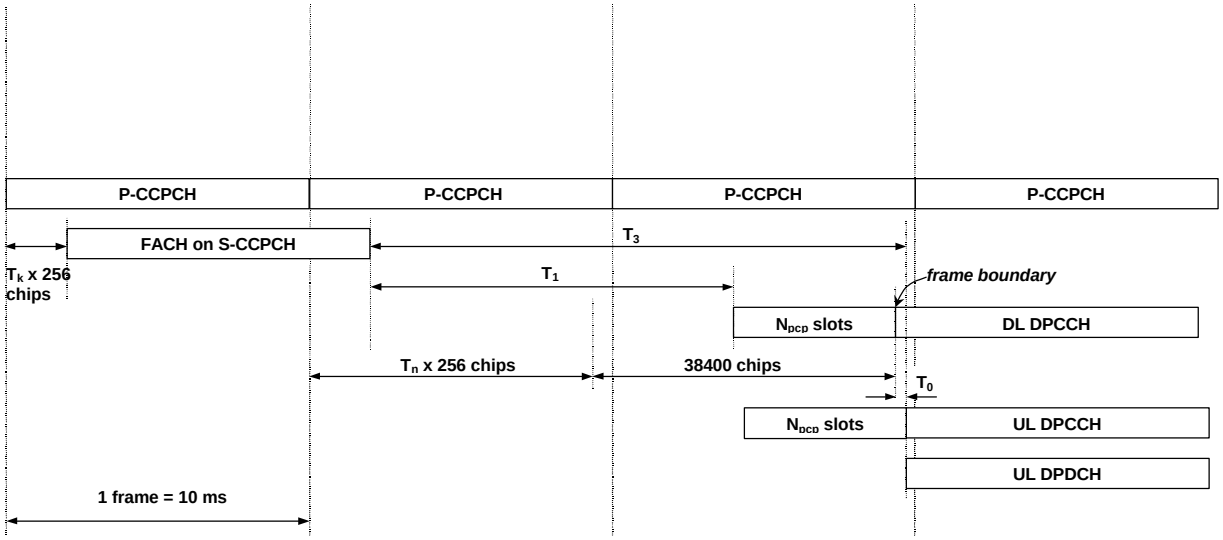


Figure 5: Timing of initialisation of UL DCH