



Smarter Micro
Link Smart

Support lower power class for NR (RWS-210135)

RAN Rel-18 Workshop (June 28 – July 2, 2021)

RFFE PA design requirements for lower power class (PC5)

- To support lower power class of UE, e.g., PC5(20dBm), the PA design requirements will be different with PC3(23dBm) or PC2(26dBm)
- As the Figure 1/2 shows, the PC5 PA design specification will be:
 - Output power: 20dBm(PC5) + 5dB(post-PA loss) = 25dBm
 - SOI CMOS will be candidate process for PA design, while the most PC2/3 PAs were developed by GaAs HBT process
 - Gain: 25dBm(PA output power) – 5dBm(transceiver max. output power) = 20dB
 - 2-stage PA design will be enough instead of 3-stage PA design using in PC2/3

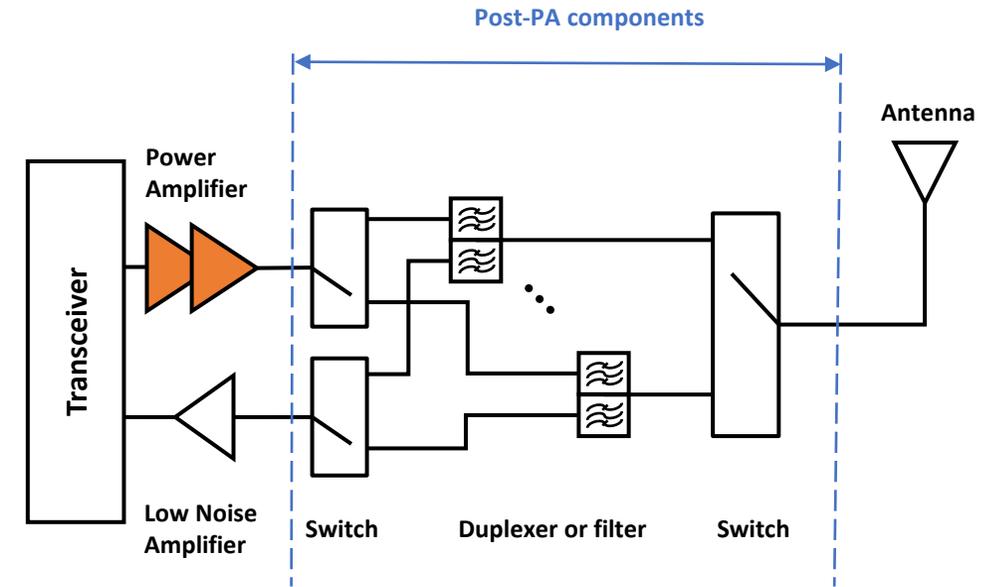


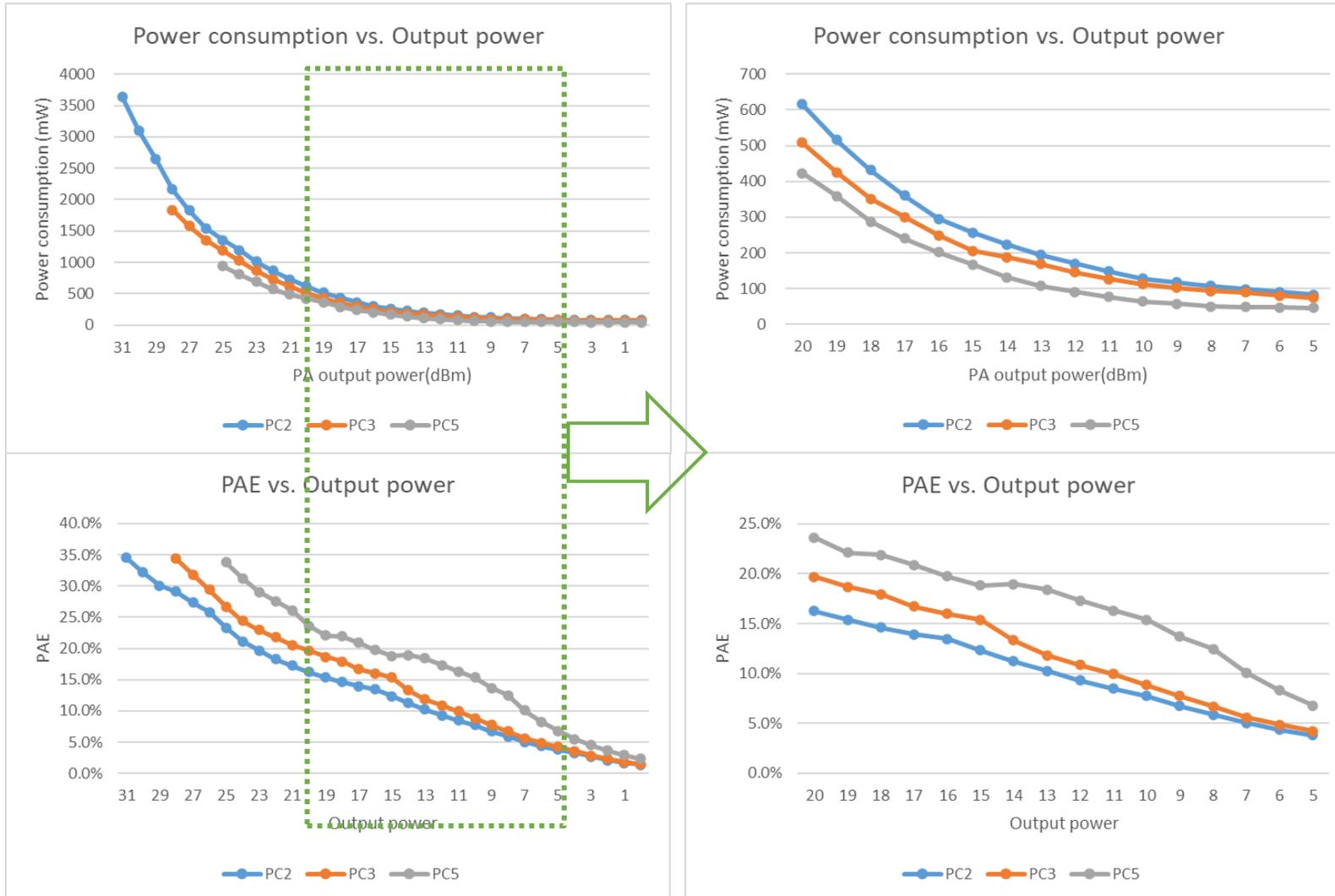
Figure 1. RFFE block diagram for NR UE

	ISSCC2020[1]	ISSCC2019[2]	ISSCC2019[3]
Transceiver output power	>6dBm	>5dBm(n77)	6dBm(n41)

Figure 2. The output power of transceiver

[1] A 12nm CMOS RF Transceiver Supporting 4G/5G UL MIMO, ISSCC 2020
 [2] Sub-6GHz 5G New Radio RF Transceiver Supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL in 14nm FinFET CMOS, ISSCC 2019
 [3] An LTE-A Multimode Multiband RF Transceiver with 4RX/2TX Inter-Band Carrier Aggregation, 2-Carrier 4x4 MIMO with 256QAM and HPUE Capability in 28nm CMOS, ISSCC 2019

Power consumption of PA at lower power class (PC5)



- The PC5 PA (max. power=25dBm) power consumption is much lower than PC2 and PC3
- The PC2/3 PA is over designed for higher output power, hence the PAE get worse at backoff power stage:
 - At 25dBm, PC5 PA saves 100~200mW than PC2/3 PA
- The PC5 PA is 2-stage topology, while the PC2/3 PA is 3-stage topology, hence the PC5 PA has higher PAE at lower power stage(0~10dBm)
 - At 5dBm, PC5 PA saves about 40mW than PC2/3 PA

Figure3. power consumption vs output power

Data measured with APT optimization.

Cost optimized for PC5 PA

- RF SOI is a very popular technology at RF components, including RF switches, antenna tuners and RF amplifiers
- Typically, the power amplifier is based on GaAs technology, which is good performance at higher output power handling than SOI

- We compared the cost both GaAs PA and SOI PA, as Figure4 shows:
 - The GaAs PA size: $0.6 \times 0.7 = 0.42 \text{mm}^2$
 - The SOI PA size: $0.5 \times 1.0 = 0.5 \text{mm}^2$
 - The unit size cost of SOI is about $1/3 \sim 1/2$ of GaAs, hence **the cost of SOI PA is 40~60% of GaAs PA with the same design**



Figure4. Die size comparison of PA using SOI and GaAs

Summary

- Lower power class (PC5) will lead to lower consumption
- SOI technology is suitable for PC5 PA design, and lower cost
- We support 20dBm UE power class (power class 5) for NR Uu and sidelink