3GPP TSG RAN Meeting #27 **RP-050039**
Tokyo, Japan, 9 - 11 March 2005

Title **CRs (Rel-5 &Rel-6 CatA) to 25.101 on corrections to the HS-DPCCH time mask requirements**
Source **3GPP TSG RAN WG4 (Radio)**
Agenda Item **8.5.5**

WG Tdoc	Spec	CR	R	Cat	Rel	Curr Ver	Title	Work Item
R4-050279	25.101	403	2	F	Rel-5	5.13.0	HS-DPCCH time mask requirements	HSDPA-RF
R4-050280	25.101	404	2	A	Rel-6	6.6.0	HS-DPCCH time mask requirements	HSDPA-RF

3GPP TSG RAN WG4 (Radio) Meeting #34 **R4-050279**

Scottsdale, US 14 - 18 February 2005

CR-Form-v7.1

CHANGE REQUEST

⌘ **25.101** **CR** **403** ⌘ **rev** **2** ⌘ Current version: **5.13.0** ⌘

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.*

Proposed change affects: UICC apps⌘ ☐ ME ☒ Radio Access Network ☐ Core Network ☐

Title:	⌘	HS-DPCCH time mask requirements
Source:	⌘	3GPP TSG RAN WG4 (Radio)
Work item code:	⌘	HSDPA-RF
Date:	⌘	28/02/2005
Category:	⌘	**F**
Release:	⌘	Rel-5

Use one of the following categories:
F *(correction)*
A *(corresponds to a correction in an earlier release)*
B *(addition of feature),*
C *(functional modification of feature)*
D *(editorial modification)*
Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use one of the following releases:

Ph2	*(GSM Phase 2)*
R96	*(Release 1996)*
R97	*(Release 1997)*
R98	*(Release 1998)*
R99	*(Release 1999)*
Rel-4	*(Release 4)*
Rel-5	*(Release 5)*
Rel-6	*(Release 6)*
Rel-7	*(Release 7)*

Reason for change:	⌘	The current requirement defines the period for evaluating the power step due to HS-DPCCH transmission as being between the reference timeslot and the target timeslot. This definition is only explicit for the case where the HS-DPCCH timeslot structure is aligned with the DPCCH. Since the HS-DPCCH can be offset from the DPCCH in increments of 0.1 slots (256 chips) it is not meaningful to define the power step relative to periods of one timeslot duration. The reason is that this evaluation period will in itself contain a power step since both the HS-DPCCH and the DPCCH/DPDCH can change power at their respective slot boundaries. Such a definition implies averaging the power across a power step in order to calculate another power step which does not make sense.
Summary of change:	⌘	The power evaluation period is defined as being bounded by adjacent DPCCH and HS-DPCCH slot boundaries. The sum of any two adjacent power evaluation periods will equal 2560 chips.
Consequences if not approved:	⌘	UE behaviour in caculating the correct power when the HS-DPCCH is not aligned with the DPCCH will be ambiguous with different possible interpretations as to how the power step should be calculated.

Clauses affected:	⌘	6.1.1				
Other specs affected:	⌘	**Y**	**N**		⌘	34.121
			X	Other core specifications		
		X		Test specifications		
			X	O&M Specifications		

Other comments:	⌘	Equivalent CRs in other Releases: CR404r2 cat. A to 25.101 Rel-6

How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at http://www.3gpp.org/specs/CR.htm. Below is a brief summary:

1) Fill out the above form. The symbols above marked ⌘ contain pop-up help information about the field that they are closest to.
2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be downloaded from the 3GPP server under ftp://ftp.3gpp.org/specs/ For the latest version, look for the directory name with the latest date e.g. 2001-03 contains the specifications resulting from the March 2001 TSG meetings.
3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

6.5.5 HS-DPCCH

The transmission of Ack/Nack or CQI over the HS-DPCCH may cause~~s~~ the transmission power in the uplink to vary. The ratio of the amplitude between the DPCCH and the Ack/Nack and CQI respectively is signalled by higher layers.

6.5.5.1 Minimum requirement

~~A change of output power is required when Ack/Nack or CQI is transmitted. The ratio of the amplitude between the DPCCH and the Ack/Nack and CQI respectively is signalled by the higher layers.~~ The sum power on DPCCH+DPDCH ~~shall not change by~~ is independent of the transmission of Ack/Nack and CQI unless the UE output power when Ack/Nack or CQI is transmitted would exceed the maximum value specified in Table 6.1~~a~~A or fall below the value specified in 6.4.3.1, whereupon the UE shall apply additional scaling to the total transmit power as defined in section 5.1.2.6 of TS.25.214 [8].

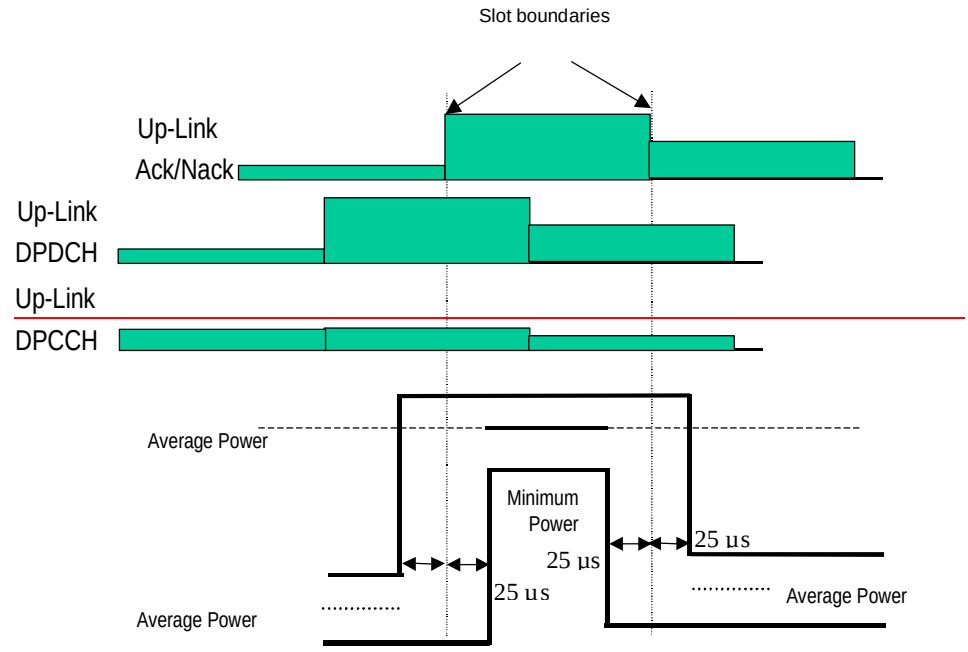
The ~~sum in total~~ composite transmitted power (DPCCH + DPDCH+HS-DPCCH) shall ~~then~~ be rounded to the closest integer dB value. When the HS-DPCCH slot timing is aligned with the DPCCH slot timing, the calculation of the power step and any subsequent change in transmitted power occurs once per DPCCH slot at the DPCCH slot boundaries. When the HS-DPCCH slot timing is not aligned with the DPCCH slot timing, this same process occurs twice per DPCCH slot, once at the DPCCH boundary and once at the HS-DPCCH boundary. A power step exactly half~~-~~way between two integer values shall be rounded to the closest integer of greater magnitude. The accuracy of the power step, given the step size, is specified in Table 6.9A.

The nominal power ~~change~~ step due to transmission of Ack/Nack or CQI is defined as the ~~relative power~~ difference between the nominal mean power of ~~during the~~ any two adjacent power evaluation periods. In the simple case where the HS-DPCCH slots are aligned with the DPCCH slots, each power evaluation period shall be one DPCCH timeslot in length. In the case where the HS-DPCCH timeslots are not aligned with the DPCCH timeslots, the power evaluation periods are shorter and start with a DPCCH slot boundary ending ~~in~~ with the next HS-DPCCH slot boundary or start with an HS-DPCCH slot boundary and end with the next DPCCH slot boundary. In this non-aligned case, the length of any two adjacent power evaluation periods equals 2560 chips. In all cases the evaluation of mean power shall exclude a 25µs period before and after any DPCCH or HS-DPCCH slot boundary. ~~original (reference) timeslot and the mean power of the target timeslot, not including the transient duration. The transient duration is from 25µs before the HS-DPCCH slot boundary to 25µs after the HS-DPCCH slot boundary.~~

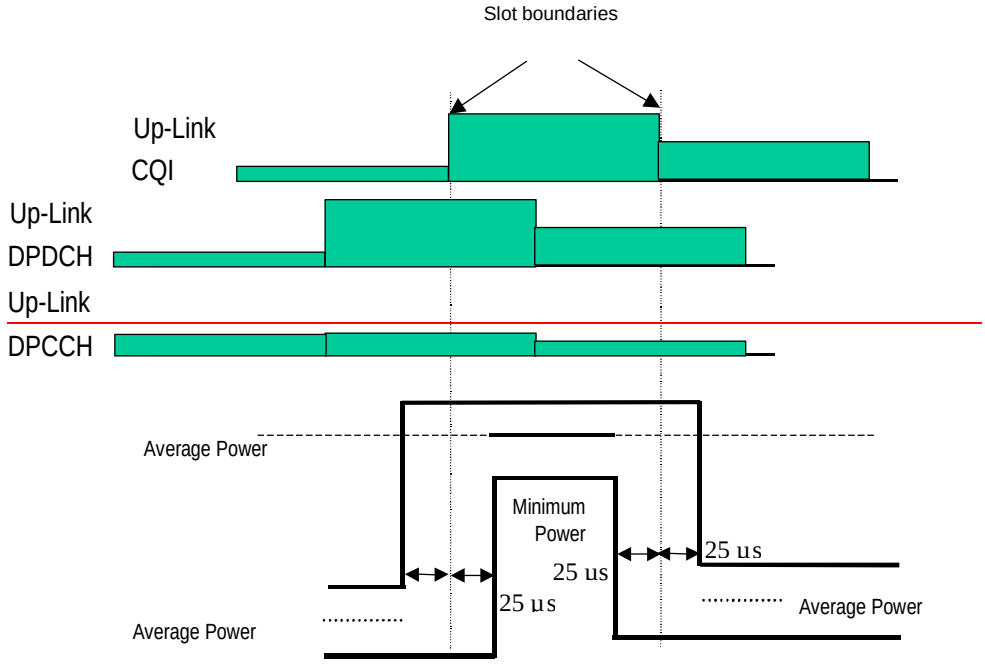
Table 6.9A: Transmitter power step tolerance

Nominal ~~P~~power step size (Up or down) ΔP [dB]	Transmitter power step tolerance [dB]
0	+/- 0.5
1	+/- 0.5
2	+/- 1.0
3	+/- 1.5
$4 \leq \Delta P \leq 7$	+/- 2.0

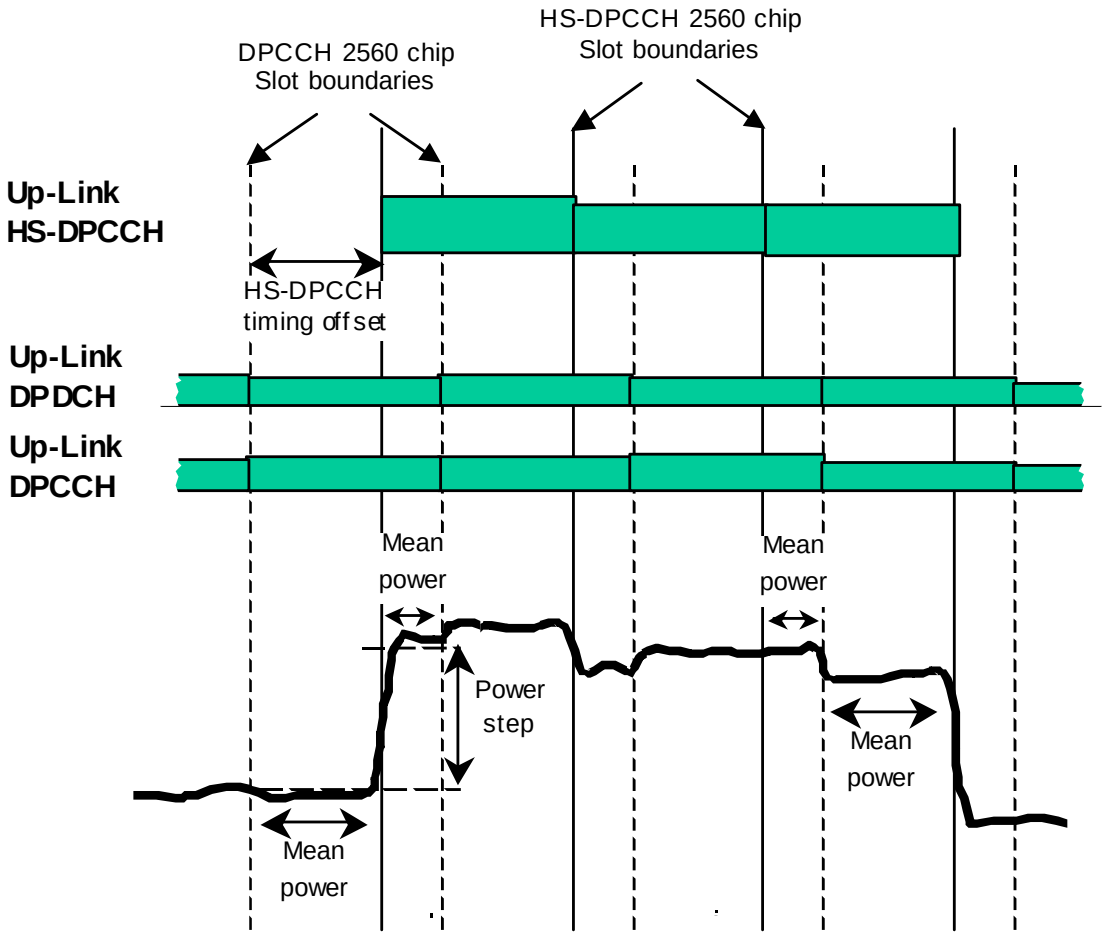
The transmit power levels versus time shall meet the mask specified in Figure 6.6~~x~~.



~~Figure 6.5A: Transmit template during Ack/Nack transmission~~



~~Figure 6.5B: Transmit template during CQI transmission~~



The mean power is evaluated excluding a 25µs transient period either side of any DPCCH or HS-DPCCH slot boundary

Figure 6.6: Transmit power template during HS-DPCCH transmission

3GPP TSG RAN WG4 (Radio) Meeting #34 **R4-050280**

Scottsdale, US 14 - 18 February 2005

CR-Form-v7.1

CHANGE REQUEST

⌘ **25.101** **CR** **404** ⌘ **rev** **2** ⌘ Current version: **6.6.0** ⌘

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ⌘ symbols.*

Proposed change affects: UICC apps⌘ ☐ ME ☒ Radio Access Network ☐ Core Network ☐

Title:	⌘	HS-DPCCH time mask requirements
Source:	⌘	3GPP TSG RAN WG4 (Radio)
Work item code:	⌘	HSDPA-RF
Date:	⌘	28/02/2005
Category:	⌘	**A**
Release:	⌘	Rel-6

Use one of the following categories:
F *(correction)*
A *(corresponds to a correction in an earlier release)*
B *(addition of feature),*
C *(functional modification of feature)*
D *(editorial modification)*
Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use one of the following releases:
Ph2 (GSM Phase 2)
R96 (Release 1996)
R97 (Release 1997)
R98 (Release 1998)
R99 (Release 1999)
Rel-4 (Release 4)
Rel-5 (Release 5)
Rel-6 (Release 6)
Rel-7 (Release 7)

Reason for change:	⌘	The current requirement defines the period for evaluating the power step due to HS-DPCCH transmission as being between the reference timeslot and the target timeslot. This definition is only explicit for the case where the HS-DPCCH timeslot structure is aligned with the DPCCH. Since the HS-DPCCH can be offset from the DPCCH in increments of 0.1 slots (256 chips) it is not meaningful to define the power step relative to periods of one timeslot duration. The reason is that this evaluation period will in itself contain a power step since both the HS-DPCCH and the DPCCH/DPDCH can change power at their respective slot boundaries. Such a definition implies averaging the power across a power step in order to calculate another power step which does not make sense.
Summary of change:	⌘	The power evaluation period is defined as being bounded by adjacent DPCCH and HS-DPCCH slot boundaries. The sum of any two adjacent power evaluation periods will equal 2560 chips.
Consequences if not approved:	⌘	UE behaviour in caculating the correct power when the HS-DPCCH is not aligned with the DPCCH will be ambiguous with different possible interpretations as to how the power step should be calculated.

Clauses affected:	⌘	6.1.1				
Other specs affected:	⌘	**Y**	**N**		⌘	
			X	Other core specifications		34.121
		X		Test specifications		
			X	O&M Specifications		

Other comments:	⌘	Equivalent CRs in other Releases: CR403r2 cat. F to 25.101 Rel-5

How to create CRs using this form:

Comprehensive information and tips about how to create CRs can be found at http://www.3gpp.org/specs/CR.htm. Below is a brief summary:

1) Fill out the above form. The symbols above marked ⌘ contain pop-up help information about the field that they are closest to.
2) Obtain the latest version for the release of the specification to which the change is proposed. Use the MS Word "revision marks" feature (also known as "track changes") when making the changes. All 3GPP specifications can be downloaded from the 3GPP server under ftp://ftp.3gpp.org/specs/ For the latest version, look for the directory name with the latest date e.g. 2001-03 contains the specifications resulting from the March 2001 TSG meetings.
3) With "track changes" disabled, paste the entire CR form (use CTRL-A to select it) into the specification just in front of the clause containing the first piece of changed text. Delete those parts of the specification which are not relevant to the change request.

6.5.5 HS-DPCCH

The transmission of Ack/Nack or CQI over the HS-DPCCH may cause~~s~~ the transmission power in the uplink to vary. The ratio of the amplitude between the DPCCH and the Ack/Nack and CQI respectively is signalled by higher layers.

6.5.5.1 Minimum requirement

~~A change of output power is required when Ack/Nack or CQI is transmitted. The ratio of the amplitude between the DPCCH and the Ack/Nack and CQI respectively is signalled by the higher layers.~~ The sum power on DPCCH+DPDCH ~~shall not change by~~ is independent of the transmission of Ack/Nack and CQI unless the UE output power when Ack/Nack or CQI is transmitted would exceed the maximum value specified in Table 6.1~~a~~A or fall below the value specified in 6.4.3.1, whereupon the UE shall apply additional scaling to the total transmit power as defined in section 5.1.2.6 of TS.25.214 [8].

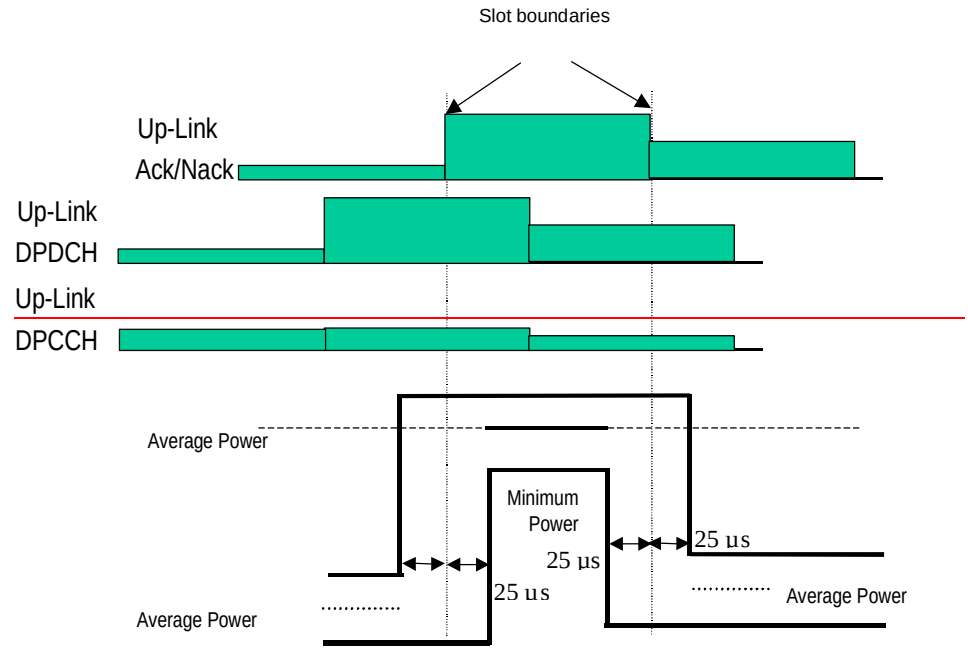
The ~~sum in total~~ composite transmitted power (DPCCH + DPDCH+HS-DPCCH) shall ~~then~~ be rounded to the closest integer dB value. When the HS-DPCCH slot timing is aligned with the DPCCH slot timing, the calculation of the power step and any subsequent change in transmitted power occurs once per DPCCH slot at the DPCCH slot boundaries. When the HS-DPCCH slot timing is not aligned with the DPCCH slot timing, this same process occurs twice per DPCCH slot, once at the DPCCH boundary and once at the HS-DPCCH boundary. A power step exactly half~~-~~way between two integer values shall be rounded to the closest integer of greater magnitude. The accuracy of the power step, given the step size, is specified in Table 6.9A.

The nominal power ~~change~~ step due to transmission of Ack/Nack or CQI is defined as the ~~relative power~~ difference between the nominal mean power of ~~during the~~ any two adjacent power evaluation periods. In the simple case where the HS-DPCCH slots are aligned with the DPCCH slots, each power evaluation period shall be one DPCCH timeslot in length. In the case where the HS-DPCCH timeslots are not aligned with the DPCCH timeslots, the power evaluation periods are shorter and start with a DPCCH slot boundary ending ~~in~~ with the next HS-DPCCH slot boundary or start with an HS-DPCCH slot boundary and end with the next DPCCH slot boundary. In this non-aligned case, the length of any two adjacent power evaluation periods equals 2560 chips. In all cases the evaluation of mean power shall exclude a 25µs period before and after any DPCCH or HS-DPCCH slot boundary. ~~original (reference) timeslot and the mean power of the target timeslot, not including the transient duration. The transient duration is from 25µs before the HS-DPCCH slot boundary to 25µs after the HS-DPCCH slot boundary.~~

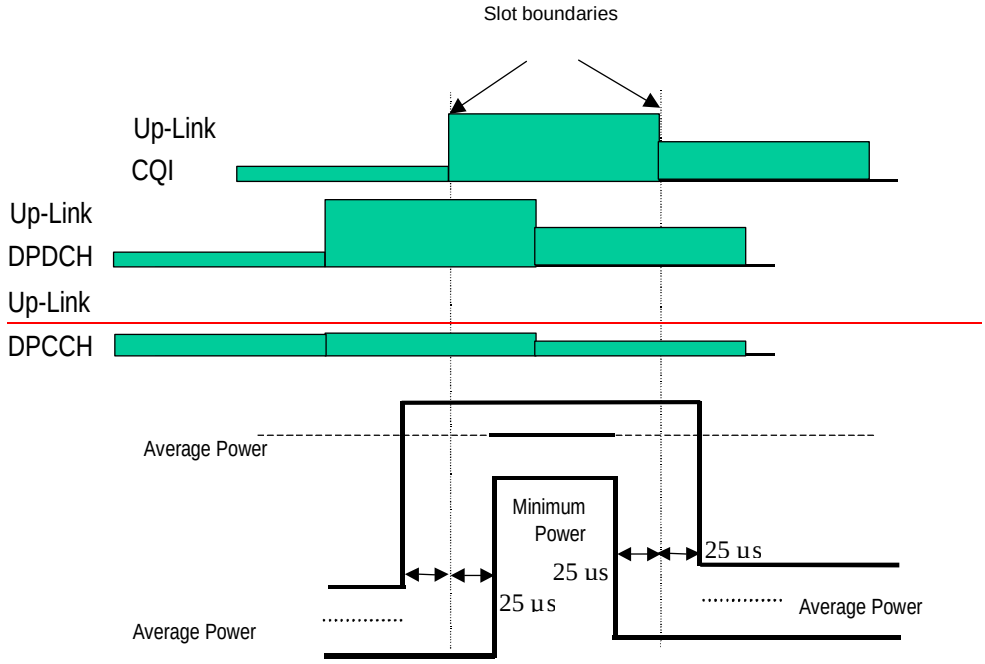
Table 6.9A: Transmitter power step tolerance

Nominal ~~P~~power step size (Up or down) ΔP [dB]	Transmitter power step tolerance [dB]
0	+/- 0.5
1	+/- 0.5
2	+/- 1.0
3	+/- 1.5
$4 \leq \Delta P \leq 7$	+/- 2.0

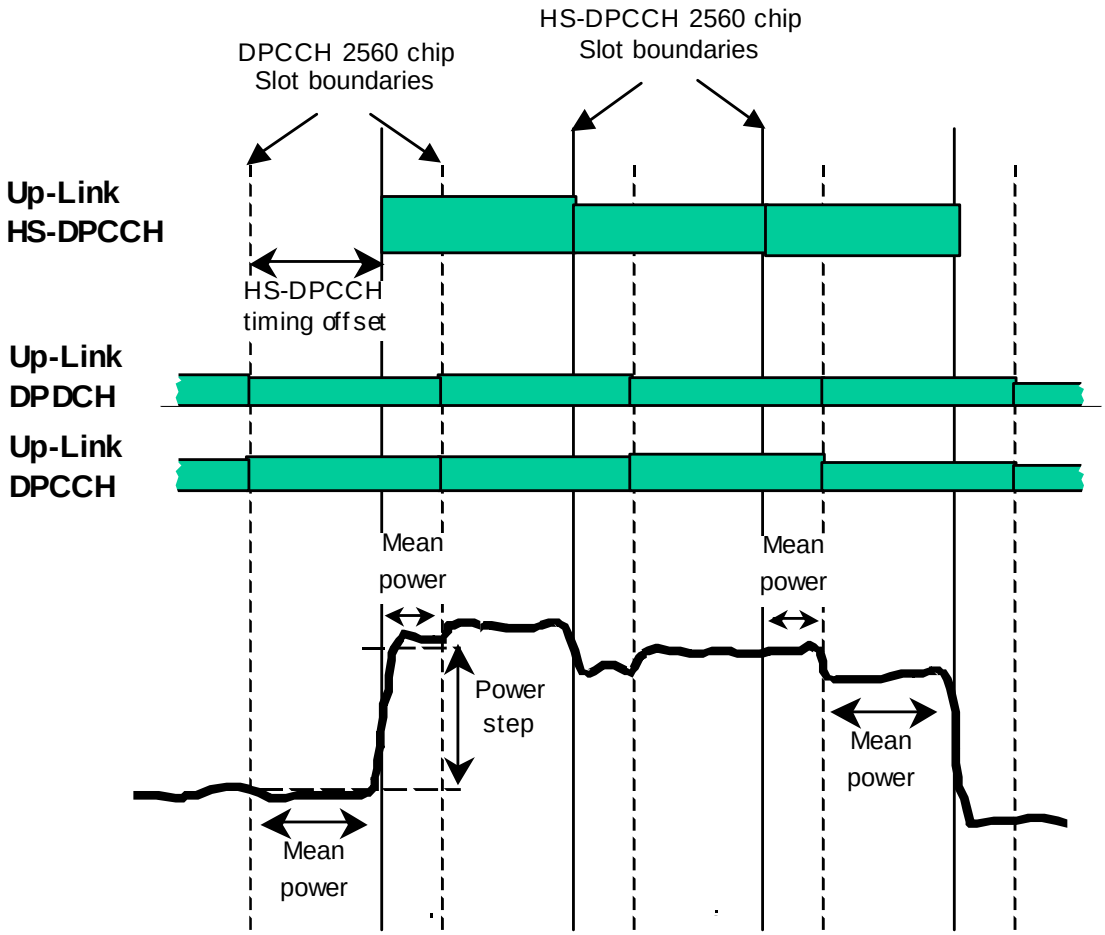
The transmit power levels versus time shall meet the mask specified in Figure 6.6~~x~~.



~~Figure 6.5A: Transmit template during Ack/Nack transmission~~



~~Figure 6.5B: Transmit template during CQI transmission~~



The mean power is evaluated excluding a 25µs transient period either side of any DPCCH or HS-DPCCH slot boundary

Figure 6.6: Transmit power template during HS-DPCCH transmission