#### **RP-050037**

#### 3GPP TSG RAN Meeting #27 Tokyo, Japan, 9 - 11 March 2005

# TitleCRs (R99 & Rel-4/Rel-5/Rel-6 CatA) to 25.133 for the Correction of<br/>DPCH\_Ec/lor level in Annex 7Source3GPP TSG RAN WG4 (Radio)Agenda Item8.5.3

WG Tdoc	Spec	CR	R	Cat	Rel	Curr Ver	Title	Work Item
R4-050256	25.133	724	2	F	R99	3.19.0	Correction to DPCH_Ec/lor level in A.7.1 UE Transmit Timing	TEI
R4-050257	25.133	725	2	Α	Rel-4	4.13.0	Correction to DPCH_Ec/lor level in A.7.1 UE Transmit Timing	TEI
R4-050258	25.133	726	2	Α	Rel-5	5.13.0	Correction to DPCH_Ec/lor level in A.7.1 UE Transmit Timing	TEI
R4-050259	25.133	727	2	Α	Rel-6	6.8.0	Correction to DPCH_Ec/lor level in A.7.1 UE Transmit Timing	TEI

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	CHANGE REQUEST	CR-Form-v7
æ	25.133 CR 724 <b># rev</b> 2 <sup>#</sup>	Current version: <b>3.19.0</b> <sup>#</sup>
For <mark>HELP</mark> on u	sing this form, see bottom of this page or look at the	pop-up text over the X symbols.
Proposed change	<b>affects:</b> UICC apps <b>೫ ──</b> ME <mark>X</mark> Radio Ac	cess Network Core Network
Title: ೫	Correction to DPCH_Ec/lor level in A.7.1 UE Trans	mit Timing
Source: ж	3GPP TSG RAN WG4 (Radio)	
Work item code: ೫	TEI	<b>Date:</b>
Category: ⊮	<ul> <li>F</li> <li>Use <u>one</u> of the following categories:</li> <li>F (correction)</li> <li>A (corresponds to a correction in an earlier release,</li> <li>B (addition of feature),</li> <li>C (functional modification of feature)</li> <li>D (editorial modification)</li> <li>Detailed explanations of the above categories can be found in 3GPP <u>TR 21.900</u>.</li> </ul>	Release: %R99Use one of the following releases: 2(GSM Phase 2))R96(Release 1996)R97(Release 1997)R98(Release 1998)R99(Release 1999)Rel-4(Release 4)Rel-5(Release 5)Rel-6(Release 6)
	<ul> <li>In A.7.1.2 step I, UE is connected with Cell 2, a situation, the power of Cell 2(-99 dBm) is lowe and the UE perceives DPCH_Ec/Io = -23 dB o understand the SS on Cell 2 and may drop the necessary for the test purpose.</li> <li>In table A.7.1 DPCH_Ec/Ior increased 0.5 dB AWGN. OCNS_Ec/Ior adjusted.</li> </ul>	r than the power of Cell1(-96 dBm), n cell 2. The UE may not e link. A link to Cell 2, however, is
Consequences if not approved:	# The purpose of the test may not be completed	, and good UEs may fail the test
Clauses affected:	೫ <mark>A.7.1.1</mark>	
Other specs affected:	YN%XXOther core specificationsXTest specificationsXO&M Specifications	21

Other comments:# Isolated impact analysis: Will not change UE implementation.<br/>Equivalent CRs in other Releases: CR725r2 cat. A to 25.133 Rel-4, CR726r2 cat.<br/>A to 25.133 Rel-5, CR727r2 cat. A to 25.133 Rel-6

## A.7.1 UE Transmit Timing

#### A.7.1.1 Test Purpose and Environment

The purpose of this test is to verify that the UE initial transmit timing accuracy, maximum amount of timing change in one adjustment, minimum and maximum adjustment rate are within the specified limits. This test will verify the requirements in section 7.1.2.

For this test two cells on the same frequency are used. Table A.7.1 defines the transmitted signal strengths, the relative timing and the propagation condition used for the two cells.

Parameter	Unit	Level
DPCH_Ec/ lor, Cell 1 and Cell 2	dB	-1 <u>3.5</u> 7
CPICH_Ec/ lor, Cell 1 and Cell 2	dB	-10
PCCPH_Ec/ lor, Cell 1 and Cell 2	dB	-12
SCH_Ec/ lor, Cell 1 and Cell 2	dB	-12
PICH_Ec/ lor, Cell 1 and Cell 2	dB	-15
OCNS_Ec/ lor, Cell 1 and Cell 2	dB	-1. <u>2</u> 05
Î <sub>or,</sub> Cell 1	dBm/3.84 MHz	-96
Î <sub>or,</sub> Cell 2	dBm/3.84 MHz	-99
Information data rate	kbps	12.2
Relative delay of path received from cell 2 with respect to cell 1	μs	+/-2
Propagation condition	A	WGN

Table A.7.1: Test parameters for UE Transmit Timing requirement

#### A.7.1.2 Test Requirements

1

For parameters specified in Table A.7.1, the UE initial transmit timing accuracy, the maximum amount of timing change in one adjustment, the minimum and the maximum adjustment rate shall be within the limits defined in section 7.1.2.

- a) After a connection is set up with cell 1, the test system shall verify that the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.  $T_0$  is defined in TS 25.211[2].
- b) Test system introduces cell 2 into the test system at delay +2  $\mu$ s from cell 1.
- c) Test system verifies that cell 2 is added to the active set.
- d) Test system shall verify that the UE transmit timing offset is still within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- e) Test system switches Tx timing of cell 2 to a delay of  $-2 \,\mu s$  with respect to cell 1.
- f) Test system verifies cell 2 remains in the active set.
- g) Test system shall verify that the UE transmit timing offset is still within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- h) Test system stops sending cell 1 signals.
- j) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size

- k) Test system shall verify that the UE transmit timing offset stays within T<sub>0</sub> +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 2.
- l) Test system starts sending cell 1 signal again with its original timing.
- m) Test system verifies that cell 1 is added to the active set.
- n) Test system verifies that the UE transmit timing is still within  $T_0 +/-1.5$  chips with respect to the first detected path of (in time) the downlink DPCCH/DPDCH of cell 2.
- o) Test system stops sending cell 2 signals.
- q) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size and the adjustment rate shall be according to the requirements in section 7.1.2 until the UE transmit timing offset is within  $T_0 + -1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- r) Test system shall verify that the UE transmit timing offset stays within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.

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#### R4-050257

	CHANGE REQUEST	CR-Form-v7
<u>م</u>		<b>4</b> 9
# #	25.133 CR 725 <b># rev 2</b> <sup># Current version:</sup> 4.13.0	<b>0</b> <sup>#</sup>
For <u>HELP</u> on usi	ing this form, see bottom of this page or look at the pop-up text over the 策 sy	/mbols.
Proposed change at	f <b>fects:</b> UICC apps# ME X Radio Access Network Core N	letwork
Title: ೫ (	Correction to DPCH_Ec/lor level in A.7.1 UE Transmit Timing	
Source: ೫ 🤅	BGPP TSG RAN WG4 (Radio)	
Work item code:  🕷	TEI Date: 第 28/02/2005	
	A       Release: \$\$ Rel-4         Use one of the following categories:       Use one of the following regores         F (correction)       2       (GSM Phase 2)         A (corresponds to a correction in an earlier release)       R96       (Release 1996)         B (addition of feature),       R97       (Release 1997)         C (functional modification of feature)       R98       (Release 1998)         D (editorial modification)       R99       (Release 1999)         Detailed explanations of the above categories can       Rel-4       (Release 4)         De found in 3GPP TR 21.900.       Rel-5       (Release 5)         Rel-6       (Release 6)       Rel-6	r) i) i)
	<ul> <li>In A.7.1.2 step k, UE is connected with Cell 2, and Cell 1 is introduced. I situation, the power of Cell 2(-99 dBm) is lower than the power of Cell1(-and the UE perceives DPCH_Ec/lo = -23 dB on cell 2. The UE may not understand the SS on Cell 2 and may drop the link. A link to Cell 2, how necessary for the test purpose.</li> <li>In table A.7.1 DPCH_Ec/lor increased 0.5 dB above demodulation requ AWGN. OCNS_Ec/ lor is adjusted</li> </ul>	96 dBm), ever, is
Consequences if not approved:	* The purpose of the test may not be completed, and good UEs may fail the	ne test
Clauses affected:	육 A.7.1.1	
Other specs affected:	Y       N         X       Other core specifications       %         X       Test specifications       34.121         X       O&M Specifications       34.121	
Other comments:	器 Isolated impact analysis: Will not change UE implementation.	

Equivalent CRs in other Releases: CR724r2 cat. F to 25.133 R99, CR726r2 cat. A

to 25.133 Rel-5, CR727r2 cat. A to 25.133 Rel-6

## A.7.1 UE Transmit Timing

#### A.7.1.1 Test Purpose and Environment

The purpose of this test is to verify that the UE initial transmit timing accuracy, maximum amount of timing change in one adjustment, minimum and maximum adjustment rate are within the specified limits. This test will verify the requirements in section 7.1.2.

For this test two cells on the same frequency are used. Table A.7.1 defines the transmitted signal strengths, the relative timing and the propagation condition used for the two cells.

Parameter	Unit	Level
DPCH_Ec/ lor, Cell 1 and Cell 2	dB	-1 <u>3.5</u> 7
CPICH_Ec/ lor, Cell 1 and Cell 2	dB	-10
PCCPH_Ec/ lor, Cell 1 and Cell 2	dB	-12
SCH_Ec/ lor, Cell 1 and Cell 2	dB	-12
PICH_Ec/ lor, Cell 1 and Cell 2	dB	-15
OCNS_Ec/ lor, Cell 1 and Cell 2	dB	-1. <u>2<mark>05</mark></u>
Î <sub>or,</sub> Cell 1	dBm/3.84 MHz	-96
Î <sub>or,</sub> Cell 2	dBm/3.84 MHz	-99
Information data rate	kbps	12.2
Relative delay of path received from cell 2 with respect to cell 1	μs	+/-2
Propagation condition	A	WGN

Table A.7.1: Test parameters for UE Transmit Timing requirement

#### A.7.1.2 Test Requirements

1

For parameters specified in Table A.7.1, the UE initial transmit timing accuracy, the maximum amount of timing change in one adjustment, the minimum and the maximum adjustment rate shall be within the limits defined in section 7.1.2.

- a) After a connection is set up with cell 1, the test system shall verify that the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected received path (in time) of the downlink DPCCH/DPDCH of cell 1.  $T_0$  is defined in TS 25.211[2].
- b) Test system introduces cell 2 into the test system at delay +2  $\mu$ s from cell 1.
- c) Test system verifies that cell 2 is added to the active set.
- d) Test system shall verify that the UE transmit timing offset is still within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- e) Test system switches Tx timing of cell 2 to a delay of  $-2 \,\mu s$  with respect to cell 1.
- f) Test system verifies cell 2 remains in the active set.
- g) Test system shall verify that the UE transmit timing offset is still within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- h) Test system stops sending cell 1 signals.
- i) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size

- j) Test system shall verify that the UE transmit timing offset stays within  $T_0 + 1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 2.
- k) Test system starts sending cell 1 signal again with its original timing.
- 1) Test system verifies that cell 1 is added to the active set.
- m) Test system verifies that the UE transmit timing is still within  $T_0 + 1.5$  chips with respect to the first significant path of the downlink DPCCH/DPDCH of cell 2.
- n) Test system stops sending cell 2 signals.
- o) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size and the adjustment rate shall be according to the requirements in section 7.1.2 until the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- p) Test system shall verify that the UE transmit timing offset stays within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.

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	CHANGE	REQUEST	CR-Form-v7
<sup>≆</sup> 25	5.133 CR 726	ж <b>rev <mark>2</mark>ж</b>	Current version: <mark>5.13.0</mark> <sup>ℋ</sup>
For <u>HELP</u> on using	this form, see bottom of this	page or look at the	e pop-up text over the X symbols.
Proposed change affe	<i>cts:</i> UICC apps <b>೫</b> <mark></mark>	ME 🗙 Radio Ad	ccess Network Core Network
Title: % Cor	rrection to DPCH_Ec/lor leve	l in A.7.1 UE Trans	smit Timing
Source: # 3G	PP TSG RAN WG4 (Radio)		
Work item code:	ΞI		<b>Date:</b>
Det	e <u>one</u> of the following categories. <b>F</b> (correction) <b>A</b> (corresponds to a correction <b>B</b> (addition of feature), <b>C</b> (functional modification of fe <b>D</b> (editorial modification) tailed explanations of the above found in 3GPP <u>TR 21.900</u> .	n in an earlier release eature)	Release: %Rel-5Use one of the following releases: 2(GSM Phase 2)2(GSM Phase 2)2(Release 1996)R97(Release 1997)R98(Release 1998)R99(Release 1999)Rel-4(Release 4)Rel-5(Release 5)Rel-6(Release 6)
	situation, the power of Cell and the UE perceives DPC understand the SS on Cell necessary for the test purpo	2(-99 dBm) is lowe H_Ec/lo = -23 dB c 2 and may drop the ose. r increased 0.5 dE	and Cell 1 is introduced. In this er than the power of Cell1(-96 dBm), on cell 2. The UE may not e link. A link to Cell 2, however, is 3 above demodulation requirement
Consequences if # not approved:	The purpose of the test ma	y not be completed	d, and good UEs may fail the test
Clauses affected: #	€ <mark>A.7.1.1</mark>		
Other specs भ affected:	YNXOther core specificaXTest specificationsXO&M Specifications	tions ¥ 34.1	21

Other comments:	第 Isolated impact analysis: Will not change UE implementation.
	Equivalent CRs in other Releases: CR724r2 cat. F to 25.133 R99, CR725r2 cat. A
	to 25.133 Rel-4, CR727r2 cat. A to 25.133 Rel-6

## A.7.1 UE Transmit Timing

#### A.7.1.1 Test Purpose and Environment

The purpose of this test is to verify that the UE initial transmit timing accuracy, maximum amount of timing change in one adjustment, minimum and maximum adjustment rate are within the specified limits. This test will verify the requirements in section 7.1.2.

For this test two cells on the same frequency are used. Table A.7.1 defines the transmitted signal strengths, the relative timing and the propagation condition used for the two cells.

Parameter	Unit	Level
DPCH_Ec/ lor, Cell 1 and Cell 2	dB	-1 <u>3.5</u> 7
CPICH_Ec/ lor, Cell 1 and Cell 2	dB	-10
PCCPH_Ec/ lor, Cell 1 and Cell 2	dB	-12
SCH_Ec/ lor, Cell 1 and Cell 2	dB	-12
PICH_Ec/ lor, Cell 1 and Cell 2	dB	-15
OCNS_Ec/ lor, Cell 1 and Cell 2	dB	-1. <u>2<mark>05</mark></u>
Î <sub>or,</sub> Cell 1	dBm/3.84 MHz	-96
Î <sub>or,</sub> Cell 2	dBm/3.84 MHz	-99
Information data rate	kbps	12.2
Relative delay of path received from cell 2 with respect to cell 1	μs	+/-2
Propagation condition	A	WGN

Table A.7.1: Test parameters for UE Transmit Timing requirement

#### A.7.1.2 Test Requirements

1

For parameters specified in Table A.7.1, the UE initial transmit timing accuracy, the maximum amount of timing change in one adjustment, the minimum and the maximum adjustment rate shall be within the limits defined in section 7.1.2.

- a) After a connection is set up with cell 1, the test system shall verify that the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected received path (in time) of the downlink DPCCH/DPDCH of cell 1.  $T_0$  is defined in TS 25.211[2].
- b) Test system introduces cell 2 into the test system at delay +2  $\mu$ s from cell 1.
- c) Test system verifies that cell 2 is added to the active set.
- d) Test system shall verify that the UE transmit timing offset is still within  $T_0 + 1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- e) Test system switches Tx timing of cell 2 to a delay of  $-2 \,\mu s$  with respect to cell 1.
- f) Test system verifies cell 2 remains in the active set.
- g) Test system shall verify that the UE transmit timing offset is still within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
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- j) Test system shall verify that the UE transmit timing offset stays within  $T_0 + 1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 2.
- k) Test system starts sending cell 1 signal again with its original timing.
- 1) Test system verifies that cell 1 is added to the active set.
- m) Test system verifies that the UE transmit timing is still within  $T_0 + 1.5$  chips with respect to the first significant path of the downlink DPCCH/DPDCH of cell 2.
- n) Test system stops sending cell 2 signals.
- o) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size and the adjustment rate shall be according to the requirements in section 7.1.2 until the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- p) Test system shall verify that the UE transmit timing offset stays within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.

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	CHANGE REQUEST						
<sup>೫</sup> 25	5.133 CR 727 <b>xrev</b> 2	₩ Current version: <b>6.8.0</b> <sup>#</sup>					
For <u>HELP</u> on using	this form, see bottom of this page or loo	k at the pop-up text over the X symbols.					
Proposed change affe	<i>cts:</i> UICC apps೫ <mark>─</mark> ME <mark>Ⅹ</mark> Ra	adio Access Network Core Network					
Title: # Co	rrection to DPCH_Ec/lor level in A.7.1 UE	Transmit Timing					
Source: ¥ 3G	PP TSG RAN WG4 (Radio)						
Work item code: ೫ TE	El	<b>Date:</b> ೫ <mark>28/02/2005</mark>					
Det	<ul> <li>a <u>one</u> of the following categories:</li> <li><i>F</i> (correction)</li> <li><i>A</i> (corresponds to a correction in an earlier</li> <li><i>B</i> (addition of feature),</li> <li><i>C</i> (functional modification of feature)</li> <li><i>D</i> (editorial modification)</li> <li>ailed explanations of the above categories categories is cound in 3GPP <u>TR 21.900</u>.</li> </ul>	R97 (Release 1997) R98 (Release 1998) R99 (Release 1999)					
	and the UE perceives DPCH_Ec/lo = -2 understand the SS on Cell 2 and may d necessary for the test purpose.	is lower than the power of Cell1(-96 dBm),					
Consequences if भ not approved:	The purpose of the test may not be con	npleted, and good UEs may fail the test					
Clauses affected: #	8 A.7.1.1						
Other specs अ affected:	YNXOther core specificationsXTest specificationsXO&M Specifications	34.121					

Other comments:	ж	Isolated impact analysis: Will not change UE implementation.
		Equivalent CRs in other Releases: CR724r2 cat. F to 25.133 R99, CR725r2 cat. A
		to 25.133 Rel-4, CR726r2 cat. A to 25.133 Rel-5

## A.7.1 UE Transmit Timing

#### A.7.1.1 Test Purpose and Environment

The purpose of this test is to verify that the UE initial transmit timing accuracy, maximum amount of timing change in one adjustment, minimum and maximum adjustment rate are within the specified limits. This test will verify the requirements in section 7.1.2.

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OCNS_Ec/ lor, Cell 1 and Cell 2	dB	-1. <u>2<mark>05</mark></u>
Î <sub>or,</sub> Cell 1	dBm/3.84 MHz	-96
Î <sub>or,</sub> Cell 2	dBm/3.84 MHz	-99
Information data rate	kbps	12.2
Relative delay of path received from cell 2 with respect to cell 1	μs	+/-2
Propagation condition	A	WGN

Table A.7.1: Test parameters for UE Transmit Timing requirement

#### A.7.1.2 Test Requirements

1

For parameters specified in Table A.7.1, the UE initial transmit timing accuracy, the maximum amount of timing change in one adjustment, the minimum and the maximum adjustment rate shall be within the limits defined in section 7.1.2.

- a) After a connection is set up with cell 1, the test system shall verify that the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected received path (in time) of the downlink DPCCH/DPDCH of cell 1.  $T_0$  is defined in TS 25.211[2].
- b) Test system introduces cell 2 into the test system at delay +2  $\mu$ s from cell 1.
- c) Test system verifies that cell 2 is added to the active set.
- d) Test system shall verify that the UE transmit timing offset is still within  $T_0 + 1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- e) Test system switches Tx timing of cell 2 to a delay of  $-2 \,\mu s$  with respect to cell 1.
- f) Test system verifies cell 2 remains in the active set.
- g) Test system shall verify that the UE transmit timing offset is still within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- h) Test system stops sending cell 1 signals.
- i) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size

- j) Test system shall verify that the UE transmit timing offset stays within  $T_0 + 1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 2.
- k) Test system starts sending cell 1 signal again with its original timing.
- 1) Test system verifies that cell 1 is added to the active set.
- m) Test system verifies that the UE transmit timing is still within  $T_0 + 1.5$  chips with respect to the first significant path of the downlink DPCCH/DPDCH of cell 2.
- n) Test system stops sending cell 2 signals.
- o) Test system verifies that UE transmit timing adjustment starts no later than the time when the whole active set update message is available at the UE taking the RRC procedure delay into account. The adjustment step size and the adjustment rate shall be according to the requirements in section 7.1.2 until the UE transmit timing offset is within  $T_0 +/-1.5$  chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.
- p) Test system shall verify that the UE transmit timing offset stays within  $T_0$  +/- 1.5 chips with respect to the first detected path (in time) of the downlink DPCCH/DPDCH of cell 1.