TSG-RAN meeting #19 RP-030094
Birmingham, UK
March 11 – 14 2003

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1#30: Four documents were covered. Three of these documents concluded the reference configuration in TR25.895. There were contributions covering midamble sequences, physical layer procedures and some minor aspects. The reference configuration defined in the TR is based on the 3.84Mcps TDD option and shows a minimum set of deviations from the Release 5 HCR-TDD standards. A document covering link level assumptions was agreed.

RAN1#31: Four documents were covered. Text proposals from three of these four documents were accepted with comments and have been included in TR25.895. The areas that were addressed in RAN1#31 were : system level simulation assumptions, backward compatibility aspects and link level simulation results for some HSDPA fixed rate reference channels.

List of Completed elements (for complex work items):

- Higher chip rate reference configuration.
- Simulation assumptions

List of open issues:

- performance results
- Link level performance, system level performance and complexity analyses.
- Feasibility analysis.

Estimates of the level of completion (when possible):

30%

SI completion date review resulting from the discussion at the working group:

Owing to the change in the RAN1 meeting schedule and the work still required for completion of the SI, it is considered that Dec 2003 is a more realistic completion date than June 2003. It is proposed that the SI completion date is changed to Dec 2003.

References to WG's internal documentation and/or TRs:

TR25.895 v1.0.0 is presented for information to TSG-RAN in the following document :

RP-030095 “TR25.895 v1.0.0 : Analysis of higher chip rates for UTRA TDD evolution”