TSG-RAN Meeting No. 14 *TSGRP-010893*
December 11-14, 2001 Kyoto, Japan

Status Report for SI to TSG

Study Item Name: Mitigating the Effect of CPICH Interference at the UE

SOURCE: Rapporteur (Shimon Moshavi, Intel) **TSG:** RAN **WG: 4**

E-mail address rapporteur: Shimon.Moshavi@intel.com

Ref. to WI sheet: RAN_Work_Items.doc, Study Item 8

Progress Report since the last TSG (for all involved WGs):

Several contributions were presented at the RAN4 meeting in November as part of this Study [15-19]. Version 1.0.0 of the Study's Technical Report was presented and endorsed by RAN4 [15]. Extensive simulation results addressing feasible mitigation accuracy in a multi-cell scenario were presented in [16]. Some additional preliminary link level simulations were also presented in [17]. In addition, a number of relevant issues were brought up in [18] and discussed at the meeting, such as CPICH interference mitigation when utilizing HSDPA.

To date, there have been a significant number of contributions to the Study addressing the gains and feasibility of CPICH interference mitigation. Based on the work already completed, RAN Work Group 4 endorsed a Work Item proposal on this topic to be presented at the current RAN meeting.

List of Completed elements (for complex work items):

In addition to background material [1-4,6,7], the Study has addressed 3 main areas:

- Radio Network Simulations to Evaluate Capacity Gains - Extensive voice capacity simulations were reported by Intel, Nokia, Motorola, and Telia, with compatible results [8-12]. In addition, one set of data capacity simulations (for 64 kbps and 144 kbps services) was presented illustrating increased gains over the voice capacity scenario [9]. Reference [12] also addressed scenarios where CPICH power is constrained to be large due to regulatory requirements.
- Link Level Simulations to Evaluate Feasible Accuracy of Cancellation: Reference [9] reported extensive simulation results illustrating a relatively high degree of cancellation accuracy for the cases considered. Reference [13] considered the performance of CPICH mitigation under extreme pessimistic timing error conditions, and found that gains remain, although reduced. Reference [16] found relatively high cancellation accuracy is feasible even in a 7-sector scenario, which included both stronger cells in a handover state, and weaker neighbor cells.
- Complexity - Reference [5] addressed the implementation complexity of mitigating CPICH interference effects by providing upper bounds on gate count, DSP requirements, and current consumption. Reference [14] considered gate count and confirmed the results in [5]. Reference [9] extended the complexity assessment to Transmit Diversity and Multi-Code operation. Reference [19] corrected the power consumption estimate given in [5].

List of open issues:

At the November RAN4 meeting, certain companies expressed interest in performing their own additional verification of the simulation and complexity results for the Study. In addition, several performance and complexity issues were raised, (e.g., relating to capacity gain, power consumption, HSDPA). After extensive discussions addressing these issues, RAN4 felt it appropriate to endorse a Work Item proposal, although the decision was reached without unanimity.

Estimates of the level of completion (when possible):

80%

WI completion date review resulting from the discussion at the working group:

March 2002

References to WG's internal documentation and/or TRs:

[1] 3GPP TSGR1-00-1371, “CPICH interference cancellation as a means for increasing DL capacity,” Intel Corporation, Nov. 2000.

[2] 3GPP TSGR1-00-0030, “Further Results on CPICH Interference Cancellation as A Means for Increasing DL Capacity,” Intel Corporation, Jan. 2001.

[3] 3GPP TSGR4-01-0238, “CPICH Interference Cancellation as a Means for Increasing DL Capacity,” Intel Corporation, Feb. 2001.

[4] 3GPP TSGRP-01-0177, “Mitigating the Effect of CPICH Interference at the UE,” Intel Corporation, Mar. 2001.

[5] 3GPP TSGR4-01-0650, “On the Implementation Complexity of CPICH Interference Cancellation,” Intel Corporation, May 2001.

[6] 3GPP TSGR4-01-1014, “On the potential capacity gain of CPICH interference mitigation,” Intel Corporation, July 2001.

[7] 3GPP TSGR4-01-1015, “Study description for SI: Mitigating the effect of CPICH interference at the UE,” Intel Corporation, July 2001.

[8] 3GPP TSGR4-01-0967, “CPICH cancellation,” Motorola, July 2001.

[9] 3GPP TSGR4-01-1330, “Feasibility Assessment for CPICH Interference Mitigation”, Intel Corporation, September 2001.

[10] 3GPP TSGR4-01-1230, “CPICH cancellation, 2-way soft handoff capacity gain” Motorola, September 2001.

[11] 3GPP TSGR4-01-1202, “Simulation results for CPICH interference mitigation” Nokia, September 2001.

[12] 3GPP TSGR4-01-1256, “Capacity gain from CPICH cancellation”, Telia, September 2001.

[13] 3GPP TSGR4-01-1231, “CPICH cancellation, UE sample time offset” Motorola, September 2001.

[14] 3GPP TSGR4-01-1232, “CPICH cancellation complexity” Motorola, September 2001.

[15] 3GPP TSGR4-011499, “TR 25.991 V1.0.0 Feasibility Study of the Mitigation of the Effect of the Common Pilot Channel (CPICH) Interference at the User Equipment,” Rapporteur, Nov. 2001.

[16] 3GPP TSGR4-011455, “CPICH Interference Mitigation Accuracy,” Intel Corp., Nov. 2001.

[17] 3GPP TSGR4-011453, “Link Level Simulation Results for CPICH Cancellation,” Nokia, Nov. 2001

[18] 3GPP TSGR4-011392, “Comments on the CPICH Interference Cancellation Scheme,” Ericsson, Nov. 2001.

[19] 3GPP TSGR4-011483, “Correction on CPICH Interference Mitigation Complexity”, Intel Corp. Nov. 2001.