

Agenda Item: **6.4**

Source: **Broadcom**

Title: **An ARP Base 4 hardware saving, flexible granularity and flexible parallelism ARP interleaver suitable for all possible block sizes in 3GPP LTE Turbo Codes**

Document for: **Discussion**

1 Introduction

In this document we introduce an ARP base 4 (almost regular permutation) interleaver structure that is suitable for all possible block sizes of 3GPP LTE turbo codes. The benefits given by these 4 interleaver structures are the following:

- 1) **Hardware saving:** a) multiplication of a variable number to a variable P in normal ARP interleaves becomes a constant scaling; b) Simple implementation (different to Rel.6 interleave [1] the ARP interleaver is given by a closed formula); c) the storage of the interleaver parameters is smaller, instead of about 108 for Rel.6 interleaves, only 29 parameters are needed.
- 2) **Flexible granularity:** The ARP interleavers are suitable for any possible block sizes minimizing the addition of dummy bits. This is especially useful for parallel decoding since the pruning technique suggested in Rel.6 may not be suitable for parallel decoding.
- 3) **Flexible parallelism:** The degree of parallelism can be any number from 1 up to the dithering cycle of the ARP and more. This flexible structure will reduce HW power consumption and ASIC clock requirement.
- 4) **Good performance:** the performances of the ARP interleavers are better than or equivalent to those obtained from Rel.6 interleavers.

Remarks: *Due to the limitation of search time, instead of base 4, in this document we use base 6 interleaver structure. We believe it is possible to have base 4 interleave structure if we have enough time to search.*

2 Almost regular permutation (ARP)

An almost regular permutation (ARP) of size $L = CW$ (i.e. C is a divider of L) introduced in [2] is defined by

$$i = \pi(j) = jP + \theta + A(j \bmod C)P + B(j \bmod C) \pmod{L}$$

where P is relative prime to L, θ is a constant and $A(x)$ and $B(x)$ are integer function defined on $\{0, 1, \dots, C - 1\}$. To insure the function defined the function is a permutation (i.e. one to one and on to), in [2] $A(x)$ and $B(x)$ are further restricted to

$$A(i)P + B(i) = C[\alpha(i)P + \beta(i)], i = 0, \dots, C - 1$$

where α and β are integer functions. In this document, we call C the *dithering cycle* of the ARP.

3 Problems on parallel turbo decoding

In order to carry on degree m parallel decoding, a contention-free memory map, which maps the values output from the m parallel processors to the different memory banks, is needed. On the other hand, 3GPP LTE turbo coding has to support any block size from 40 up to 8192 or more. With the limited number of interleaves (about 500 interleaves in 3GPP TS 25.212 (V6.8.0, called Rel.6)[1]), the pruning technique is introduced, that is adding the dummy bits to the information block that is not a given interleave size and pruned them away from the output of the interleaved data. However, this pruning technique will cause problem on the contention-free map since the map is defined on the original (pre-pruned) interleave size. Therefore, pruning technique may be too difficult for efficient implementation. That means the dummy bits have to be added to the code block. However, if we do not carefully choose the interleavers, adding dummy bits may induce significant overhead. For example, using Rel.6 interleave for a block size 2304 (listed in the simulation blocks for [3]) 216 (9.3%) dummy bits need to be added.

4 Proposed ARP interleaves

In this document, we propose a set of 4 base ARP interleaves for any all possible block size from 40 to 8192. We choose P be a fixed prime, i.e. 1021. In this way, multiply P in the ARP becomes scaling, which saves hardware area and power. Only 4 different dithering cycle C and 4 different periodic function pairs $(\alpha(x), \beta(x))$ are used, namely

- 1) Block size $40 \sim R_1$: $C=3$ and using $(\alpha_3(x), \beta_3(x))$;
- 2) Block size $R_1+1 \sim R_2$: $C=4$ and using $(\alpha_4(x), \beta_4(x))$;
- 3) Block size $R_2+1 \sim R_3$: $C=8$ and using $(\alpha_8(x), \beta_8(x))$;
- 4) Block size $R_3+1 \sim 8192$: $C=10$ and using $(\alpha_{10}(x), \beta_{10}(x))$.

Remark: As we mentioned in Section 1, due to the limited searching time, we tentatively use base 6 interleaver structures. Here is the possible 6 interleavers.

- 1) Block size $40 \sim 299$: $C=3$ and using $(\alpha_3(x), \beta_3(x))$;
- 2) Block size $300 \sim 499$: $C=4$ and using $(\alpha_{4,1}(x), \beta_{4,1}(x))$;
- 3) Block size $500 \sim 999$: $C=4$ and using $(\alpha_{4,2}(x), \beta_{4,2}(x))$;
- 4) Block size $1000 \sim 1999$: $C=8$ and using $(\alpha_{8,1}(x), \beta_{8,1}(x))$;
- 5) Block size $2000 \sim 4999$: $C=8$ and using $(\alpha_{8,2}(x), \beta_{8,2}(x))$;
- 6) Block size $5000 \sim 8192$: $C=10$ and using $(\alpha_{10}(x), \beta_{10}(x))$.

In general, given any information sequence of block size L, one can find L its corresponding region among 1) to 4) and its dithering cycle C. The ARP interleaves, the largest number of the dummy bits need to be added, and the possible parallel degrees are listed in the following table (where $[]$ is the ceiling function).

Block size L	C	Interleave size N	ARP	Parallel degree	maximal dummy bits
$40 \sim R_1$	3	$3*[L/2]$	$\{1021*x+\theta_3+3*[\alpha_2(x \bmod 3)*1021+\beta_3(x \bmod 3)]\} \bmod N$	1,2,3 (and 4,...,3v if $3v N, v>1$)	2

$R_1+1 \sim R_2$	4	$4*[L/4]$	$\{1021*x+\theta_4+4*[\alpha_4(x \bmod 4)*1021+\beta_4(x \bmod 4)]\} \bmod N$	1,2,3,4 (and 5,...,4v if $4v N, v>1$)	3
$R_2+1 \sim R_3$	8	$8*[L/8]$	$\{1021*x+\theta_8+8*[\alpha_8(x \bmod 8)*1021+\beta_8(x \bmod 8)]\} \bmod N$	1,2,3,4,5,6,7,8 (and 9,..., 8v if $8v N, v>1$)	7
$R_3+1 \sim 8192$	10	$10*[L/10]$	$\{1021*x+\theta_{10}+10*[\alpha_{10}(x \bmod 10)*1021+\beta_{10}(x \bmod 10)]\} \bmod N$	1,2,3,4,5,6,7,8, 9,10 (and 11,..., $10v$ if $10v N, v>1$)	9

Remark: As we mentioned in Section 1, due to the limited searching time, we tentatively use base 6 interleaver structures. Here is the possible 6 interleavers.

Block size L	C	Interleave size N	ARP	Parallel degree	maximal dummy bits
40~299	3	$3*[L/3]$	$\{1021*x+\theta_3+3*[\alpha_3(x \bmod 3)*1021+\beta_3(x \bmod 3)]\} \bmod N$	1,2,3 (and 4,...,3v if $3v N, v>1$)	2
300~499	4	$4*[L/4]$	$\{1021*x+\theta_{4,1}+4*[\alpha_{4,1}(x \bmod 4)*1021+\beta_{4,1}(x \bmod 4)]\} \bmod N$	1,2,3,4 (and 5,...,4v if $4v N, v>1$)	3
500~999	4	$4*[L/4]$	$\{1021*x+\theta_{4,2}+4*[\alpha_{4,2}(x \bmod 4)*1021+\beta_{4,2}(x \bmod 4)]\} \bmod N$	1,2,3,4 (and 5,...,4v if $4v N, v>1$)	3
1000~1999	8	$8*[L/8]$	$\{1021*x+\theta_{8,1}+8*[\alpha_{8,1}(x \bmod 8)*1021+\beta_{8,1}(x \bmod 8)]\} \bmod N$	1,2,3,4,5,6,7,8 (and 9,..., 8v if $8v N, v>1$)	7
2000~4999	8	$8*[L/8]$	$\{1021*x+\theta_{8,2}+8*[\alpha_{8,2}(x \bmod 8)*1021+\beta_{8,2}(x \bmod 8)]\} \bmod N$	1,2,3,4,5,6,7,8 (and 9,..., 8v if $8v N, v>1$)	7
5000~8192	10	$10*[L/10]$	$\{1021*x+\theta_{10}+10*[\alpha_{10}(x \bmod 10)*1021+\beta_{10}(x \bmod 10)]\} \bmod N$	1,2,3,4,5,6,7,8, 9,10 (and 11,..., $10v$ if $10v N, v>1$)	9

The interleave parameters (subject to change due to the ongoing simulations) are given in the following table

L	C	θ	Interleave size N	$\alpha_C(0), \alpha_C(1), \dots, \alpha_C(C-1)$	$\beta_C(0), \beta_C(1), \dots, \beta_C(C-1)$
40~299	3	7	$3*[L/3]$	0 0 1	15,16,15
300~499	4	3	$4*[L/4]$	0, 0, 1, 1	127 197 147 218
500~999	4	7	$4*[L/4]$	0, 0, 1, 0	149 106 13 120
1000~1999	8	7	$8*[L/8]$	0 0 1 1 0 1 0 0	496 198 151 478 366 376 21 129
2000~4999	8	7	$8*[L/8]$	1 1 0 0 0 1 1 1	414 141 130 249 67 117 490 280

5000~8192	10	0	10*[L/10]	1 0 1 0 0 0 0 0 1 1	360 278 127 486 322 4 325 273 288 206
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Parallel degrees for 42 information block sizes

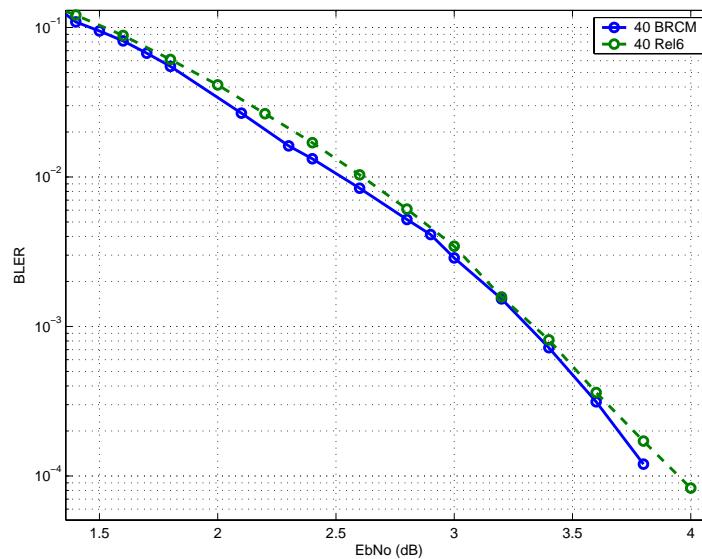
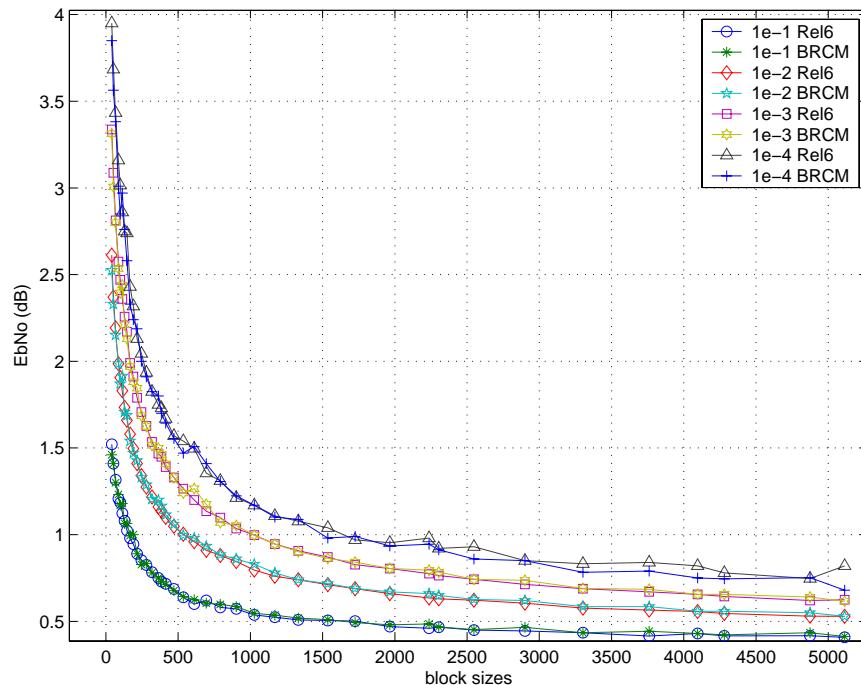
infor size	Interleave size N	Parallel degree
40	42	1,2,3,4,5,6,...
52	54	1,2,3,4,5,6,7,8,9,...
67	69	1,2,3,...
87	87	1,2,3,...
99	99	1,2,3,4,5,6,7,8,9,...
113	114	1,2,3,4,5,6,...
129	129	1,2,3,...
146	147	1,2,3,4,5,6,...
167	168	1,2,3,4,5,6,7,8,9,...
190	192	1,2,3,4,5,6,7,8,9,...
216	216	1,2,3,4,5,6,7,8,9,...
246	246	1,2,3,4,5,6,...
280	282	1,2,3,4,5,6,...
319	320	1,2,3,4,5,6,...,20,...
363	364	1,2,3,4,...,28,...
384	384	1,2,3,4,5,6,7,8,...,16,...
414	416	1,2,3,4,5,6,7,8,...,16,...
471	472	1,2,3,4,5,6,7,8,...
536	536	1,2,3,4,5,6,7,8,...
611	612	1,2,3,4,5,6,7,8,...,12,...
695	696	1,2,3,4,5,6,7,8,...,24,...
792	792	1,2,3,4,5,6,7,8,...,24,...
902	904	1,2,3,4,5,6,7,8,...
1027	1032	1,2,3,4,5,6,7,8,...,24,...
1169	1176	1,2,3,4,5,6,7,8,...,24,...
1331	1336	1,2,3,4,5,6,7,8,...
1536	1536	1,2,3,4,5,6,7,8,...,24,...
1725	1728	1,2,3,4,5,6,7,8,...,24,...
1965	1968	1,2,3,4,5,6,7,8,...,24,...
2237	2240	1,2,3,4,5,6,7,8,...,32,...
2304	2304	1,2,3,4,5,6,7,8,...,24,...
2547	2552	1,2,3,4,5,6,7,8,...
2900	2904	1,2,3,4,5,6,7,8,...,24,...
3302	3304	1,2,3,4,5,6,7,8,...,56,...
3760	3760	1,2,3,4,5,6,7,8,...,40,...
4096	4096	1,2,3,4,5,6,7,8,...,32,...
4281	4288	1,2,3,4,5,6,7,8,...,32,...
4874	4880	1,2,3,4,5,6,7,8,...,40,...
5550	5550	1,2,3,4,5,6,7,8,9,10,...,30,...
6144	6150	1,2,3,4,5,6,7,8,9,10,...,30,...

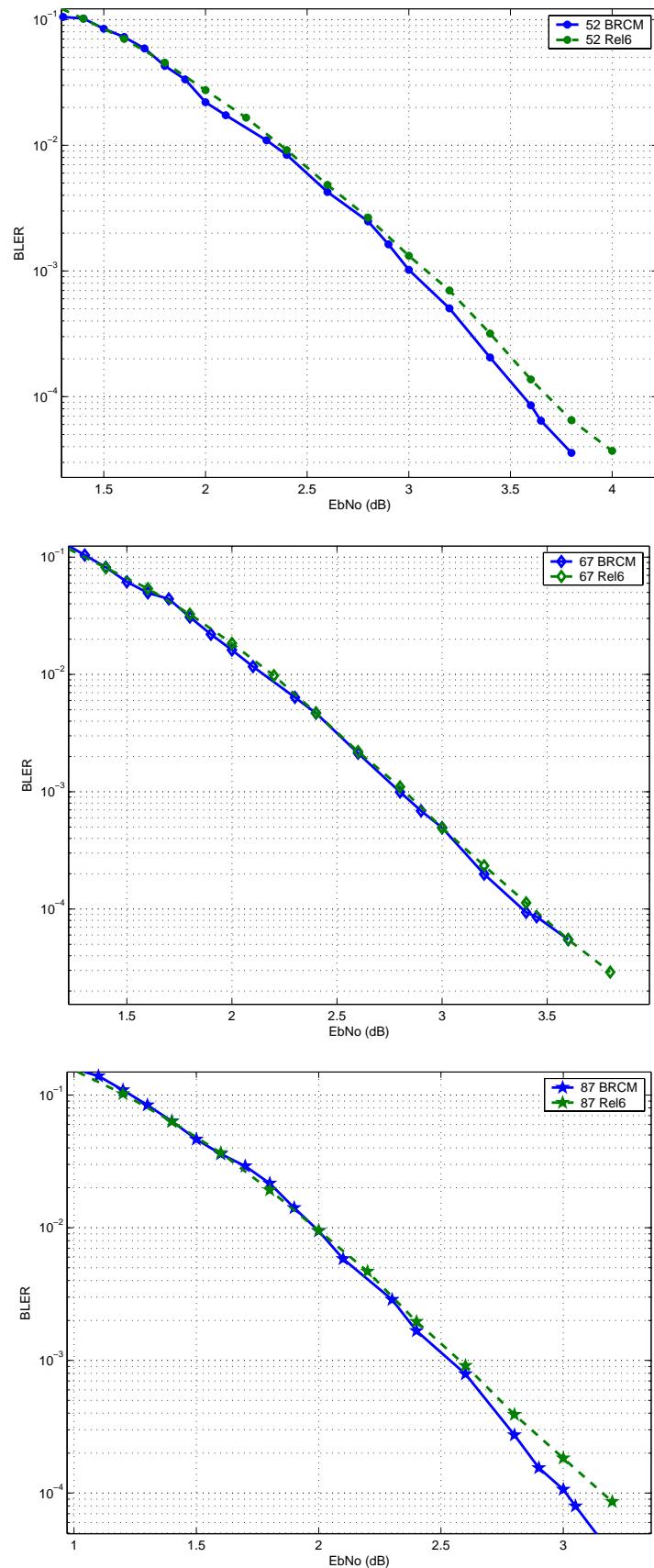
7195	7200	1,2,3,4,5,6,7,8,9,10,...,30,...
8192	8200	1,2,3,4,5,6,7,8,9,10,...,30,...

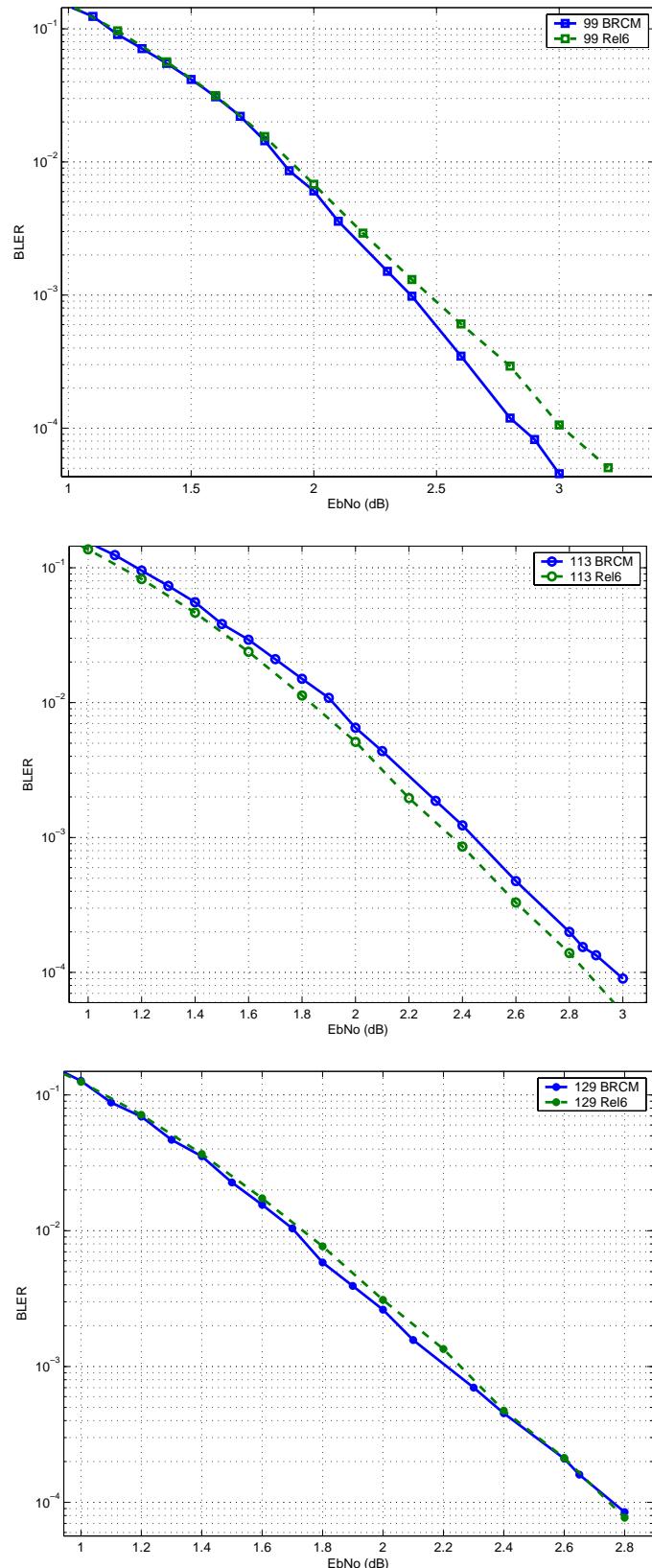
5 Performance comparing to interleavers in Rel6

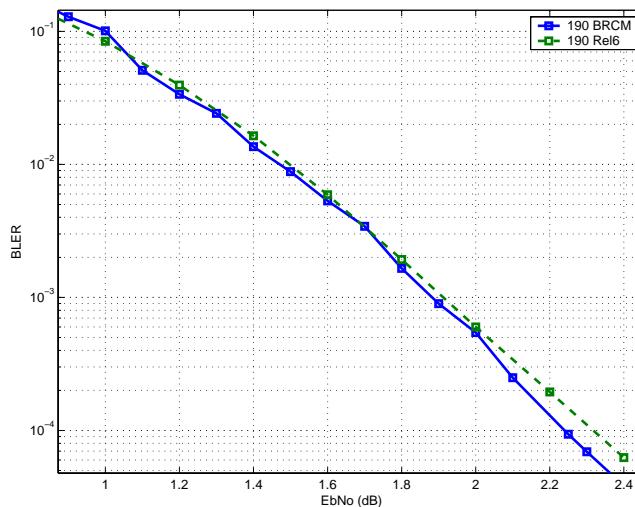
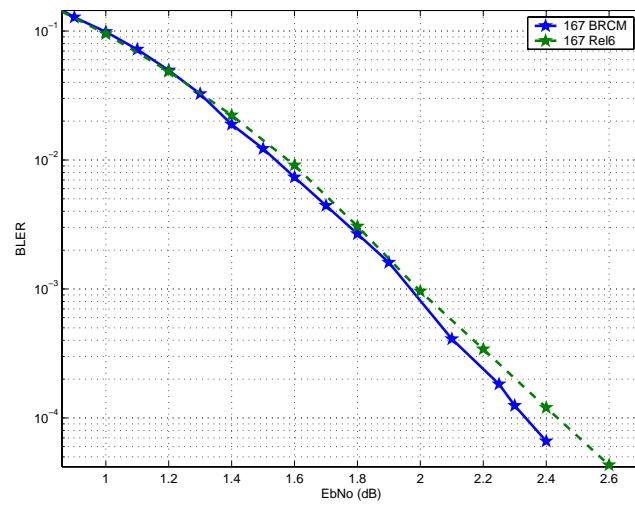
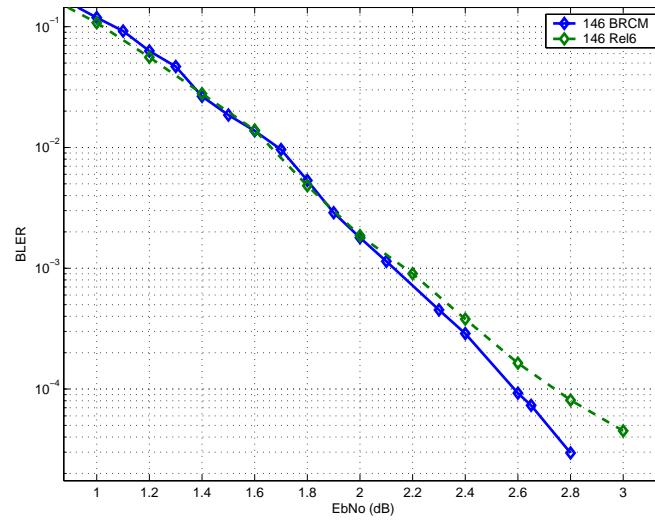
Remark: Due to the simplification of our interleavers comparing to the interleavers in Rel6 (there are more than 400 different interleaves in Rel6), there might be a tiny performance loss (about 0.05dB) for about 6 block sizes among 39 block sizes. The performances with other block sizes are better or equal to what Rel6 interleaves can offer.

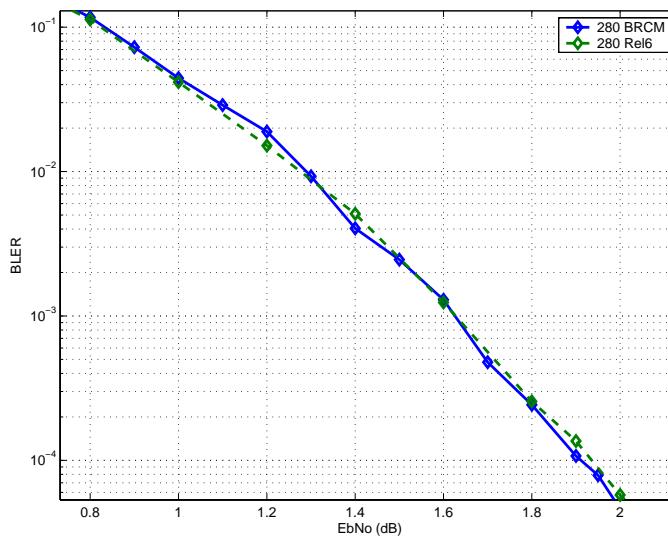
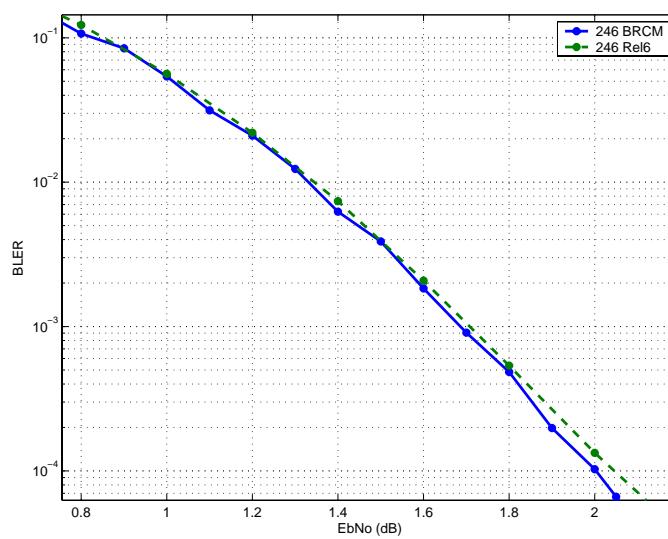
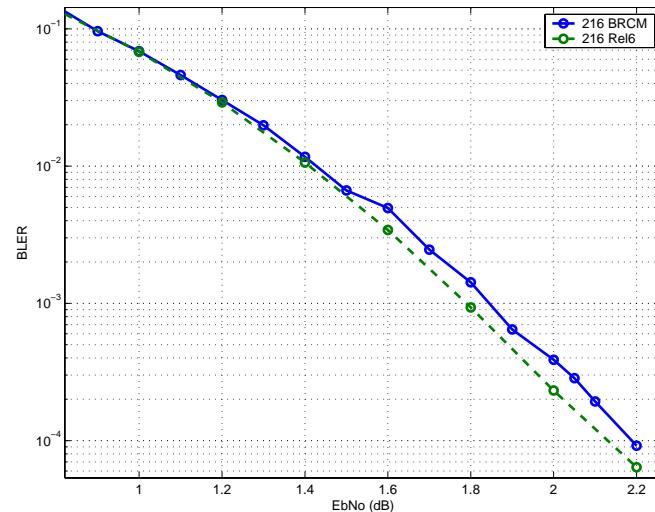
The first picture shows the difference over BER=1e-1,1e-2,1e-3 and 1e-4 and the rest is the detailed comparison for every individual block sizes listed in Riga meeting.

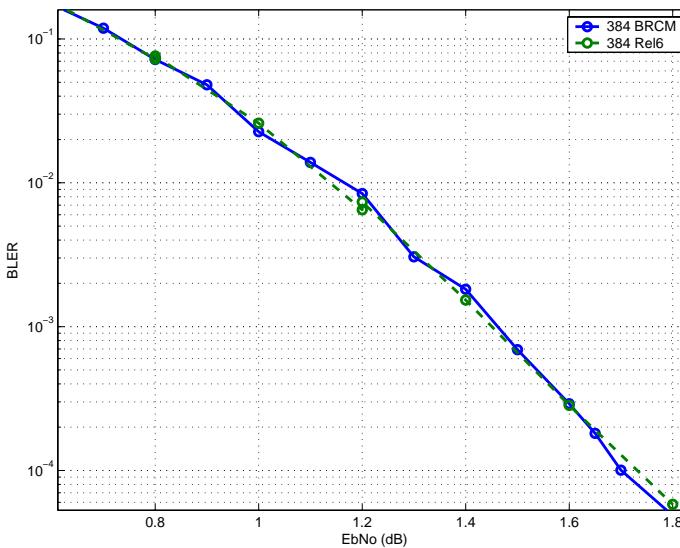
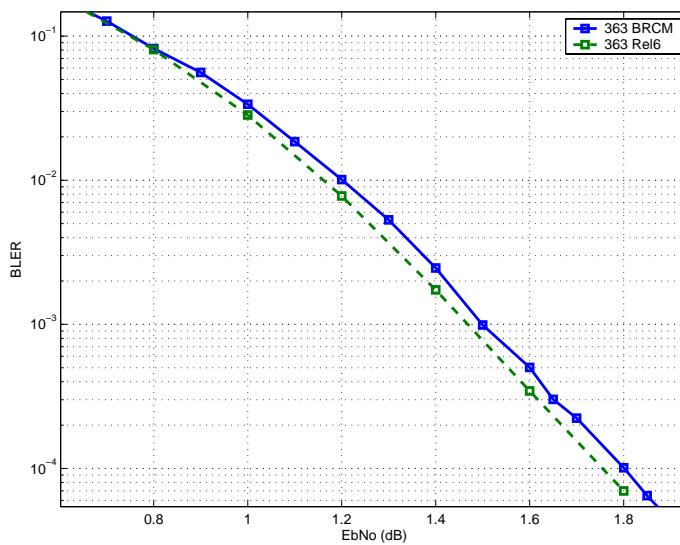
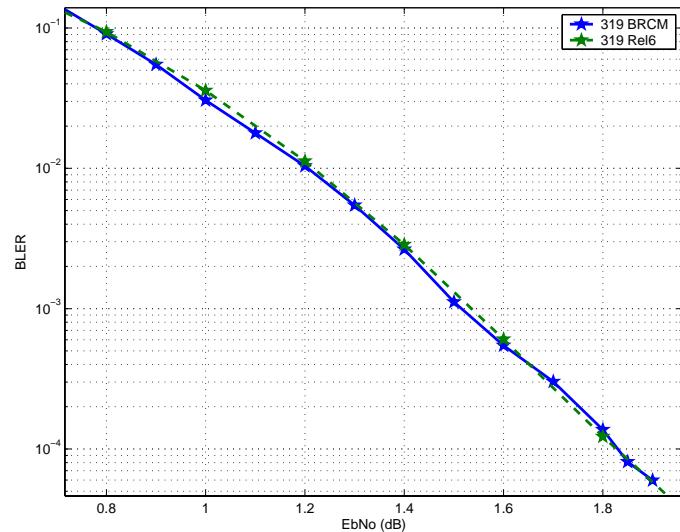


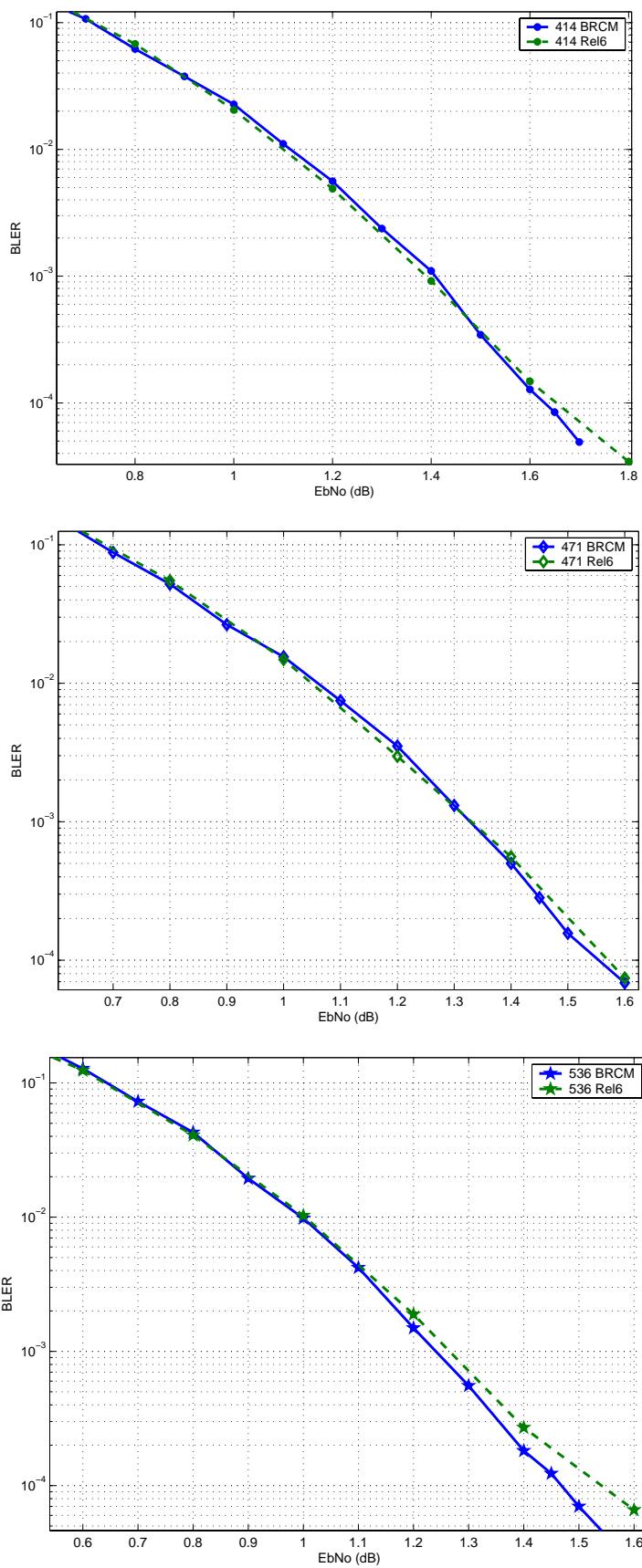


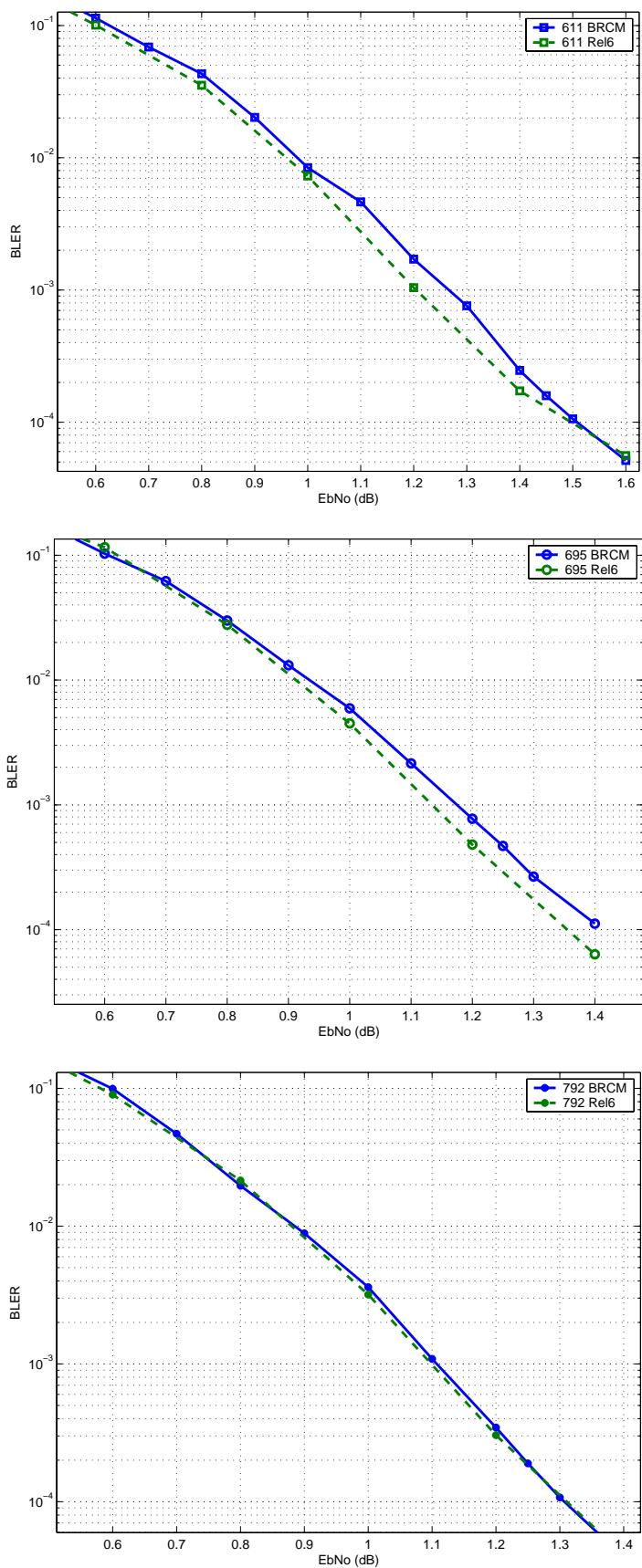


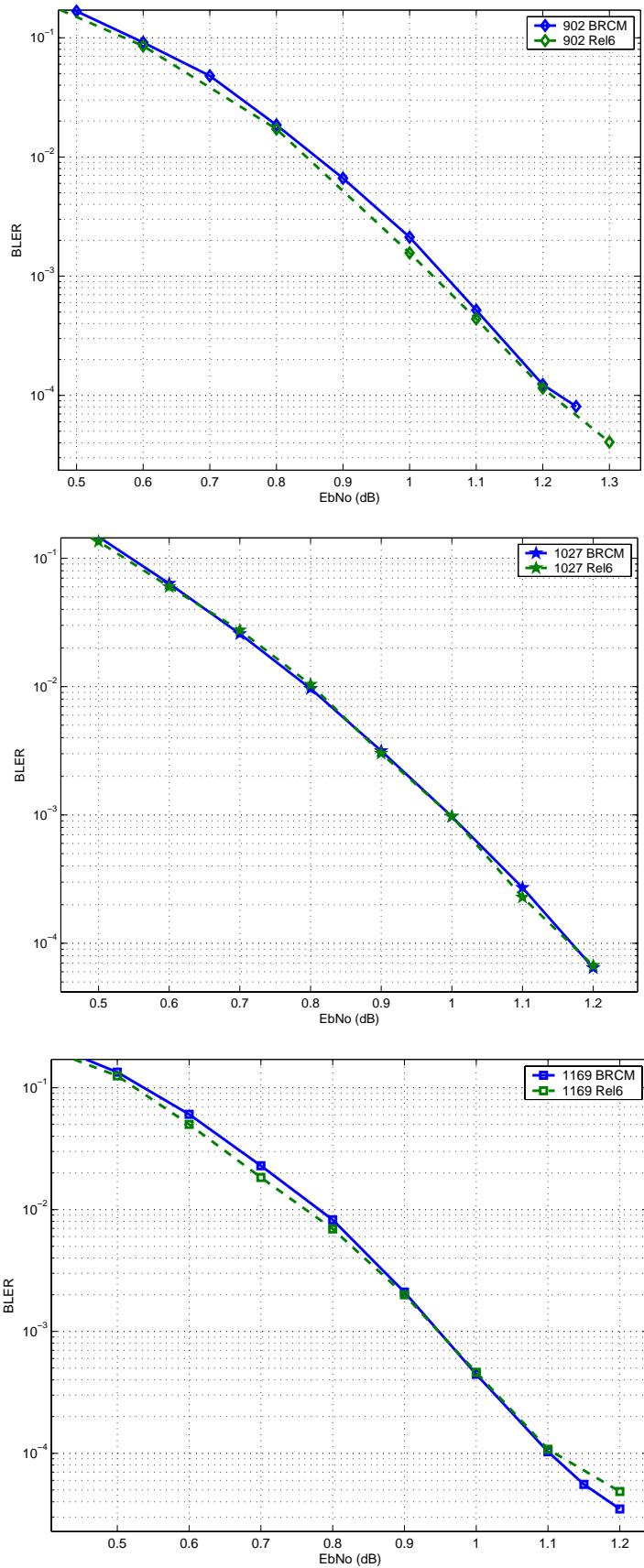


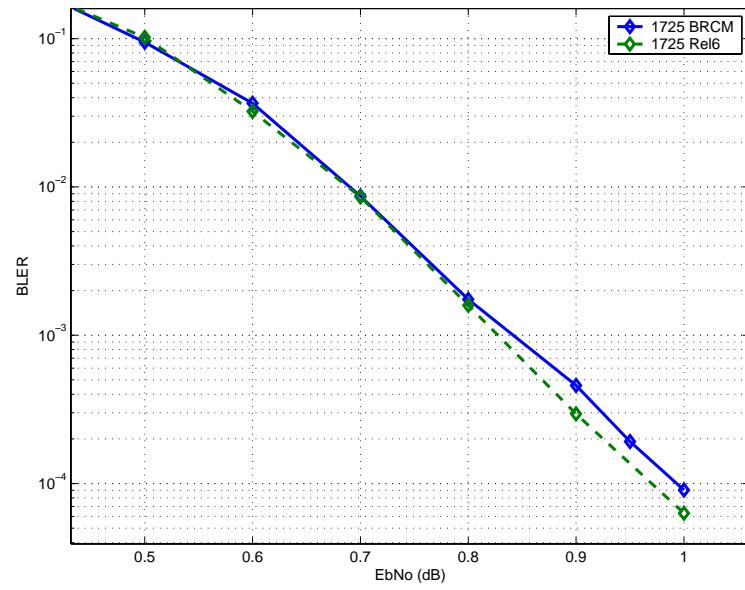
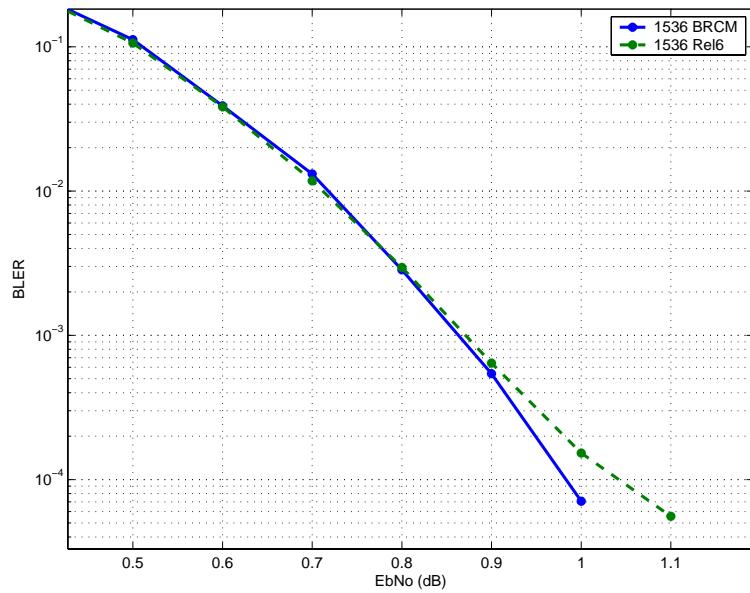
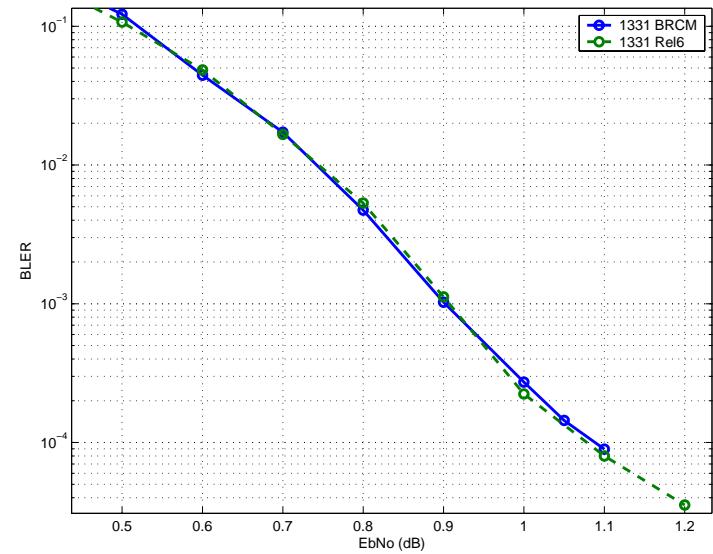


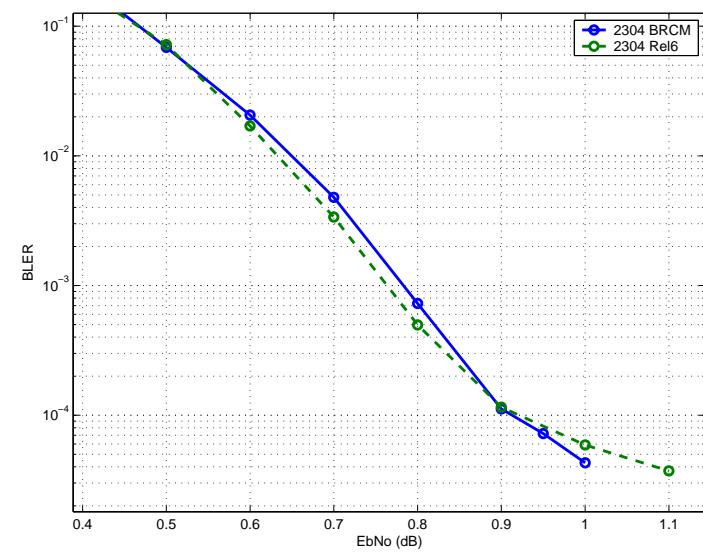
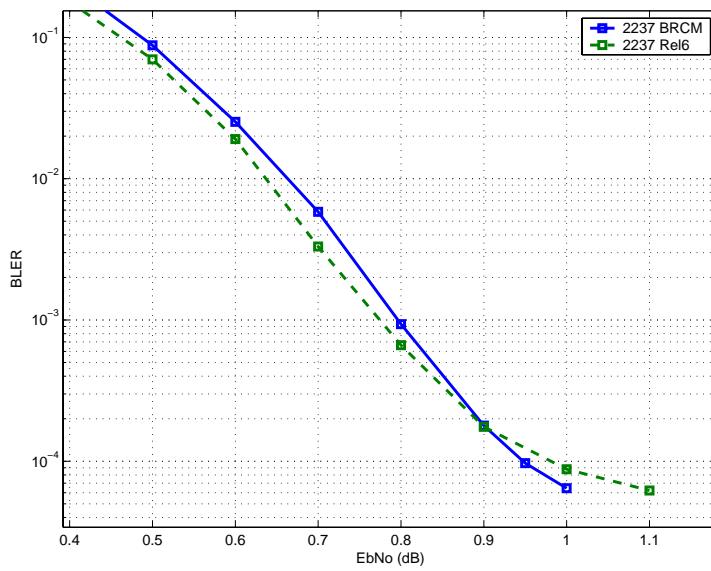
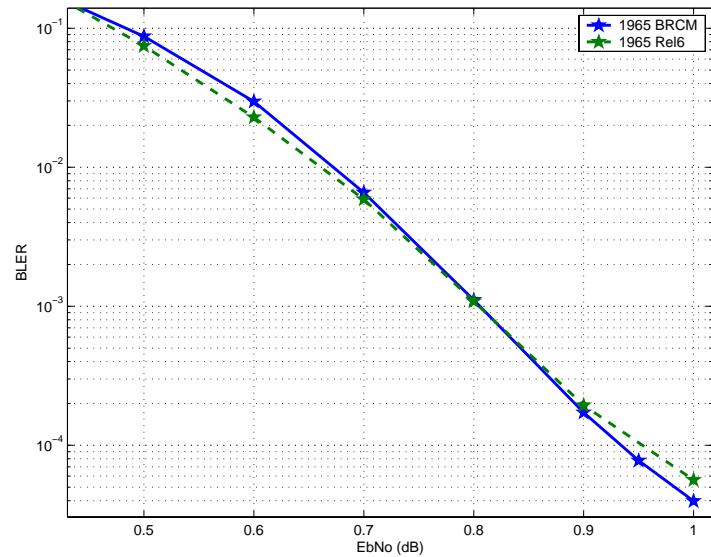


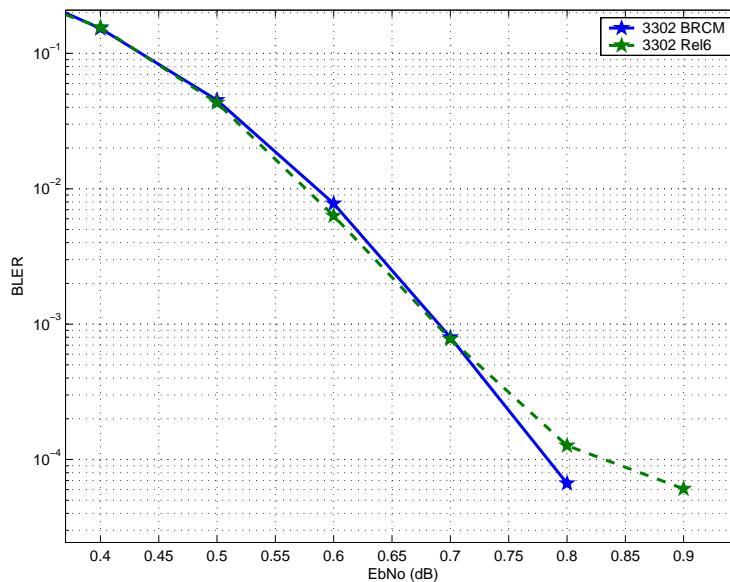
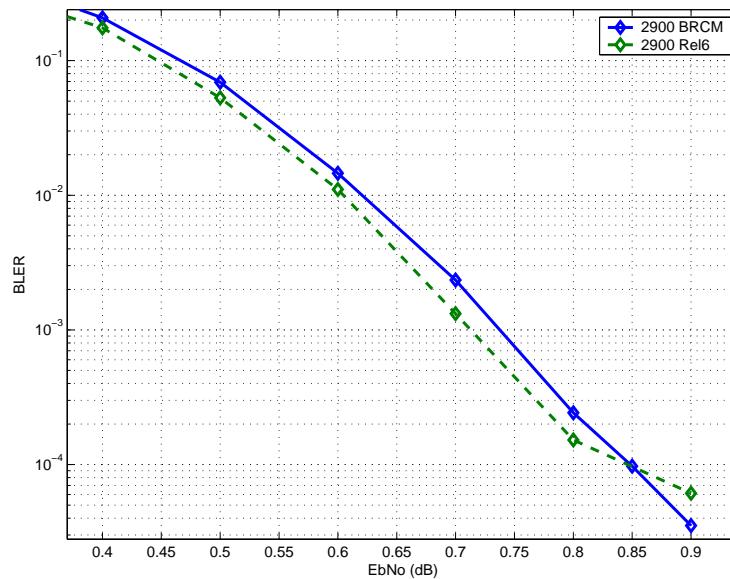
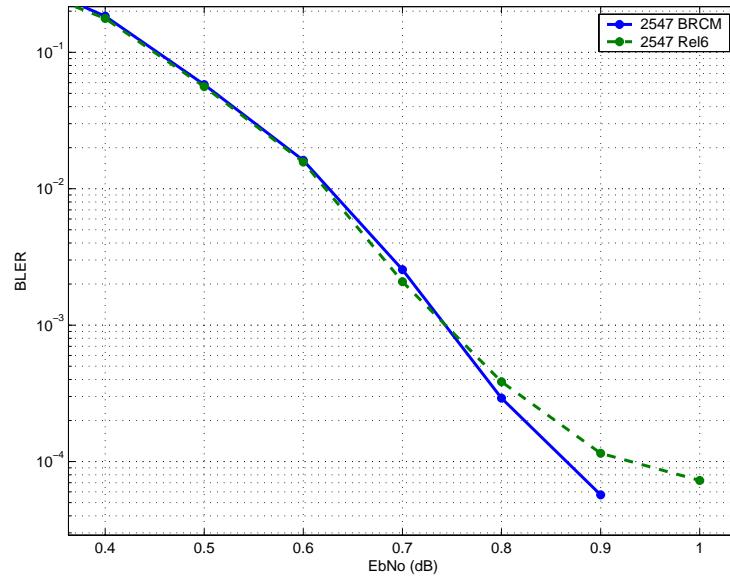


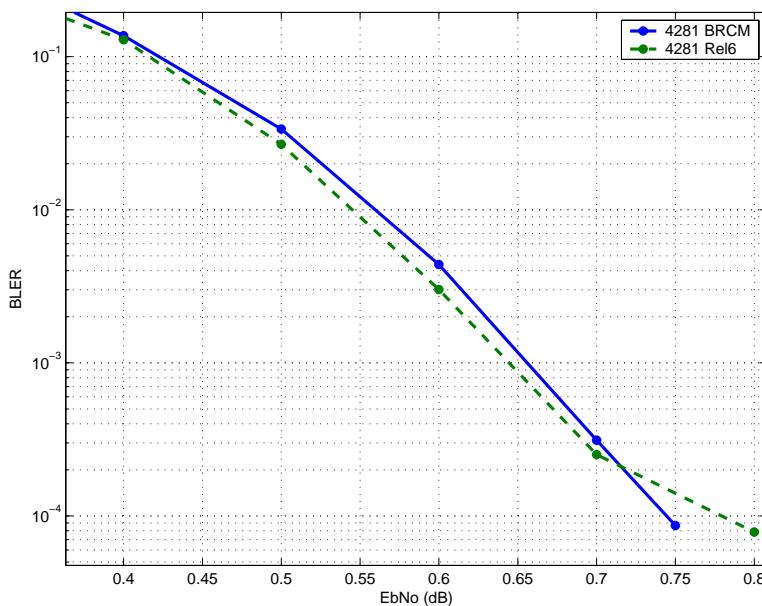
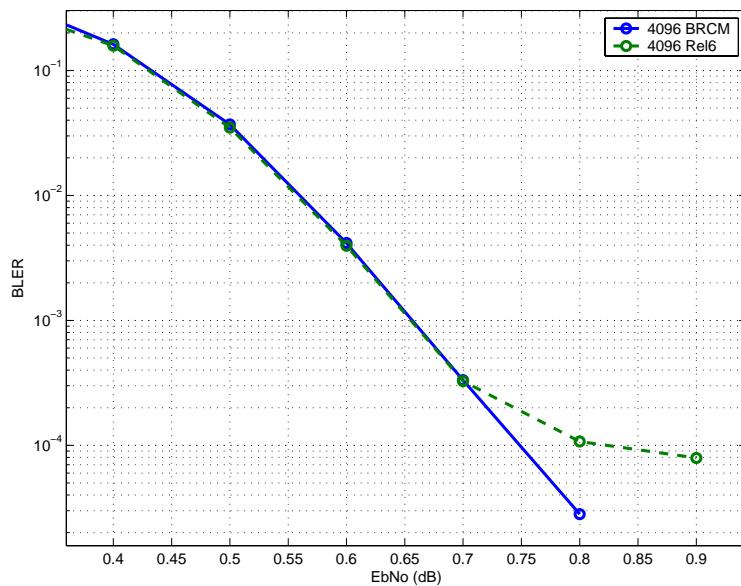
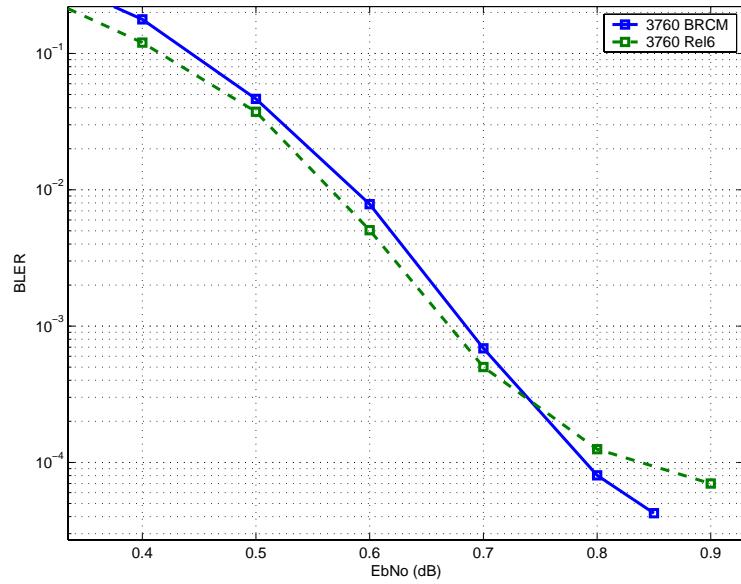


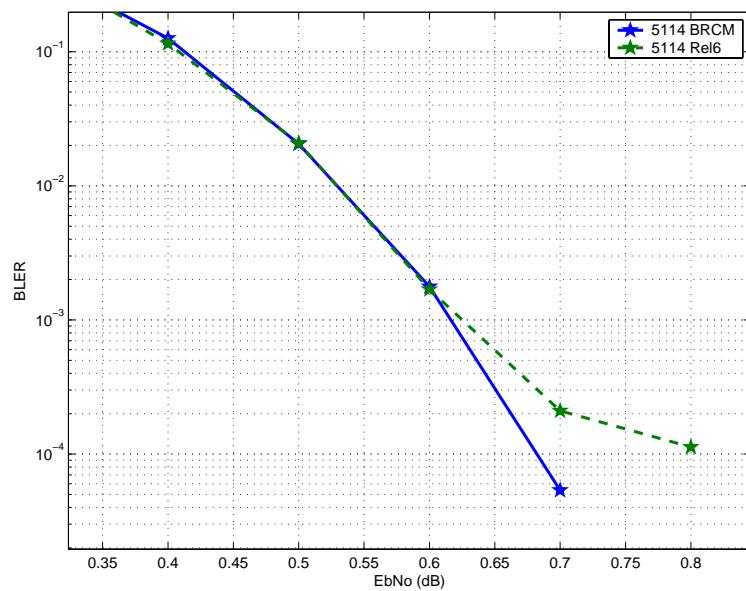
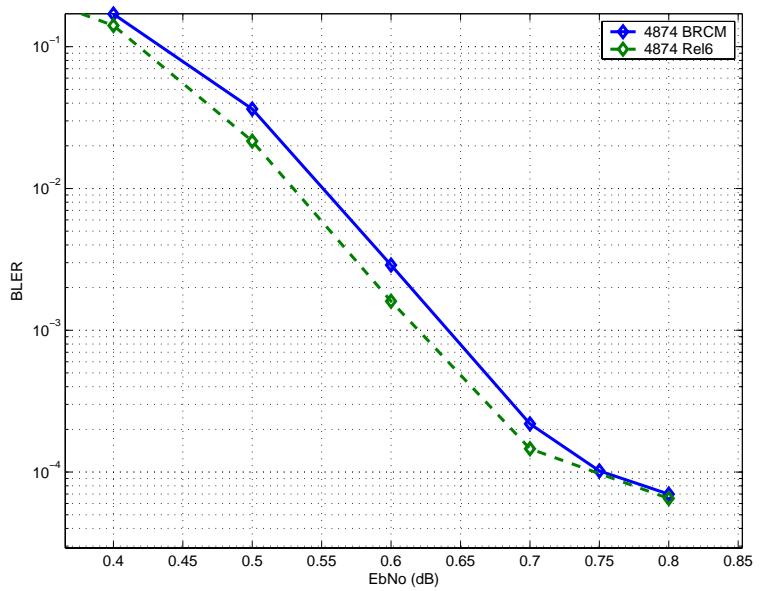


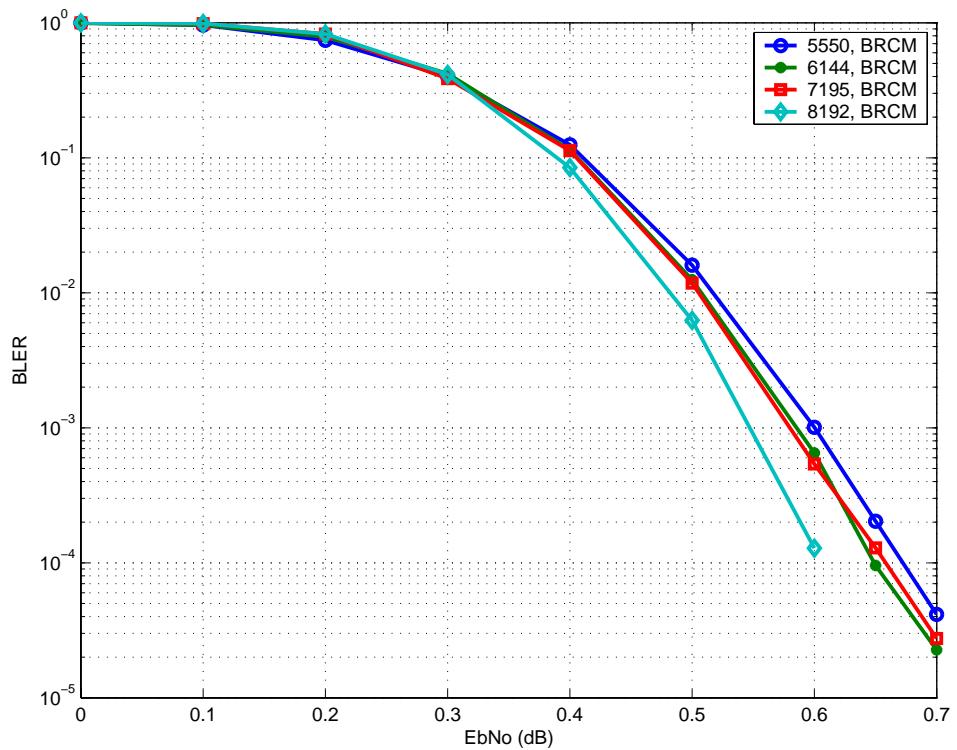












6 References

- [1] 3GPP TS 25.212 V6.8.0 (2006-06)
- [2] C. Berrou, Y. Saouter, C. Douillard, S. Kerouédan, and M. Jézéquel, "Designing good permutations for turbo codes: towards a single model," *2004 IEEE International Conference on Communications (ICC)*, Vol.: 1, pp: 341- 345, 20-24 June 2004.
- [3] Proposed way forward on turbo interleaver (tc_info_sizes_test_mot_nov14.txt), *3GPP TSG RAN WGI #47 RI-063564*

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