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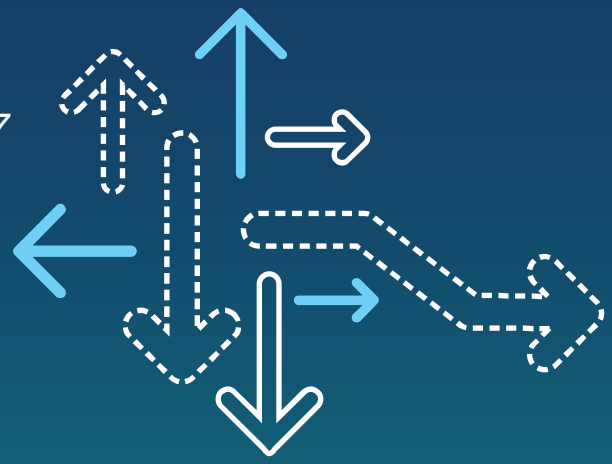
RP-172022

Revision of RP-171607



NR FDD gap analysis

Qualcomm Incorporated

Introduction

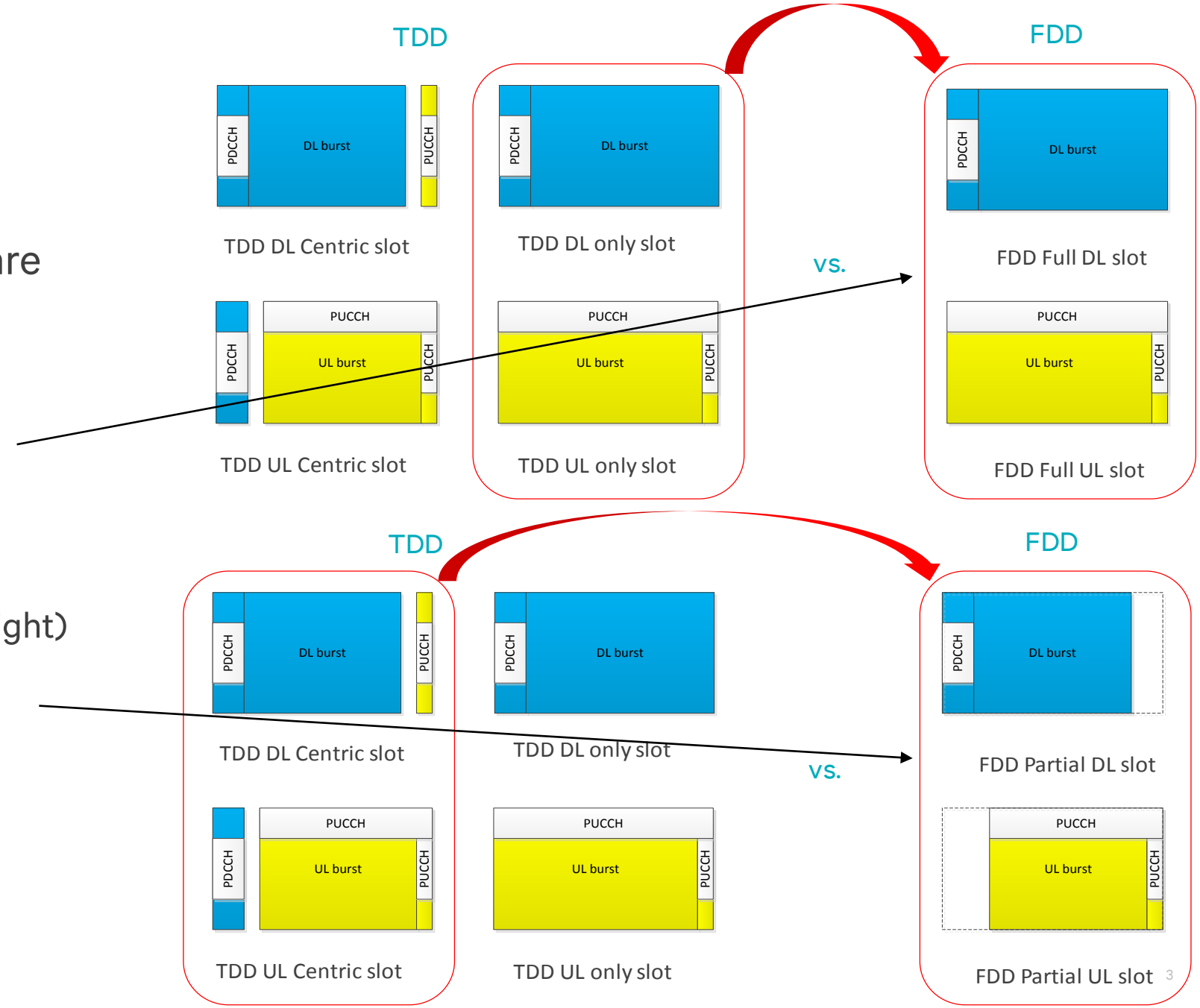
Status of FDD discussions

- There has not been any discussion on FDD operation in RAN1
- The general assumption seems to be that FDD operation is straightforward and does not require RAN1 specification work
- We do not agree with this view and describe shortcomings of the assumed full slot based approach (Option 1 in the following slides)
- At the same time, we propose that FDD can still use the same slot formats as agreed for TDD

Background

Slot formats

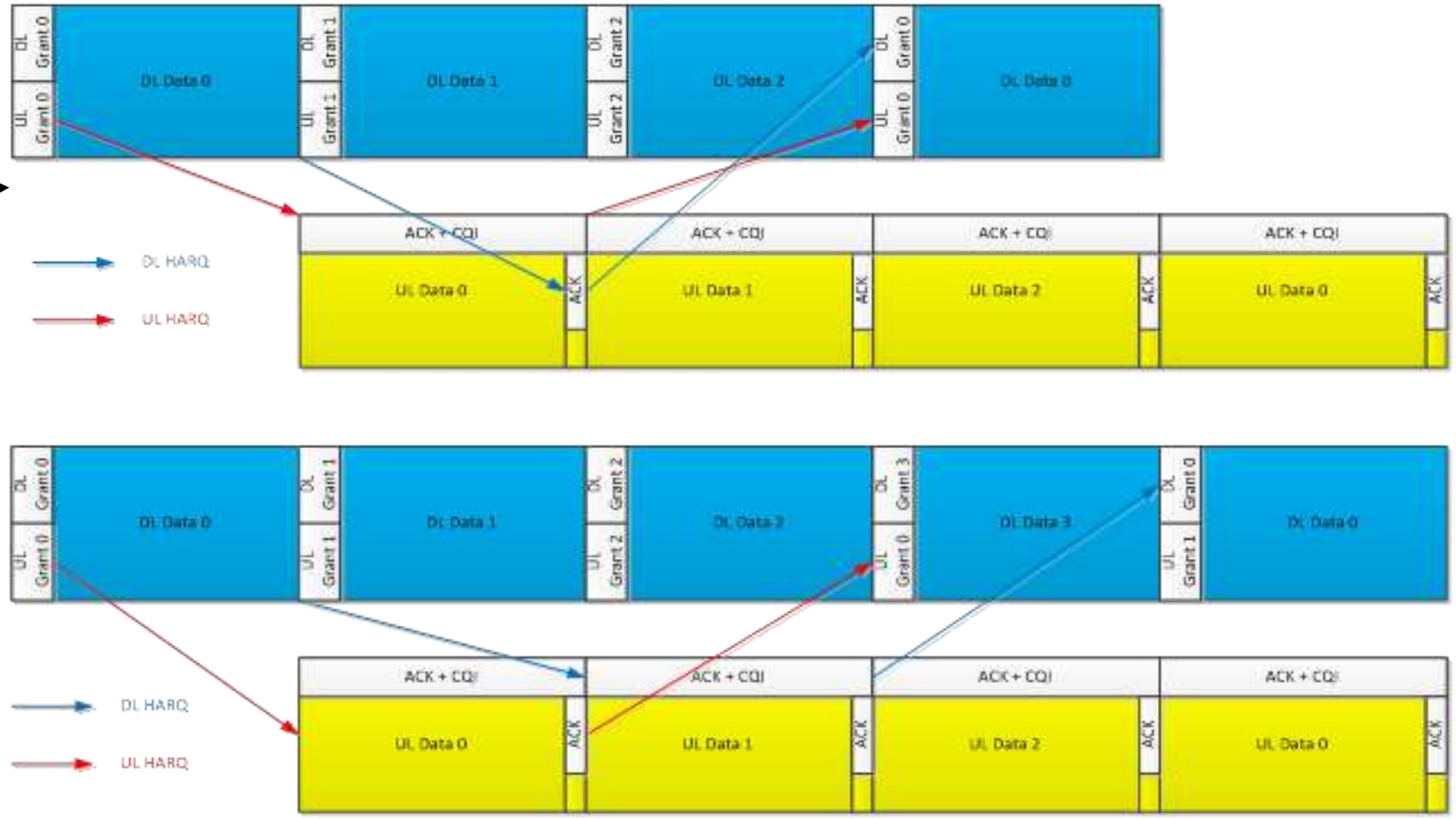
- Two of the TDD slot formats are candidates for use in FDD
  - Full slots (Top Figure on right)
    - Full DL slot (blue)
    - Full UL slot (yellow)
  - Partial slots (Bottom Figure on right)
    - Partial DL slot (blue)
    - Partial UL slot (yellow)



Full slot based solution

Negative impact on latency

- **Assumed FDD Option 1: Use full DL and full UL slots**
  - Case of short PUCCH
    - 3 DL HARQ processes
    - 3 UL HARQ processes
  - Case of long PUCCH
    - 4 DL HARQ processes !
    - 3 UL HARQ processes
- Problem: Similar latency as with TDD self-contained subframes could not be achieved !



Mini-slot based solution

Negative impact on control overhead

- **Assumed FDD Option 2: Use mini-slot version of full DL and full UL slots**

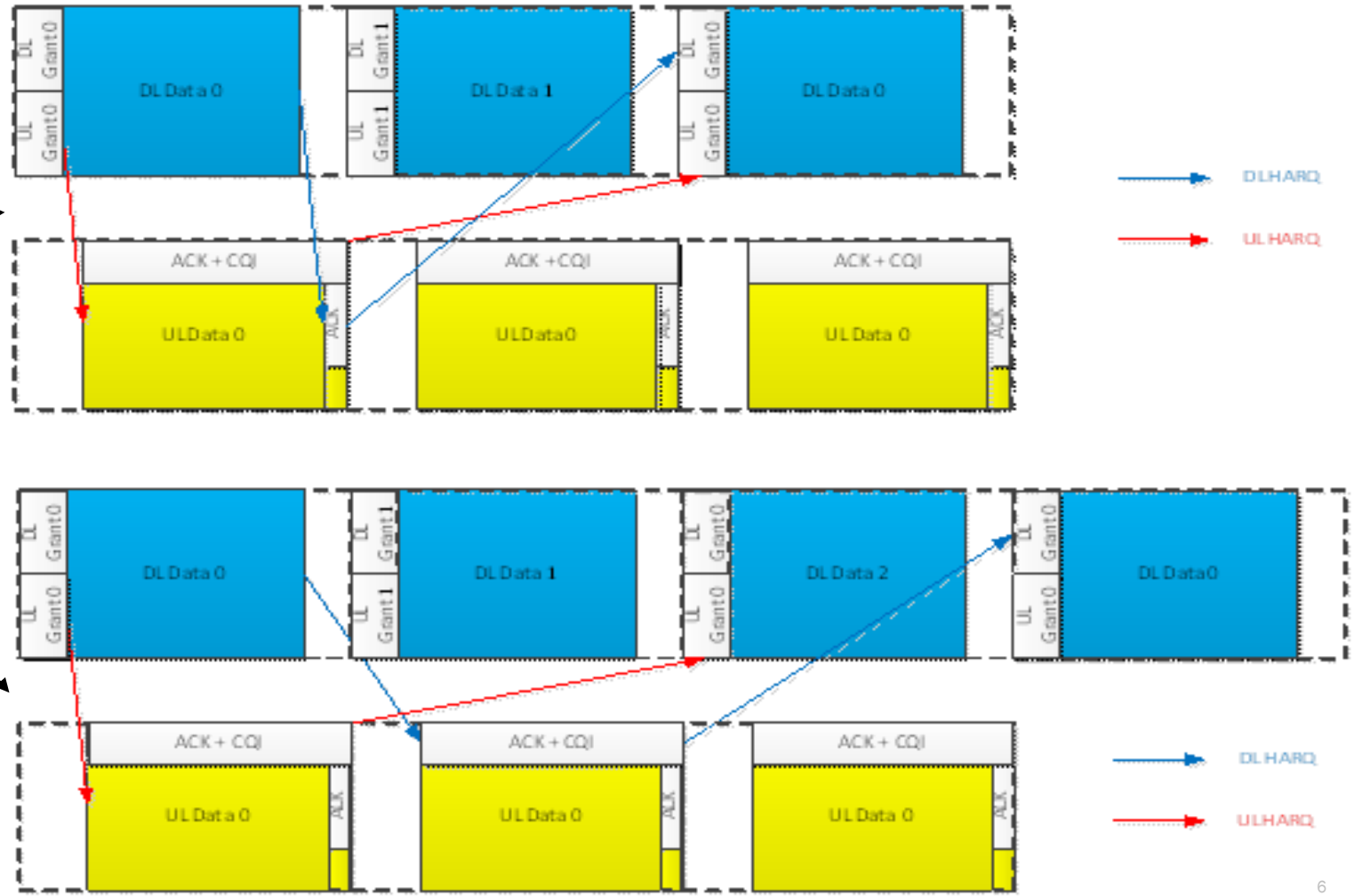
- Similar figures could be drawn as in previous slide but with each unit being a mini-slot instead of a slot
  - Still 3 or 4 HARQ interlaces required but delay scales proportional to mini-slot vs. slot duration ratio

- Problem: When relying on mini-slot for sustained data transfer (i.e. case of large packets requiring many continuous mini-slots transmissions) there is a significant control overhead with this approach

Partial slot based solution

Additional mechanism required to recover blanking loss

- **Assumed FDD Option 3: Use partial DL and UL slots**
  - Case of short PUCCH
    - 2 DL HARQ processes
    - 2 UL HARQ processes
  - Case of long PUCCH
    - 3 DL HARQ processes
    - 2 UL HARQ processes
- Additional solution for recovering the blanking loss is needed



Half Duplex - FDD Operation (1/2)

Better Coverage, Battery Life, and Lower Cost

- HD-FDD advantages compared to FD-FDD
  - Better coverage and power consumption (duplexer-less)
    - Many FDD bands are “tough” for full-duplex RF implementation due to small duplexing gap
      - E.g., Band 2, 3, 5, 7, 8, 12, 13, 14, 17, 20, 22, 25, 26, 27, 28, 30, 31, 68
    - Duplexer insertion loss leads to higher Tx power consumption and large REFSENS loss (up to a few dB)
  - Lower cost for multi-band implementation (duplexer-less)
    - 10-20 duplexers are typically needed for phones with roaming capability
- HD-FDD disadvantages compared to FD-FDD
  - No simultaneous DL/UL transmission.
  - 50% single UE resource utilization for FDD spectrum
- LTE HD-FDD is specified but not used for eMBB
  - Large switching overhead and frame structure leads to < 1/3 of FD-FDD peak rate

- Do we want to enable better FDD performance for NR?

Half Duplex FDD Operation (2/2)

Comparison of 3 FDD frame structures

- FDD Option 1 (full slot, e.g., LTE-like): HD-FDD could achieve <=1/3 of FD-FDD peak rate
  - 1 slot DL-Rx, 1 slot Rx-Tx switching + UL Tx (short PUCCH), 1 slot Tx-Rx switching
- FDD Option 2 (uniform mini-slot): HD-FDD could achieve ~1/4 of FD-FDD peak rate
  - 1 mini-slot DL-Rx, 1 mini-slot switching , 1 mini-slot UL Tx, 1 mini-slot switching
- FDD Option 3 (partial-slot): HD-FDD could achieve 78.5% of FD-FDD peak rate
  - 11 symbol DL, 1 symbol switching, 1 symbol UL, 1 symbol switching

Conclusion

Requirements for proposed solution

- We propose that in the December version of Rel-15, an efficient FDD mode is defined
- In particular, Option 1 (Use of full DL and UL slots) should not be adopted as the only solution since it cannot match the TDD slot structure latency and low performance HD-FDD operation
- Consider Option 3 as a baseline solution
  - Also consider optimizations to compensate for the blanking loss
- In general, the FDD specification should meet the following requirements
  - Commonality with TDD slot structures
  - Comparable achievable minimum latency to TDD self-contained subframes
  - Efficient half-duplex operation

Thank you

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